Amal Kundu
Matthew W Hann
Rafael Ordonez

TI Designs – Precision: Verified Design

Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor

TEXAS INSTRUMENTS

TI Designs – Precision

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
ADS7042	Product Folder
OPA314	Product Folder
OPA835	Product Folder

Circuit Description

This Verified Precision Design details the design procedure, simulated results, and showcases the actual performance of a 12-bit discrete data acquisition block using the ADS7042, optimized for extremely low power, small form factor applications for the following ***three different designs***:

1) **Design #1: 12 bit, 500ksps** optimized for current monitoring, battery monitoring, electromyography (EMG), skin impedance, and wearable fitness
2) **Design #2: 12 bit, 1Msps** optimized for hard disc drives, motor control, motor encoders, optical encoders, and optical modules
3) **Design #3: 12 bit, < 1ksps** optimized for tilt, gyro, pressure, temperature, gas, chemical, blood glucose, low voltage (1.8V-3.3V, JESD8-7A), and DC sensor measurements

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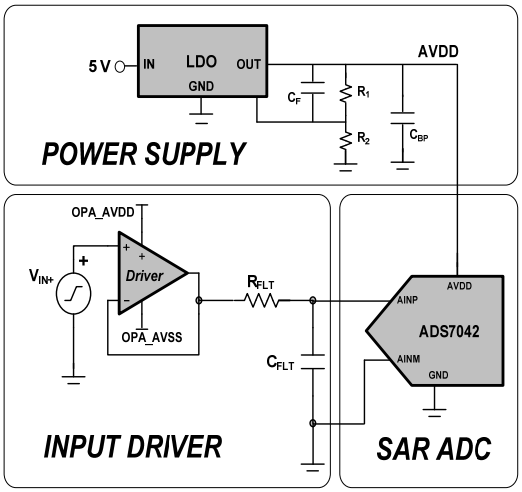

Design	#1	#2	#3
Resolution	12 bit	12 bit	12 bit
Throughput	100-500ksps	500ksps-1MSPS	< 10ksps
Input Driver	OPA314	OPA835	No Driver!
SAR ADC	ADS7042	ADS7042	ADS7042
Power Dissipation	1000µW	2.5mW	< 1µW

ADS7042 Actual Size = 1.5 x 1.5 x .35(H) mm!

1 Design Summary

Table 1 shows the three different application circuits using the ADS7042 for which design summaries will be provided:

Design	#1	#2	#3
Resolution	12 bit	12 bit	12 bit
Throughput	100-500ksps	500ksps-1MSPS	< 10ksps
Input Driver	OPA314	OPA835	No Driver!
SAR ADC	ADS7042	ADS7042	ADS7042
Power Dissipation	1000µW	2.5mW	< 1µW

Table 1: Summary of Three Design Circuits using ADS7042

1.1 Design #1:

This design is optimized for a 500ksps sampling rate and an input signal of 10 kHz.

- Supply Voltage: 3.3 V
- Input: 3.3 V analog signal source
- Output: 12-bit digital output
- Communication Protocol: 3-Wire SPI
- Clock: 16 MHz clock (SCLK)
- Chip Select: 500 kHz chip-select (CSZ)

The design goals & performance are summarized in Table 2; Figure 1 depicts the measured FFT.

Parameter	Goal	Simulated	Actual
Signal frequency (KHz)	10	10	10
Throughput (ksps)	500	500	500
Resolution (bits)	12	12	12
SNR@ 10kHz (dB)	70	70	70
THD@10kHz (dB)	-75	N/A	-77.5
SINAD (dB)	69	N/A	69.4
Power (µW)	1000	950	900

Table 2: Comparison of Design Goals, Simulations, and Measured Performance of DESIGN #1

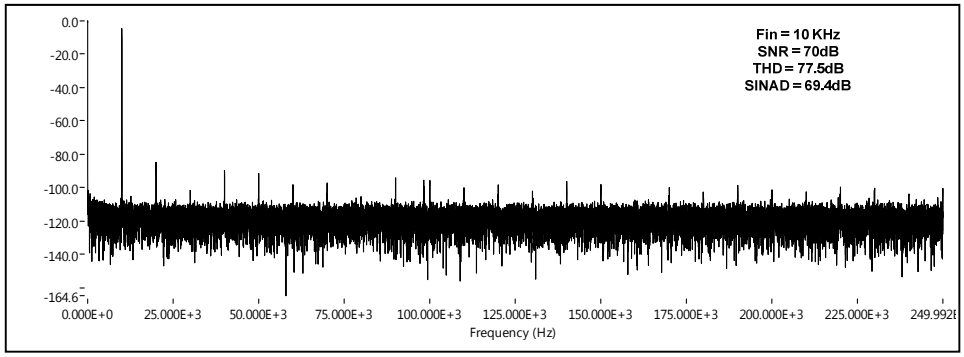

Figure 1: Measured FFT of a 10 kHz input signal with -0.3dB signal power (Design #1)

1.2 Design #2:

This design is optimized for a 1 Msps sampling rate and an input signal of 100 kHz.

- Supply Voltage: 3.3 V
- Input: 3.3 V analog signal source
- Output: 12-bit digital output
- Communication Protocol: 3-Wire SPI
- Clock: 16 MHz clock (SCLK)
- Chip Select: 1000 KHz chip-select (CSZ)

The design goals and performance are summarized in Table 3. Figure 2 depicts the measured FFT for the Design #2.

Parameter	Goal	Simulated	Actual
Signal frequency (KHz)	100	100	100
Throughput (ksps)	1000	1000	1000
Resolution (bits)	12	12	12
SNR (dB)	70	70	70.2
THD@100kHz (dB)	-80	N/A	-84
SINAD (dB)	69	N/A	70.2
Power (µW)	3000	2800	2500

Table 3: Comparison of Design Goals, Simulations, and Measured Performance of DESIGN #2

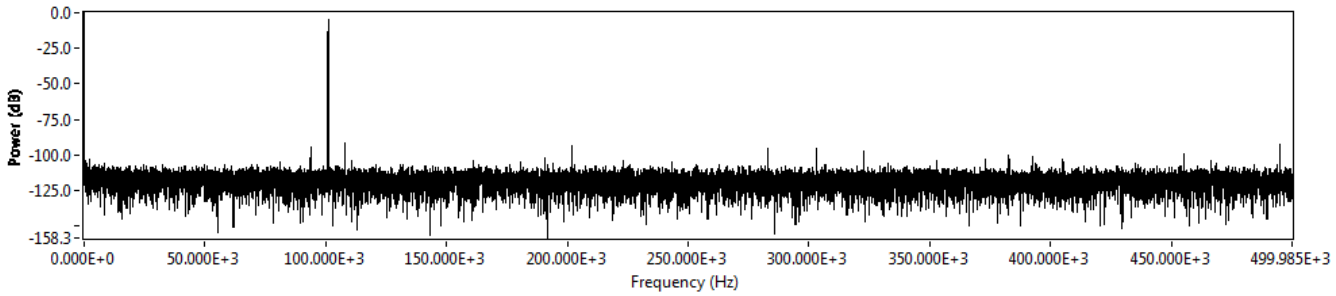

Figure 2: Measured FFT of a 100 KHz input signal with -0.3 dB signal power (Design #2)

1.3 Design #3:

This design is optimized for a 10ksps sampling rate and an input signal of 100Hz.

- Supply Voltage: 3.3 V
- Input: 3.3 V analog signal source
- Output: 12-bit digital output
- Communication Protocol: 3-Wire SPI
- Clock: 16 MHz clock (SCLK)
- Chip Select: 1 KHz chip-select (CSZ)

The design goals and performance are summarized in Table 4. Figure 3 depicts the measured FFT for the Design #3:

Parameter	Goal	Simulated	Actual
Signal frequency (Hz)	100	100	100
Throughput (ksps)	1	1	1
Resolution (bits)	12	12	12
SNR@100Hz (dB)	70	70	70.6
THD@100Hz (dB)	-80	N/A	-83.5
SINAD (dB)	69	N/A	70.4
Power (µW)	1	N/A	< 1

Table 4: Comparison of Design Goals, Simulations, and Measured Performance of Design #3

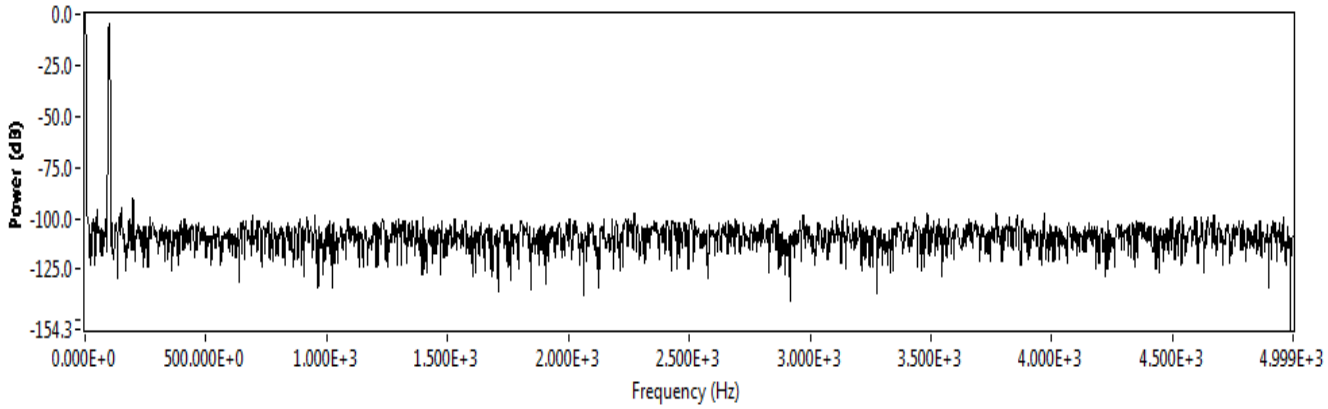

Figure 3: Measured FFT of a 100Hz input signal with -0.3 dB signal power at 1ksps (Design #3)

2 Theory of Operation

Table 5 summarizes the key design tradeoffs for a low power data acquisition block based on a successive approximation register (SAR) analog to digital converter (ADC) and Figure 4 shows the design steps that will be discussed in this document to optimize the following three design scenarios: (1) Design #1: Optimization of the drive amplifier and anti-aliasing filter for lowest power, smallest size, and sampling rates up to 500ksps. (2) Design #2: Optimization of the drive amplifier and anti-aliasing filter for lowest power, smallest size, and sampling rates up to 1Msps. (3) Design #3: Elimination of the drive amplifier to interface with a low impedance sensor and achieve an effective number of bits (ENOB) of up to 10 bits for input signal frequencies below 1 kHz.

Requirement	General Benefit / Tradeoff
Drive Amplifier Output Impedance (R_o)	• Achieving low power means that signal chain components such as operational amplifier (OP AMP) drivers need to be minimized. • If the sensor output impedance and sampling rate of the ADC are low enough, a direct connection to the ADC may be possible.
Input Signal Amplitude (V_P)	• The sensor's full scale output range must be comprehended to utilize the full dynamic range of the ADC. • If the zero scale reading produces a negative output, it must be compliant with ADC's input range or level shifted. • If the full scale output voltage is beyond the compliance of the ADC, attenuation needs to be implemented. • Any type of level shifting or attenuation will require a circuit that adds power consumption.
Input Signal Frequency (f_{in})	Higher input frequencies require higher sampling rates, which translate into settling time. This may not be achievable without an OP AMP buffer, which will inherently draw more power.
Effective Number of Bits (ENOB)	• The ENOB is directly related to both the noise and distortion in an analog signal chain. • The higher the input frequency, the more that distortion can inherently suffer from the increase of the noise bandwidth of a front end driver and internal component mismatches and latency.
System Response Time (T_{resp})	This is a function of how quickly the system needs to respond when the ADC is issued a "convert" command
Power Consumption (P_d)	This is largely dependent on the following factors: • Analog Power Supply • Sampling Rate • Power in the amplifier driver

Table 5: Summary of Key Design Requirements and Tradeoffs

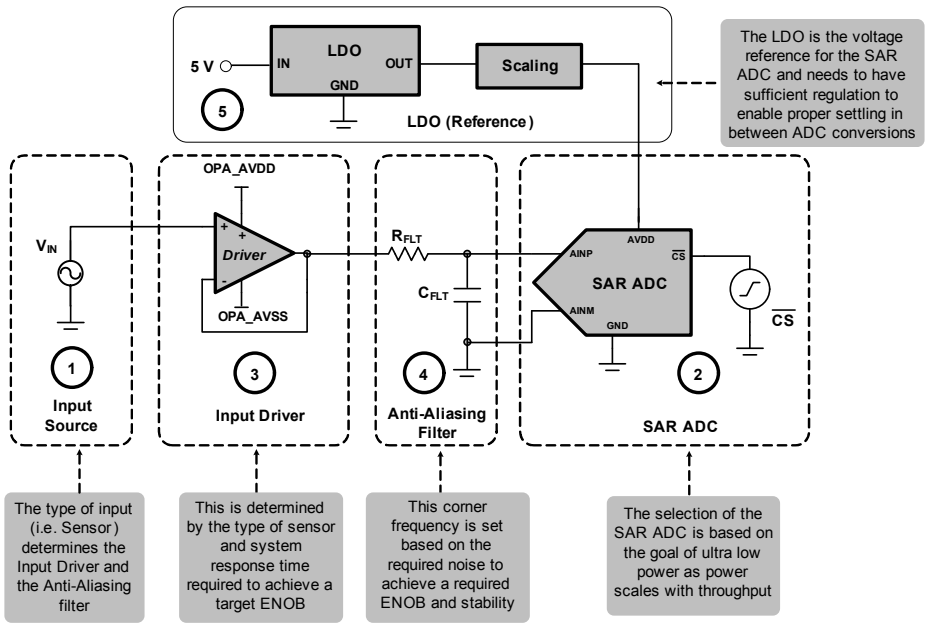

Figure 4: Block Level View of Low Power Data Acquisition Design Steps

2.1 Input Source Considerations

Design #1 (500ksps): If the input signal has an output that is high impedance and low input frequency, it is necessary to optimize the input driver block (#3 in Figure 4) using a low power amplifier. This is important to isolate the ADC input from the output impedance of the input source. The amplifier also helps to provide the output current drive required to produce a settled value from the charge loss due to the internal switched capacitive inputs of the SAR ADC.

Design #2 (1MSPS): If the input signal is greater than 10 kHz and a response time of < 2µs is required, it is necessary to optimize the input driver block (3) using a higher bandwidth amplifier that still maintains the power requirements and ENOB for a given application.

Design #3 (1ksps): The critical parameter of interest is the output impedance of the input source. If the input is very slow moving, has an output impedance that is low, and the overall system ENOB is not a critical parameter, it is possible to design a circuit where the input driver (see block 3, Figure 4). This type of a use case is of particular interest for applications in which the primary goal is to achieve the absolute lowest power possible. Typical applications that fall into this category are low power sensor applications (temperature, pressure, humidity, gas, chemical).

2.2 Considerations for Selecting the Input Drive Amplifier

Achieving low power can often come at the cost of distortion, which ultimately causes degradation in the overall system ENOB. The two primary contributors to the distortion of the data acquisition block shown in Figure 4 are the input driver (3) and the actual SAR ADC itself (2). System distortion can be introduced in many places in the signal chain, but one of the most common sources is the amplifier. Table 6 gives a summary of the different places where this distortion is introduced:

Requirement	*General Benefit / Tradeoff*
Drive Amplifier Output Impedance (R_o)	The output impedance can affect the amplifier's settling by degrading stability and reducing the output current drive needed to recharge the input filter capacitor during an ADC conversion
Input Signal Amplitude ($V_{in}PP$)	• As the signal increases in amplitude, the **open loop gain** of the amplifier often degrades when the output approaches the supply rail. This degradation is further exaggerated when the output needs to source and sink current. Understanding the conditions under which open loop gain is maintained is important in preventing the introduction of added system distortion. • As the signal increases in amplitude, it is important that common mode input range of the amplifier is not violated as this will add distortion into the system. Oftentimes one of the ways around this is to add a small amount of gain to keep the input range compliant; however, the tradeoff in adding gain is a degradation in small signal bandwidth, open loop gain, and the introduction of added system noise with the gain resistors
Input Signal Frequency (f_{input})	As the input signal increases in frequency, the open loop gain of the amplifier often degrades at -20dB / decade. The amount of acceptable degradation is a function of the target system ENOB and can determine whether a higher bandwidth (and therefore higher current) amplifier is chosen

Table 6: Summary of Sources of Distortion in Input Drivers

Figure 5 shows how when an input signal (Vin) is passed through an amplifier, the amplifier generates harmonics of the input signal as the open loop gain, A(s), changes with input voltage. However, this nonlinearity (NL) gets attenuated by the amplifier's open loop gain when negative feedback is added as in Figure 5. Equation (1) reflects the overall output transfer function including the NL term, which represents a simple depiction of how nonlinearity gets added into a system.

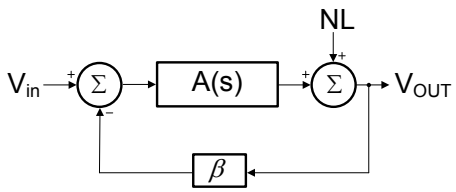

Figure 5: Transfer Function of a Driver Amplifier with Negative Feedback

$$V_{out} = \frac{V_{in} \bullet A(s)}{1 + \beta \bullet A(s)} + \frac{NL}{1 + \beta \bullet A(s)} \quad (1)$$

Driver amplifier distortion has to be negligible to maximize the ENOB of the data acquisition block. As a general design rule of thumb, an amplifier is chosen to be 10dB lower than the ADC distortion to ensure that the total system distortion only degrades ~ 0.5dB.

$$THD_{amp} < THD_{ADC} - 10dB \quad (2)$$

2.3 Considerations for selecting an anti-aliasing filter

2.3.1 Analyzing Input Settling Error using ADC Total Harmonic Distortion

In many cases when settling is considered, it is with respect to the instantaneous voltage droop (ΔV) that results on C_{FLT} as a result of closing the sample and hold switch (see Figure 6). If the value for C_{FLT} is chosen to be much larger than the sampling capacitor (C_{SH}), this droop can be minimal and will not be the dominant source of settling error. However, the input settling behavior of the ADC is impacted by the proper selection and optimization of the values of both R_{FLT} and C_{FLT} for the ADC input filter.

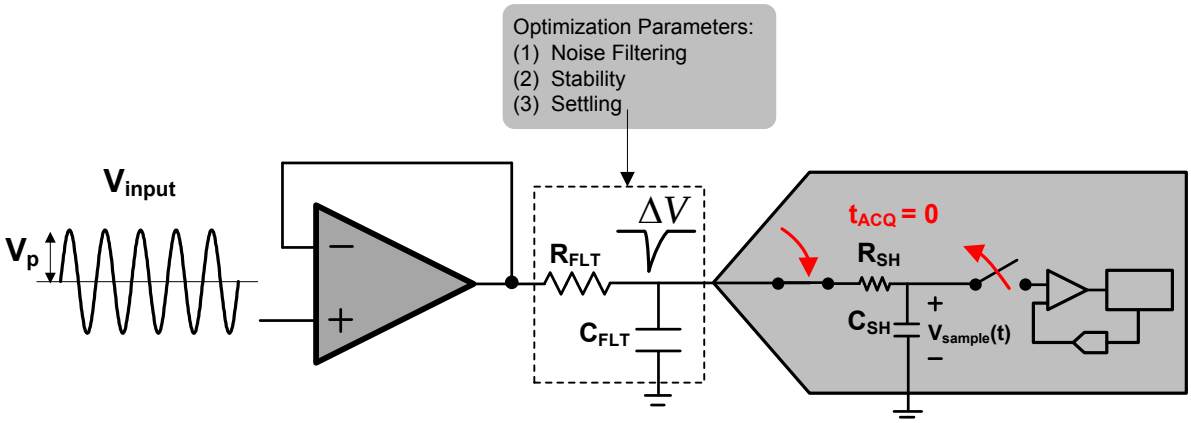

Figure 6. Input Settling Behavior of ADC for Sinusoidal Signal

For a high resolution ADC, it is difficult to measure the settling behavior of the ADC inputs using any external instruments due to the high accuracy requirements. Hence, the best way to measure the ADC input settling is to use the ADC itself. This implies that if the signal at the input of the ADC is not settled to the required accuracy, the error manifests itself in the ADC performance. The two ADC parameters that get affected the most as a results of improper settling are linearity (under dc test conditions) and distortion (under ac conditions). In this section, we will use the distortion performance of the ADC to analyze the overall input settling behavior and derive the necessary equations to design the components of the input filter.

The settling error at the input of the ADC is worst if the input signal changes drastically between any two conversion cycles of the ADC. For AC conditions, this implies that the settling error is worst when the rate of change of the input signal is at a maximum; therefore, the rate of change of a sinusoidal signal is maximum at the zero cross-over point, where the settling error reaches a maximum value, denoted by "Er_{Pk}". At the peaks of the sine wave signal, the input to the ADC changes minimally between any two conversions and hence, the settling error can be assumed to be minimal as well. The empirical variation of the input settling error w.r.t. to the input signal waveform is shown in Figure 7. In this example, the full scale range (FSR) of the ADC is assumed to be 0V to V_{REF}.

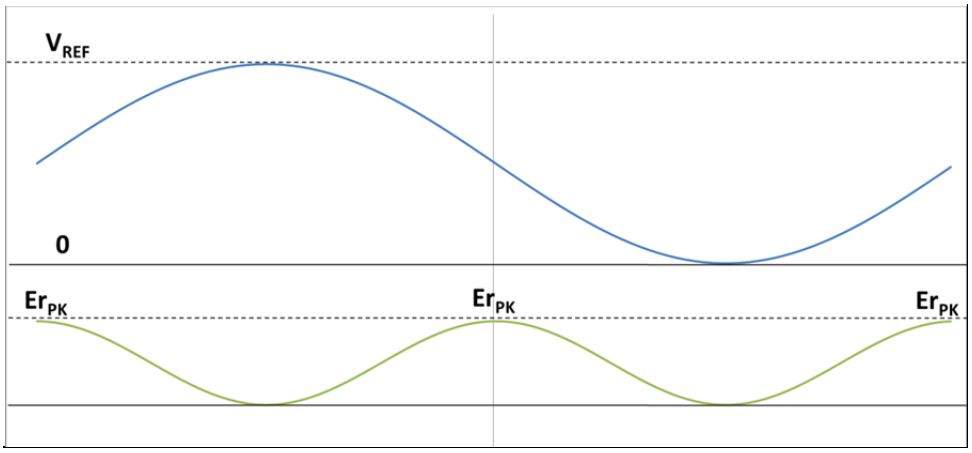

Figure 7: Plot showing variation of ADC Input Settling Error as Function of ADC Input Signal

The error due to settling at the inputs of the ADC impacts the overall distortion performance of the ADC. As shown in Figure 7, the input settling error can be simplified into a second order harmonic of the input signal with a peak value of "Er_{Pk}". In order to minimize additional distortion due to input settling, it is important to minimize the contribution of settling error to the power contained in the harmonic content of the ADC output. The rms value or power content of the settling error response is denoted by:

$$D_{SETTLING} = \left(\frac{Er_{Pk}}{2}\right)^2 + \frac{\left(Er_{Pk} - Er_{Pk}/2\right)^2}{2} = \frac{3 \times Er_{Pk}^2}{8}$$

For an ADC with FSR equal to V_{REF} and total harmonic distortion specified as THD_{ADC}, the total power content of the harmonics is denoted by D_{ADC}:

$$THD_{ADC} = 10\log\left[\frac{D_{ADC}}{\left(V_{REF}/2\sqrt{2}\right)^2}\right]$$

$$\Rightarrow D_{ADC} = \frac{V_{REF}^2}{8} \times 10^{\frac{-|THD|}{10}}$$

The degradation in ADC distortion performance due to input settling can be minimized by ensuring that $D_{SETTLING}$ is much less than the harmonic power, D_{ADC}. In a good design, the ADC input settles properly such that:

$$D_{SETTLING} \leq \frac{1}{10} \times D_{ADC}$$

Under worst case conditions, the peak value of the input settling error can be calculated as:

$$\frac{3 \times Er_{Pk}^2}{8} = \frac{1}{10} \times D_{ADC}$$

$$\Rightarrow \frac{3 \times Er_{Pk}^2}{8} = \frac{1}{10} \times \frac{V_{REF}^2}{8} \times 10^{\frac{-|THD|}{10}}$$

$$\Rightarrow Er_{Pk} = \frac{V_{REF}}{\sqrt{3}} \times 10^{\frac{-(|THD|+10)}{20}} \quad (3)$$

In time domain analysis, the input settling behavior of the ADC is an exponential function of the maximum voltage difference between any two successive conversions, ΔV_{MAX}; minimum time allowed for acquisition of ADC input signal, t_{ACQ} and time constant (τ) of input RC filter.

$$Er_{PK} = \Delta V_{MAX} \times e^{-\left(\frac{t_{ACQ}}{\tau}\right)}$$

The above equation does not account for the attenuation in ΔV_{MAX}, created by the charge sharing effect of the filter capacitor, C_{FLT} and input sampling capacitor, C_{SH} of the ADC. This modifies the input settling equation to the following:

$$Er_{PK} = \Delta V_{MAX} \times \frac{C_{SH}}{C_{SH} + C_{FLT}} \times e^{-\left(\frac{t_{ACQ}}{\tau}\right)}$$

For a sinusoidal input signal varying from 0V to V_{REF}, the maximum rate of change happens at the mid-point, as shown in Figure. Hence the value of ΔV_{MAX} (as illustrated in Figure 8) is given as:

$$\Delta V_{MAX} = t_{CONV} \times \left(\frac{dV}{dt}\right)_{MAX}$$

$$\Rightarrow \Delta V_{MAX} = t_{CONV} \times \pi \times f_{IN} \times V_{REF}$$

Max Rate of Input Signal

$$\left(\frac{dV}{dt}\right)_{MAX} = 2\pi f_{IN} \times \frac{V_{REF}}{2} = \pi \times f_{IN} \times V_{REF}$$

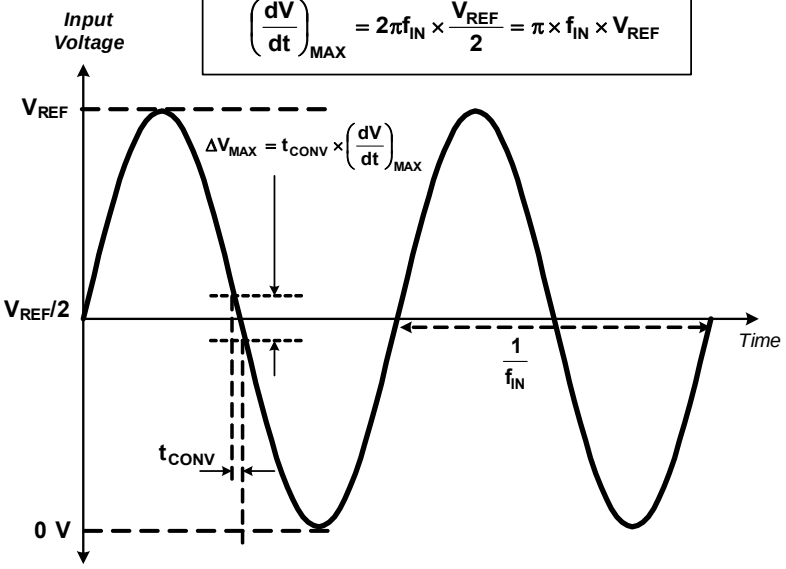

Figure 8. Analyzing Maximum Change in ADC Input for Sinewave Signal

Substituting the value for ΔV_{MAX} in the expression for Er_{Pk}, we get:

$$Er_{PK} = t_{CONV} \times \pi \times f_{IN} \times V_{REF} \times \frac{C_{SH}}{C_{SH} + C_{FLT}} \times e^{-\left(\frac{t_{ACQ}}{\tau}\right)} \quad (4)$$

On combining equations (**3**) and (**4**), we get:

$$\frac{V_{REF}}{\sqrt{3}} \times 10^{\frac{-(|THD|+10)}{20}} = t_{CONV} \times \pi \times f_{IN} \times V_{REF} \times \frac{C_{SH}}{C_{SH} + C_{FLT}} \times e^{-\left(\frac{t_{ACQ}}{\tau}\right)}$$

$$\tau = \frac{t_{ACQ}}{\ln\left[\sqrt{3} \times t_{CONV} \times \pi \times f_{IN} \times \left(\frac{C_{SH}}{C_{SH} + C_{FLT}}\right) \times 10^{\frac{(|THD|+10)}{20}}\right]} \quad (5)$$

The time-constant (τ) is created from the source impedance or filtering-resistor (R_{FLT}), filtering capacitor (C_{FLT}), and sample-and-hold capacitor (C_{SH}) of the ADC, as given below:

$$\tau = R_{FLT} \times (C_{FLT} + C_{SH})$$

Substituting the time-constant (τ) in equation (5) yields a "transcendental function" that can solve for the maximum value of the filtering resistor (R_{FLT}) after picking a filtering capacitor (C_{FLT}).

$$R_{FLT} \leq \left(\frac{1}{C_{FLT} + C_{SH}}\right) \times \frac{t_{ACQ}}{\ln\left[\sqrt{3} \times t_{CONV} \times \pi \times f_{IN} \times \left(\frac{C_{SH}}{C_{SH} + C_{FLT}}\right) \times 10^{\frac{(|THD|+10)}{20}}\right]} \quad (6)$$

Figure 6 shows a simplified model of an amplifier and the sampling circuit internal to a SAR ADC. The sampling capacitor (C_{SH}) of the ADC is connected to the input through the sampling switch during the sampling phase and remains isolated during the conversion phase. Thus at the start of each sampling phase, instantaneous charge is required to charge the sampling capacitor (C_{SH}) to the level of the input voltage. This charge demand creates transient distortion at the amplifier output which can be mitigated through the use of a filter capacitor (C_{SH}), which provides instantaneous charge for the sampling capacitor. The minimum value of the filter capacitor (C_{FLT}) is determined by the maximum allowed droop at the ADC input. Equation (7) is a "rule of thumb" for setting the minimum value of the anti-aliasing filter's capacitance value. The derivation for this is summarized in **SLAU515** by equation 13.

$$C_{FLT} \geq 20 \times C_{SH} \quad (7)$$

Also, since most operational amplifiers are specified to maintain open loop gain with resistive loads ≥ 1kΩ, it is important that at the frequency of interest (f_{input}) that C_{FLT} never exceeds this value to ensure proper settling as shown in equation (**8**).

$$C_{FLT} \leq \frac{1}{2\pi \times 1k\Omega} \quad (8)$$

2.3.1.1 *Stability Considerations for the Anti-Aliasing Filter*

The tradeoff of using a lower value for R_{FLT} is that it can degrade the stability of the driver amplifier reducing phase margin. Designing for good system phase margin can be done through a Bode plot analysis in SPICE, but can also be done analytically if the location of the pole and zero formed by amplifier output impedance (R_o), R_{FLT} and C_{FLT} is known. The structured derivation for this can be found in **SLAU515,** but the overall summary yields the relationship shown in equation (**9**) to optimize stability:

$$R_{FLT} \geq \frac{R_O}{9} \quad (9)$$

2.3.1.2 *Noise Filtering* of the anti-aliasing filter

Knowing the broadband noise of the input driver amplifier (e_n) and the cutoff frequency of the anti-aliasing filter gives the calculation for the integrated RMS noise (e_{n_amp}):

$$e_{n\_amp} = e_n \times \sqrt{f_{filter} \times \frac{\pi}{2}} \quad (10)$$

If root-sum-square of the RMS noise of e_{n_amp} adheres to the requirement set in **SLAU513**, equation 14, the noise of the ADC will dominate the total noise, e_{n_total}:

$$e_{n\_total} = \sqrt{e_{n\_amp}^2 + e_{n\_ADC}^2} \cong e_{n\_ADC} \quad (11)$$

NOTE: If e_{n_amp} is not at least 3x lower than e_{n_total}, this means that either f_{filter} needs to be adjusted or a different drive amplifier selected to achieve a given THD target.

2.4 Voltage Reference (LDO) Design

The precision of a data acquisition system is only as good as its reference source which can directly impact most of the performance parameters of the ADC. As shown in Figure 9, the reference source is comprised of a low drift reference voltage and low impedance buffer. DC accuracy, stability and drive capability are the main design criteria for the reference system. For a high precision data acquisition system with resolution greater than or equal to 14 bits, it is extremely critical to use a dedicated reference circuit to achieve the system performance. A detailed analysis explaining the design and optimization of the reference driver circuit is explained in TIDU512.

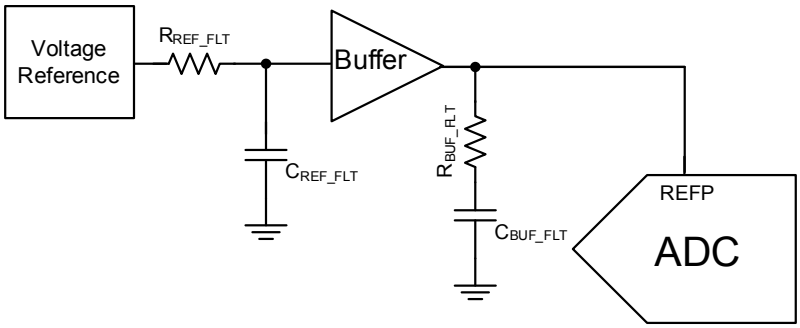

Figure 9: Simplified Diagram of Voltage Reference and Driver

In this TI precision design, the maximum resolution of the system is 12 bits, which significantly relaxes the accuracy requirements of the voltage reference circuit. Hence it is possible to achieve the performance goal by using the power supply of the ADC as the voltage reference. This offers the advantage of reducing the circuit components as well as significantly reduces the overall system power consumption.

The system power supply design usually comprises of a low dropout (LDO) voltage regulator to mitigate any fluctuations in the voltage of the system supply bus. If the LDO output is also used to drive the reference pin of the ADC, then it is important to carefully analyze each specification of LDO and its impact on the system performance. Some key specifications of an LDO and its effect on the system performance are described below:

- **Low Quiescent Current (IQ):** In order to minimize the system power consumption, the IQ of the LDO should be kept as low as possible. It is also important to keep the current constant with respect to the load current. This condition can be met by selecting an LDO with a MOS transistor as the series pass element. Being a voltage-driven device, a MOS transistor does not draw any gate current.
- **Load Regulation:** Load regulation is a measure of the circuit's ability to maintain the output voltage or minimize the voltage variation under varying load current conditions. SAR ADC introduces a dynamic switched-capacitor load on its reference pin. Hence if an LDO is driving the ADC reference, it needs to provide a dynamic current which depends on the throughput, conversion clock frequency and analog input of the ADC. Figure 7 shows a typical load current waveform with conversion clock for a SAR ADC. During each bit decision of an ADC's conversion process, an internal bit capacitor gets charged to the reference voltage, thus leading to a transient glitch on the reference voltage. In

order to ensure system performance, the LDO output must recover from this transient glitch before the next bit decision.

- **Power supply rejection:** Power supply rejection ratio (PSRR), also known as ripple rejection, measures the ability of the LDO to prevent the regulated output voltage from fluctuating due to variations in the input voltage. For any variation in the input supply voltage, it is important to keep the variation in LDO output to be less than 1 LSB in order to ensure the system performance.

  The PSRR is usually specified in LDO datasheets as a function of input frequency. The rejection is usually very high at low input frequencies to better reject the ripples due to 50-60Hz supply frequency. The PSRR goes down as the input frequency goes up. Hence, it is important to consider the highest input frequency to design for the worst case PSSR specification of the LDO.

- **Output Noise:** Noise in the LDO output voltage directly gets manifested in the overall system noise performance. Thus it has to be negligibly small compared to the quantization error of the ADC. Typically a large decoupling capacitor placed much closer to the LDO output pin helps to reduce the wide band thermal noise of the LDO output. Most LDO devices have an external compensation pin to enable customers to connect a bypass capacitor to reduce the output noise. A bypass capacitor, in conjunction with an internal resistor, creates a low-pass filter to further reduce the noise.

- **Stability:** The capacitor helps to minimize the noise from the LDO, but the value of the capacitor cannot be made arbitrarily large as it starts affecting the stability of the LDO. The maximum value of this capacitor is dictated by the stability of the LDO. Using a series resistor at the output of the LDO helps with stability by isolating the capacitor, but it is not recommended to use series resistor in the reference path as it degrades the accuracy of the system. Hence, it is recommended to use a small resistor Radd in series with the output capacitor (Figure) to stabilize the output response of the LDO.

  A typical LDO datasheet provides a graph showing the stable range of the compensation series resistance (CSR) values, since CSR can cause instability with respect to output currents. The CSR is the sum of the equivalent series resistance (RESR) of the output capacitance and the additional resistor (Radd).

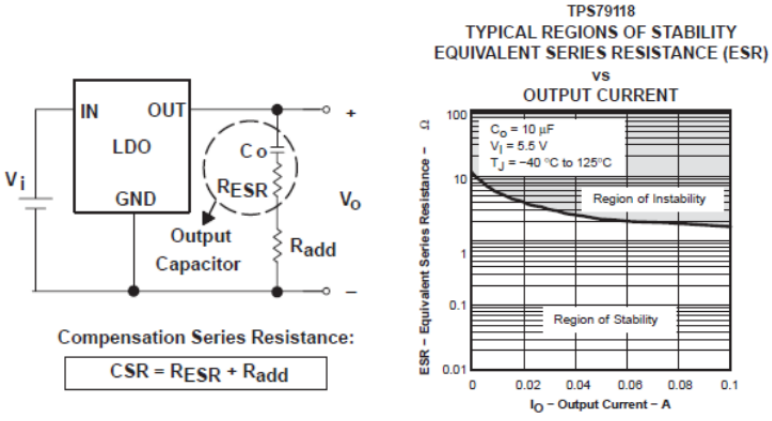

Figure 10: Diagram Showing Effect of Series Resistance on Stability

An additional resistor can be used if the R_{ESR} is too small. An example of a typical stable range of CSR values is shown in Figure 10. The curve shows that CSR must be between 0.2 Ω and 9 Ω so that the LDO regulator is stable. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the CSR requirements.

3 Component Selection

3.1 ADC Selection

3.1.1 Smallest Size:

This design has been optimized for smallest size using TI's 12-bit 1MSPS low power SAR ADC, ADS7042. This ADC makes an excellent choice for designs that have limited board space and very confined form factor as it is available in the ultra-small 1.5 X 1.5 mm 8-pin X2QFN package. See for the actual size of the device:

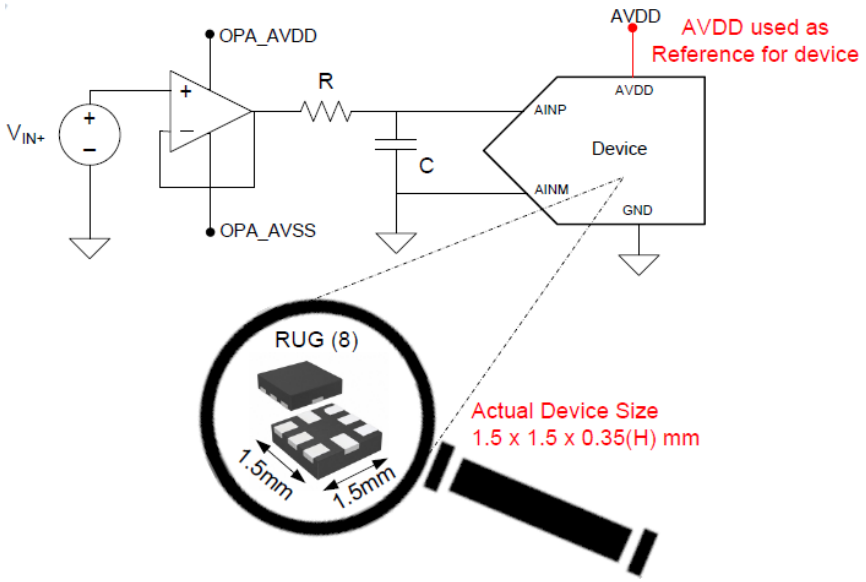

Figure 11: Actual Size Image of ADS7042

3.1.2 Low Power:

The ADS7042 achieves lowest power by optimizing power consumption in both the analog and digital domains.

3.1.2.1 Analog Power Dissipation:

This ADC shares the reference pin with supply and supports operation from 1.8 to 3.6 V. Thus there is no need of having a separate supply source from voltage reference. Figure 12 shows how analog power on the ADS7042 scales linearly with throughput and achieves the following figures of merit for the 3 different designs highlighted in this document:

(1) Design #1

a. **350 µW** power at a throughput of **500ksps** (AVDD = 3.0V)
b. **100 µW** power at a throughput of **500ksps** (AVDD = 1.8V)

(2) Design #2

a. **690 µW** power at its maximum throughput of **1 MSPS** (AVDD = 3.0V)
b. **234 µW** power at its maximum throughput of **1 MSPS** (AVDD = 1.8V)

(3) Design #3

a. **< 1 µW** power at a throughput of **1ksps** (AVDD = 3.0V)
b. **< 500 nW** power at a throughput of **1ksps** (AVDD = 1.8V)

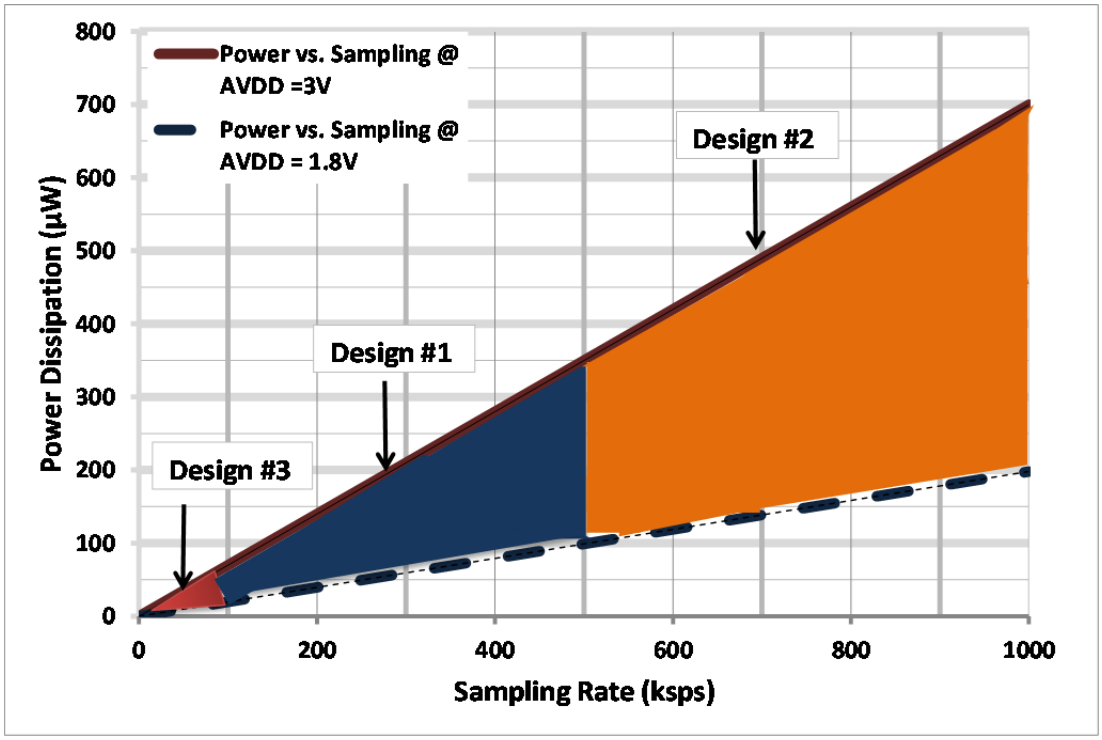

Figure 12: Analog Power Dissipation vs. Sampling Rate (AVDD = 3.3V and 1.8V)

3.1.2.2 Digital Power Dissipation

The ADS7042 supports the ***JESD8-7A standard by supporting a DV_{DD} range down to 1.65V***, which may be set independent of AV_{DD}. This low digital supply voltage gives the ADS7042 an inherent advantage in terms of digital power consumption.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		1.8	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	At 1 MSPS with AVDD = 3 V			230	µA
		At 100 kSPS with AVDD = 3 V			23	µA
		At 1 MSPS with AVDD = 1.8 V		130		µA
P_D	Power dissipation	At 1 MSPS with AVDD = 3 V			690	µW
		At 100 kSPS with AVDD = 3 V			69	µW
		At 1 MSPS with AVDD = 1.8 V		234		µW

Figure 13: Digital I/O Supply Data Sheet Conditions for ADS7042

The ADS7042 supports a simple 3-wire SPI interface and *needs only a 16 MHz clock to achieve a 1 MSPS throughput*, making it very easy to use for most FPGA, DSP, and other simple host controllers. For even lower power consumption, throughput can be controlled simply by reducing the system clock.

PARAMETER		MIN	TYP	MAX	UNIT
TIMING SPECIFICATIONS					
$f_{THROUGHPUT}$	Throughput			1	MSPS
t_{CYCLE}	Cycle time	1			µs
t_{CONV}	Conversion time		12.5 × t_{SCLK} + t_{SU_CSCK}		ns
t_{DV_CSDO}	Delay time: $\overline{CS}$ falling to data enable			10	ns
t_{D_CKDO}	Delay time: SCLK falling to (next) data valid on DOUT			30	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to DOUT going to 3-state	5			ns
TIMING REQUIREMENTS					
t_{ACQ}	Acquisition time	200			ns
f_{SCLK}	SCLK frequency			16	MHz
t_{SCLK}	SCLK period	62.5			ns
t_{PH_CK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{PH_CS}	$\overline{CS}$ high time	60			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

Figure 14: SCLK Frequency for ADS7042

3.2 Driver amplifier selection

3.2.1 Design #1

The goal of each application is to minimize power and maximize dynamic range, so it is important to be able to configure the drive amplifier in a *unity gain buffer*. The OPA314 is an extremely power efficient OPAMP with true rail-to-rail signal swing, a quiescent operating current of only 150 µA, and very low broadband noise. Since its bandwidth is limited to 3 MHz, it is ideal for "Design #1" applications which are limited to sampling rates of less than 500ksps and an input signal frequency less than 10 KHz.

Selection Parameter	Design #1
OP AMP Driver	OPA314
Signal swing(V)	0-3.3
Negative supply (V)	0
Positive supply (V)	3.3
Quiescent Current (µA)	150
Bandwidth (MHz)	3
Noise (nV/√Hz)	14 @ 1KHz

Table 7: Summary of Driver Specifications for Design #1

3.2.2 Design #2

For higher signal frequencies (i.e.100kHz) and sampling rates, the OPA835's 80MHz of gain bandwidth makes it a better choice than the OPA314. The one caveat to using the OPA835 is that it requires some voltage headroom on the inputs which makes the supply requirement more difficult for 0 to V_{REF} signal swing. Table 7 and Table 8 compare the critical performance parameters for these two amplifiers.

Selection Parameter	Design #2
OP AMP Driver	OPA835
Signal swing(V)	0-3.3
Negative supply (V)	-0.7
Positive supply (V)	4.7
Quiescent Current (µA)	250
Bandwidth (MHz)	56
Noise (nV/√Hz)	9.3 @ 100KHz

Table 8: Summary of Driver Specifications for Design #2

3.2.3 Design #3

For lower signal frequencies (i.e. < 1kHz) and sampling rates, if the source impedance from the input is less than 1kΩ, it is still possible to maintain good SINAD without a drive amplifier. The tradeoff of source impedance versus AC performance is summarized in Table 12.

3.3 Anti-aliasing filter selection

Using Equations (**3**) to (**9**), and the considerations developed in the "Theory of Operation, Section 2.3.1," the values for the antialiasing filter can be calculated. These are tabulated in Table 9.

Parameters	Selection Criteria Summary
Filter Cutoff (τ)	• Design #1: For f_{in} =10kHz, f_{sample} = 500ksps, choose τ = 500kHz (higher than Nyquist for settling) • Design #2: For f_{in} =100kHz, f_{sample} = 1Msps, choose τ = 5MHz (higher than Nyquist for settling) • Design #3: For f_{in} =100Hz, f_{sample} = 1ksps, choose τ = 1kHz
C_{FLT} Value	• Design #1: For f_{in} =10kHz, f_{sample} = 500ksps, choose C_{FLT} = 1.59nF (see Equations (**7**)and (**8**)) • Design #2: For f_{in} = 100kHz, f_{sample} = 1Msps, choose C_{FLT} = 1.59nF(see Equations (**7**)and (**8**)) • Design #3: For f_{in} =100Hz, f_{sample} = 1ksps, choose C_{FLT} = 1.59nF (see Equations (**7**)and (**8**))
C_F Type *Important*	Choose a COG which is much higher quality than an X7R. The X7R yields spurious harmonics in the FFT because its value of C changes with applied voltage.
R_{FLT} Value	• Design #1: For f_{in} =10kHz, f_{sample} = 500ksps, choose R_{FLT} = 200Ω (see Equation (**6**) and section 2.3.1) • Design #2: For f_{in} = 100kHz, f_{sample} = 1Msps, choose R_{FLT} =25Ω (see Equation (**6**) and section 2.3.1) • Design #3: For f_{in} =100Hz, f_{sample} = 1ksps, choose R_{FLT} = *See Table 12 showing source impedance vs. SINAD

Table 9: Calculation Results for Designs #1, #2, and #3

3.4 Power supply and voltage reference selection

ADS7042 shares the supply pin with reference and supply voltage works as a reference. Thus either a low voltage LDO or reference source with sufficient drive strength may be used. TPS79101DBVREP is a low voltage drop regulator and provides 3.3 V output from a 5 V input. This is used as the supply for both ADS7042 and OPA314. There is option for different power supplies to verify the design with OPA835 on the same PCB. Thus actual PCB space looks larger than actual requirement.

4 Simulation

This circuit has been simulated to verify several critical system level functionalities and parameters like: allowable signal swing, stability of the driver amplifier, noise contribution from the driver amplifier, ADC timing signals and transient settling of the sampled signal.

4.1 DC signal swing

The TINA-TI schematics for dc signal swing and AC loop gain simulation are shown in Figure 15: TINA-TI Simulation Circuits for Input Drivers for Designs #1Figure 15 and Figure 16, respectively. DC simulation results presented in Figure 17 show that OPA314 can support a true rail-to-rail signal swing whereas OPA835 needs a large overhead supply on both sides. Thus OPA314 can operate from the same supply and ground while OPA835 needs two different supply voltages for 0-3 V signal range.

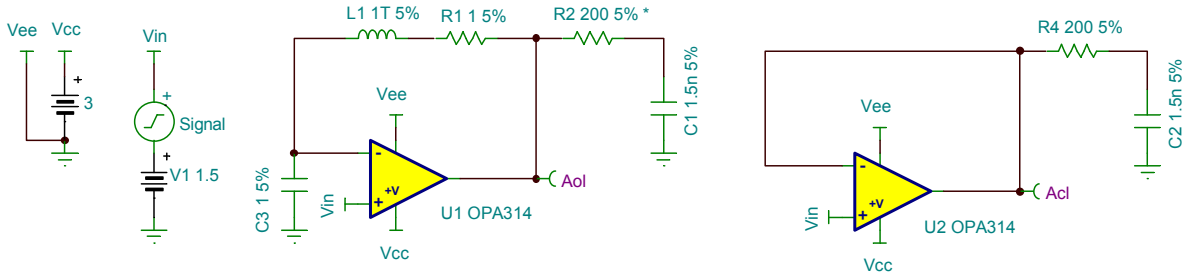

Figure 15: TINA-TI Simulation Circuits for Input Drivers for Designs #1

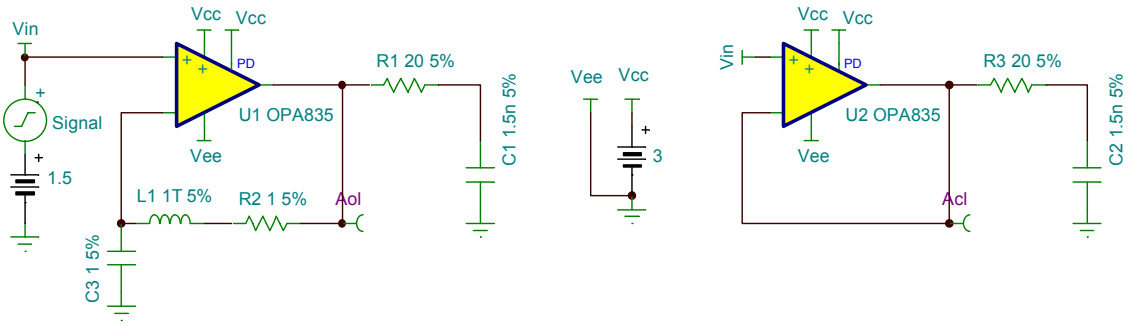

Figure 16: TINA-TI Simulation Circuits for Input Drivers for Designs #2

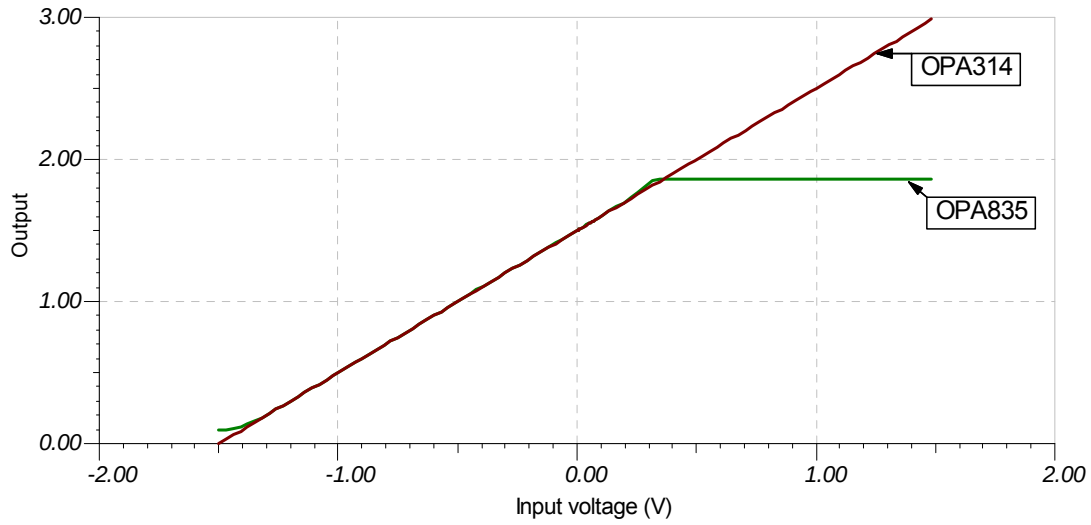

Figure 17: DC Transfer Curve for Design #1 (OPA314) and Design #2 (OPA835)

4.2 Stability simulation

A large inductor of value 1 TH is introduced in the feedback path to break the loop for high frequency and 1 F capacitor provides the ac ground at non-inverting input of the amplifier. The input load of ADS7042 in sampling phase is very small compared to the filter time constant and hardly make any difference to the ac characteristic in the frequency zone of interest. Figure 18 and Figure 19 show frequency responses for design #1 and #2 respectively. Phase margin and loop bandwidth with different RC values are presented in Table 10 for both the designs.

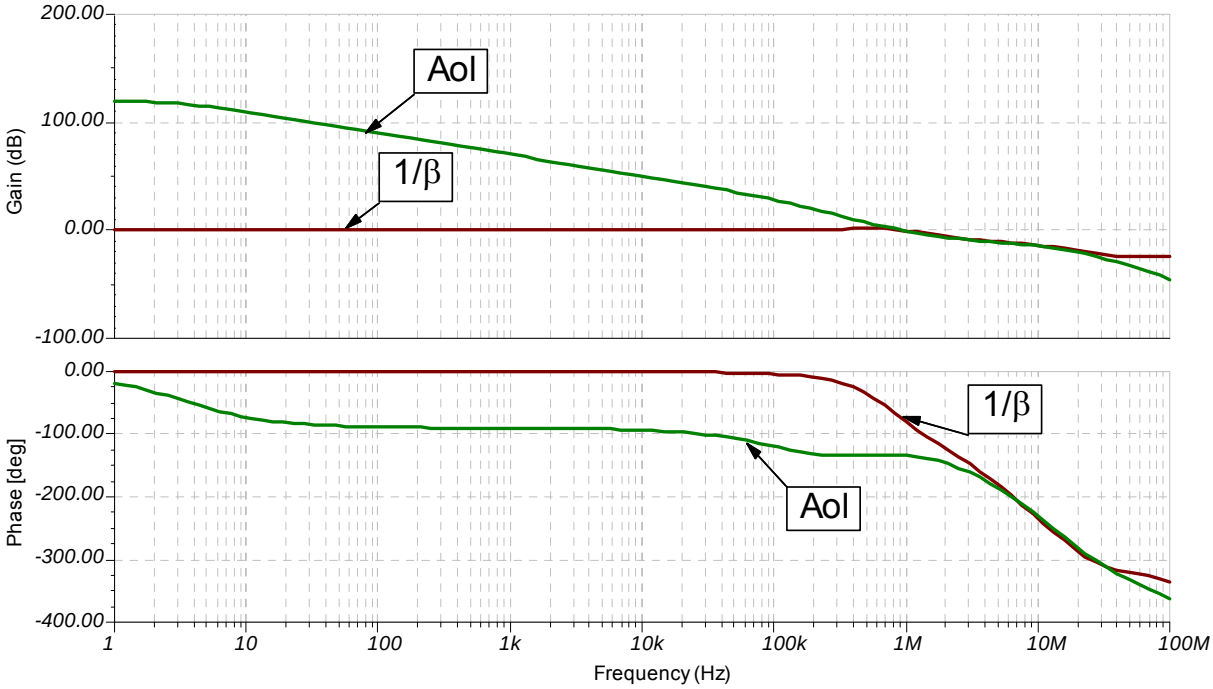

Figure 18: TINA-TI schematic result: AC transfer characteristics for design #1

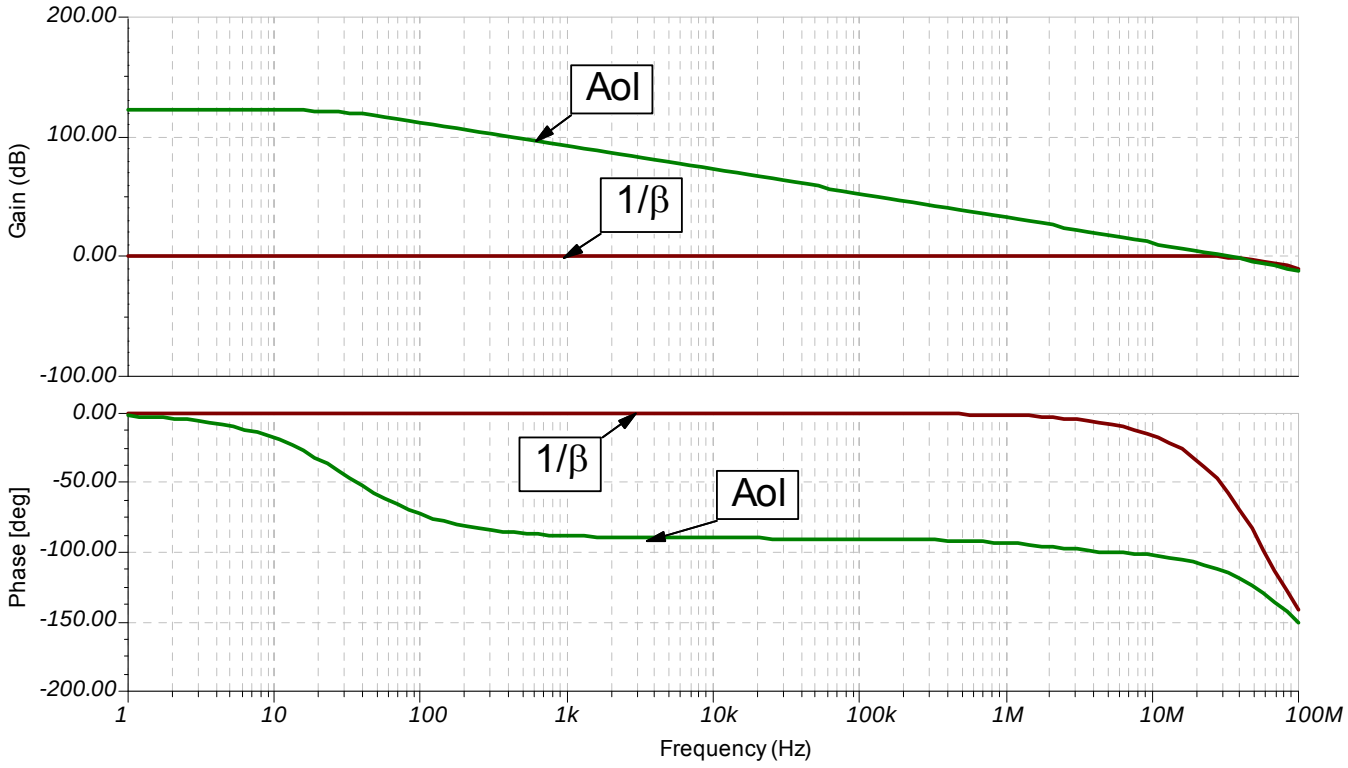

Figure 19: TINA-TI schematic result: AC transfer characteristics for design #2

Design	#1			#2			
R_{FLT} (Ω)	C_{FLT} (nF)	Bandwidth (kHz)	Phase margin (deg)	R_{FLT} (Ω)	C_{FLT} (nF)	Bandwidth (MHz)	Phase margin (deg)
100	1.5	785	48.6	10	1.5	29.2	63
200	**1.5**	**953**	**46**	**20**	**1.5**	**33.7**	**65**
300	1.5	1190	51	30	1.5	35.6	64
200	0.5	1320	26	20	0.5	34.4	61.5
200	2.5	886	54	20	2.5	33.5	65.4

Table 10: Phase margin and bandwidth with filter RC

Simulation data shows larger filter capacitor value helps to improve phase margin at the cost of bandwidth. On the other hand larger resistor value helps to improve both phase margin and bandwidth which degrades the distortion at higher signal frequency. Stability of the amplifier is cross-verified through small signal step response simulation. Here also the ADC input load has been neglected and circuit has been simplified as Figure 20. Step response simulation result is shown in Figure 21 and Figure 22.

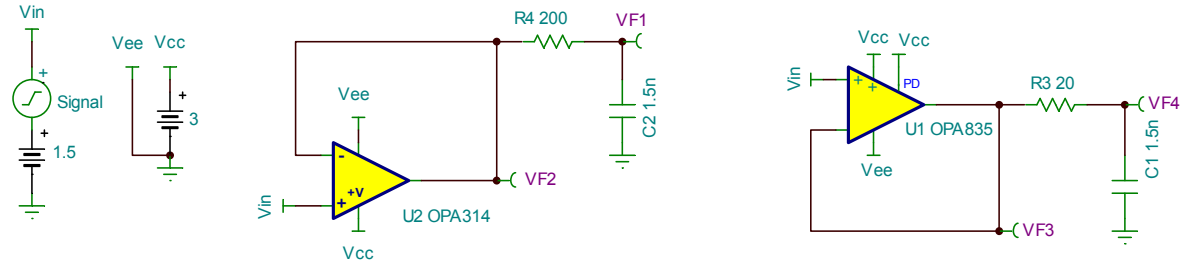

Figure 20: TINA-TI – Schematic for step response and noise simulation

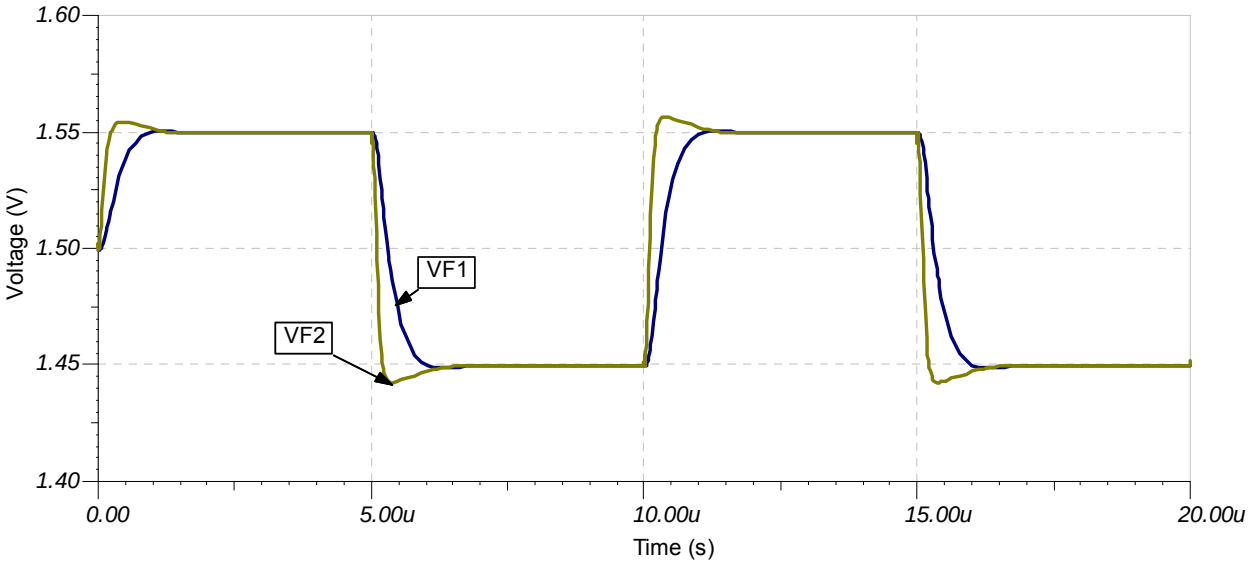

Figure 21: TINA-TI schematic result: Small signal step response for design #1

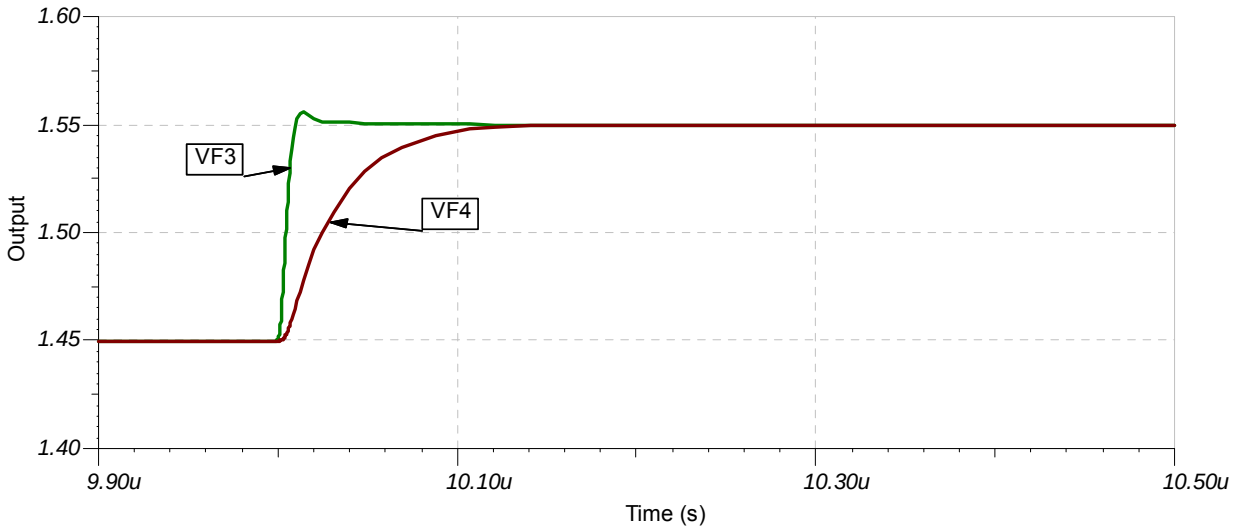

Figure 22: TINA-TI schematic result: Small signal step response for design #2

4.3 Noise simulations

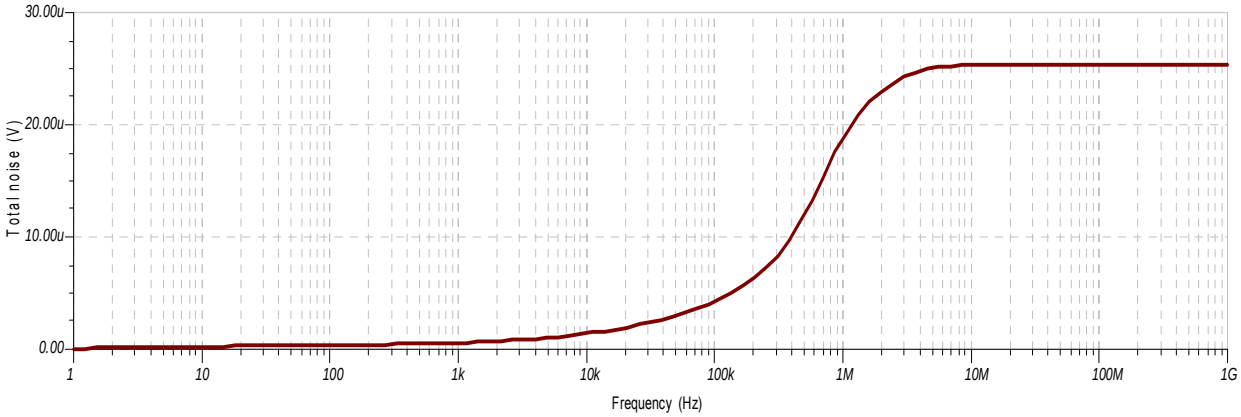

Figure 23: TINA-TI schematic result: Total noise from the driver amplifier for design #1

The noise contribution from the driver amplifier at ADC input is simulated for design #1 with the same schematic shown in Figure 20. Driver amplifier noise contribution at ADC input is 25 µV. ADS7042 noise contribution is typically 316 µV for 3 V reference voltages. Thus total system noise is expected to be

$$e_{n\_total} = \sqrt{(25\mu VRMS)^2 + (316\mu VRMS)^2} = 317\mu VRMS$$

$$SNR = 10\log\left(\frac{P_{signal}}{e_{n\_total}}\right) = 70dB$$

4.4 Timing simulations

Sampling and conversion time is controlled by two timing signals called CSZ and SCLK. SCLK is a free running clock and controls the conversion time. ADC conversion is initiated by the falling edge of CSZ. ADC enters sampling mode at the end of conversion and sampling ends at the falling edge of CSZ. Thus sampling time can be controlled by selecting CSZ pulse width only. ADC sampling and conversion time for 500 KSPS throughput with 16 MHz clock and 500 KHz CSZ is shown in Figure 24. Sampling and conversion time scales linearly with SCLK frequency.

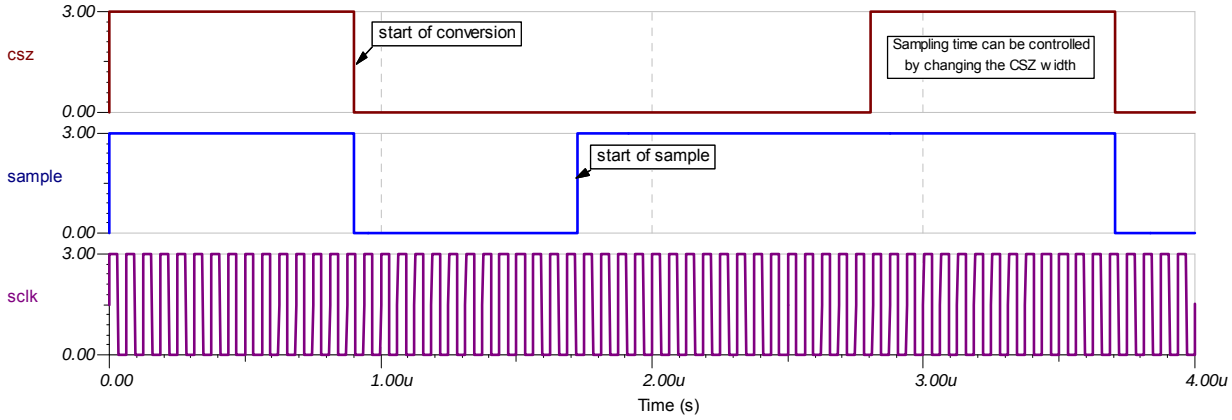

Figure 24: TINA-TI schematic result: ADS7042 timing diagram

4.5 Transient simulations

The TINA-TI™ schematics of the actual data acquisition blocks are shown in Figure 25 and Figure 26. Transient settling of a 10 kHz full-scale sinusoidal signal at 500 KSPS sampling rate is simulated with a 16 MHz SCLK for design #1. Figure 27 shows the accurate settling of the transient glitch at the end of every sample. Zoomed version of the simulation result shows an RC delay between the input and sampled signal but no transient glitch is seen. Design #2 is optimized for higher signal frequency and simulated for a 100 kHz signal. Figure 28 shows the simulated transient waveform for 1 MSPS throughput at 100 kHz signal frequency.

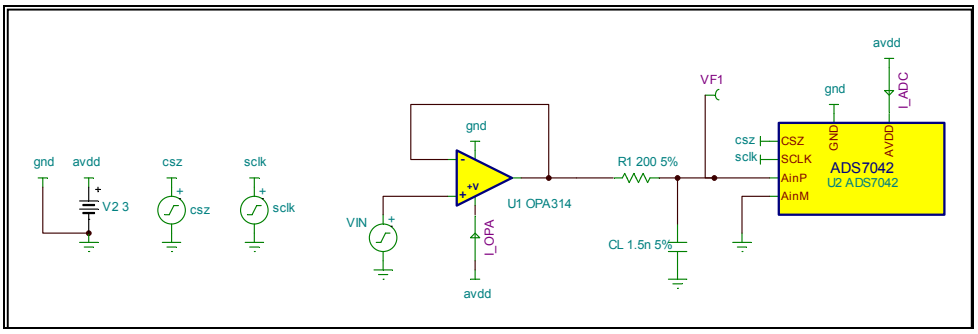

Figure 25: TINA-TI – Schematic for transient response of the track and hold circuit for design #1

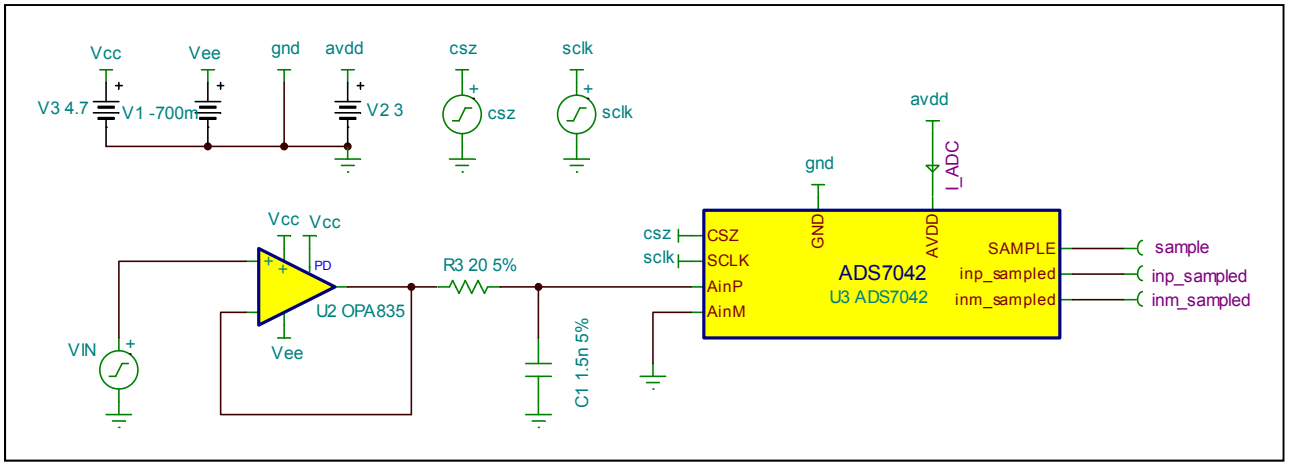

Figure 26: TINA-TI – Schematic for transient response of the track and hold circuit for design #2

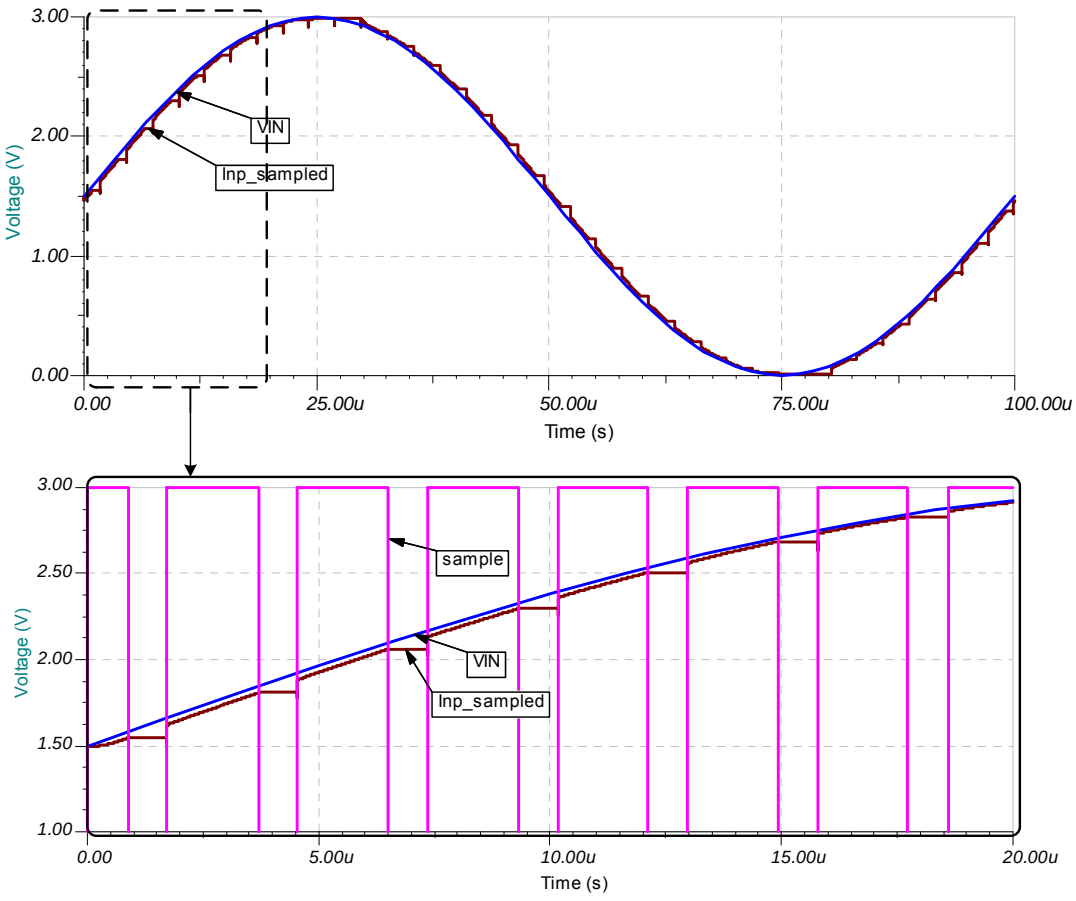

Figure 27: TINA-TI Schematic simulation result: settling of a 10 kHz input signal for design #1

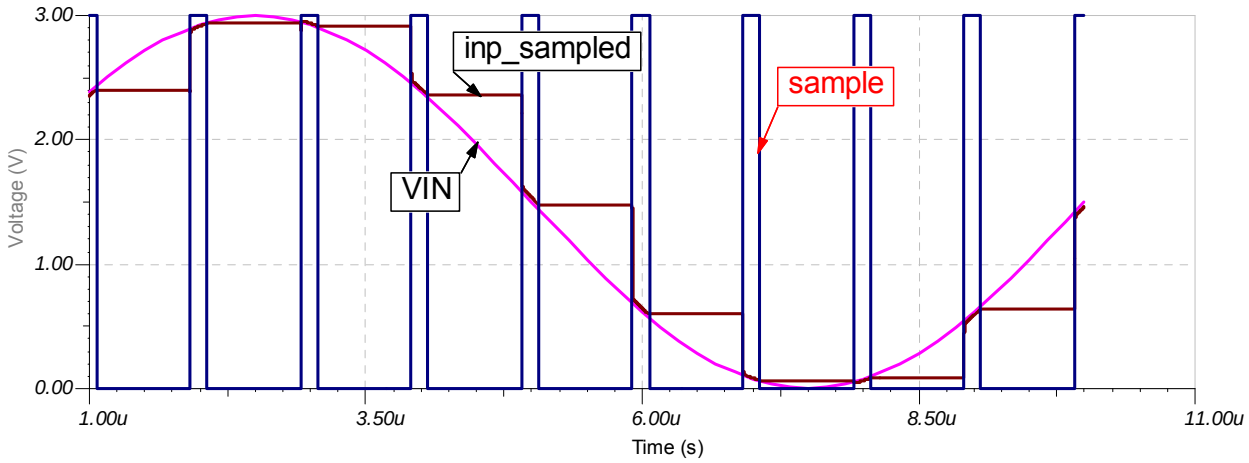

Figure 28: TINA-TI Schematic simulation result: settling of a 10 kHz input signal for design #2

5 PCB Design

The PCB schematic and bill of materials are available in Appendix A. The circuit was developed on a simple 4 layer PCB with two dedicated plane layers for GND and supply. The final PCB dimension is 5.85 X 3.8cm. Figure 29 shows the layout of the board. Critical layout concerns are listed below:

- The decoupling capacitors are placed close to the device supply pin. Because the analog supply is also used as the internal voltage reference, it is necessary to ensure that a1uF capacitor is placed close to each supply pins of ADS7042 to ensure optimal filtering.
- Series termination resistors for each high frequency signal should be placed close to the source. 49.9 Ω resistors are being used for SCLK, CSZ and SDO with 50 Ω trace.
- The input driver circuit, comprised of OPA314 should be located as close as possible to the input of the ADC to minimize loop area, thus making the layout more robust against EMI/RFI rejection. Similarly, the resistor and capacitor of the anti-aliasing filter at the inputs of the ADC should be kept close together and close to the inputs of the ADC to minimize the loop area. The length of the feedback paths and parasitic capacitance at the amplifier input should be minimized to avoid undesirable oscillations.

5.1 PCB Layout

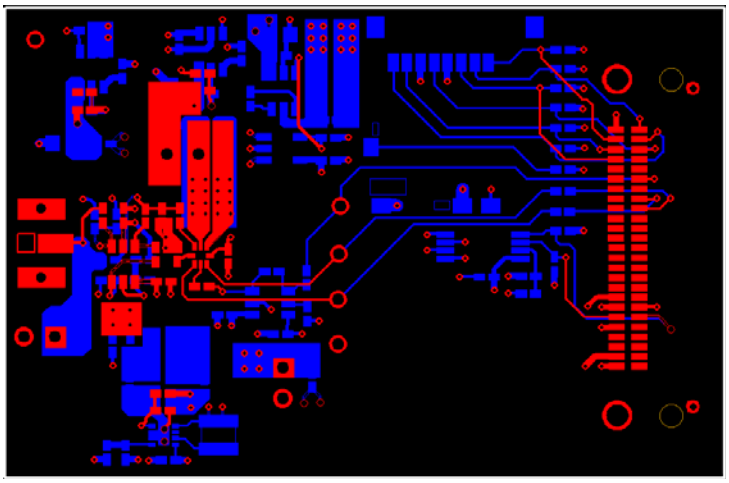

Figure 29: PCB Layout for ADS7042 Test Board

6 Verification & Measured Performance

6.1 Results & Performance Summary for 3 Design Options (Design #1, Design #2, Design #3)

Table 11: Comparison of Design Goals vs. Measured Performance of 3 DesignsTable 11 shows a summary of the performance results of each of the 3 designs vs. the actual design goal:

Parameter	Design #1 Goal	Design #1 Actual	Design #2 Goal	Design #2 Actual	Design #3 Goal	Design #3 Actual
Signal frequency (KHz)	10.00	10.00	100.00	100.00	100	100
Throughput (ksps)	500	500	1000	1000	10	10
Resolution (bits)	12	12	12	12	12	12
SNR (dB)	70	70.3	70.0	70.1	70	69.9
THD (dB)	-75	-77.5	-80	-84	-80	-83.5
SINAD (dB)	69	69.4	69	70.2	69	70.4
Power (µW)	1000	900	3000	2500	1	< 1

Table 11: Comparison of Design Goals vs. Measured Performance of 3 Designs

Though OPA314 and ADS7042 make the most power efficient combination for data acquisition system, its performance degrades beyond 10 kHz signal frequency. This design is limited by the OPA314 bandwidth and stability requirements. OPA835 is a good alternative for higher signal frequency and comes with the cost of extra power. Additionally this needs a 5 V and -1 V power supply to support 0-3.3 V signal swing. A much lower filter resistor (R_{FLT} < 20 ohms) can be used for 1.5nF filter capacitor (C_{FLT}). Figure 30 presents the dynamic performance across input frequency showing no additional distortion at 100 kHz signal frequency. Noise degradation is due to the source contribution and can be eliminated by a notch filter. Dynamic performance is measured up to 250 kHz signal frequency with the OPA835 and a 25Ω filter resistance on a PCB board that is not shown in this design document. The input signal is fed through a band-pass filter to eliminate the source noise. Figure 31 compares the dynamic performance between OPA314 and OPA835.

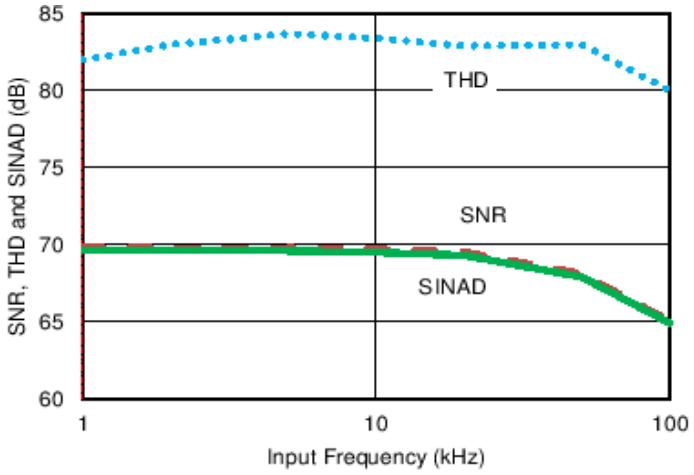

Figure 30: Dynamic Performance of the OPA835 with Frequency

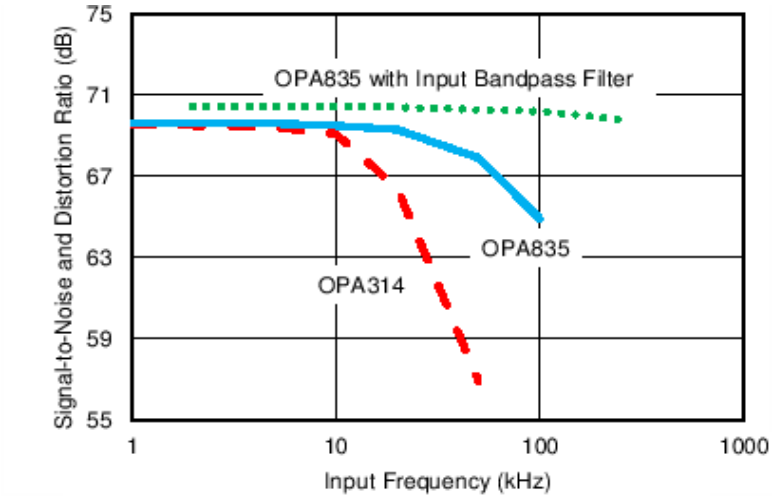

Figure 31: SNR plots with OPA314 and OPA835

6.2 Eliminate the driver amplifier for lower signal frequencies

The input driver amplifier works as a low impedance buffer at the cost of extra power and board space and essential for high frequency signal. The ADS7042 comes with a low value switching capacitor which makes it more conducive to inputs with higher source impedance. Table 12 summarizes the dynamic performance measured with a 2 kHz signal frequency for different filter resistance (R_{FLT}) values, a fixed C_{FLT} value of 1.5nF, and throughputs ranging from 10ksps – 1Msps.

Throughput (ksps)	SINAD for a 2 KHz signal @ -0.5 dB signal (units in dB)						
	R_{FLT} (Ω)	25 Ω	250 Ω	2500 Ω	10000 Ω	25000 Ω	50000 Ω
10		70.01 dB	70.13 dB	70.07 dB	70.10 dB	70.04 dB	69.76 dB
50		70.02 dB	70.03 dB	70.18 dB	69.87 dB	68.50 dB	67.52 dB
100		69.9 dB	70.03 dB	70.08 dB	68.84 dB	67.54 dB	65.88 dB
500		69.97 dB	70.03 dB	67.50 dB	64.63 dB	60.36 dB	x
1000		69.86 dB	69.30 dB	63.55 dB	60.78 dB	x	x

Table 12: SINAD vs. Source Impedance (R_{FLT}) and Throughput

7 Modifications

7.1 Modifications to Circuit #1: Low Power, 12 bit, 500ksps SAR ADC Block

Figure 32 shows an application suggestion using Circuit #1 in a Body Impedance measurement for a wearable fitness band. The measurement is accomplished by using a known ac excitation source, "VIN" with a mid-scale reference voltage to create a current waveform that is proportional to the complex impedance of the body. The current waveform is then converted back into a voltage using the "I-V Converter with Gain" block, after which it get sampled by Circuit #1. Table 13 shows how the trans-impedance amplifier can be modified based on the type of input signal bandwidth needed; likewise, Table 14 shows how Circuit #1 can be modified if lower sampling rates are required for the application.

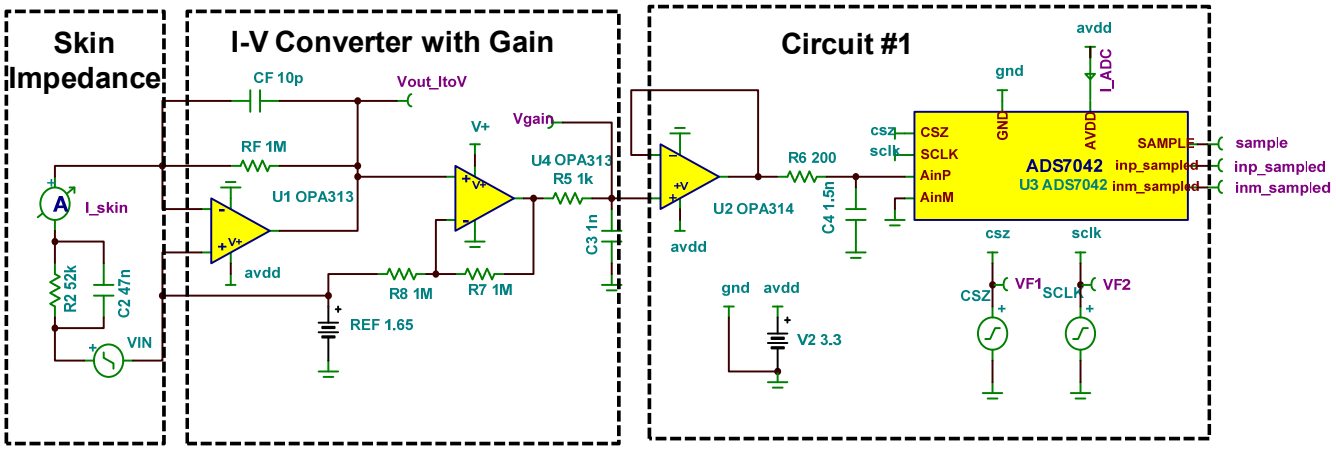

Figure 32: Application Example Using Circuit #2-Skin Impedance Measurement

Input Signal Frequency	I-V Converter (transimpedance amp)	I-V Converter (gain amp)
50 / 60 Hz	OPAx379	OPAx379
1kHz	OPA313 / OPA333	OPA313 / OPA333
10kHz	OPA313 / OPA333	OPA313 / OPA333
50kHz	OPA376	OPA314

Table 13: Amplifier Options for Modifying Figure 32

ADS7042 Sampling Rate	Input Driver for Circuit #1
< 1 ksps	No Driver
1 – 10 ksps	OPA313 / OPA333
10 – 100 ksps	OPA313 / OPA333
100—250 ksps	OPA378
250—500ksps	OPA314

Table 14: Modification Suggestions for Drive Amplifier of Circuit #1 for Different Sampling Rates

7.2 Modifications to Circuit #2: 12 bit, 1MSPS SAR ADC Block

Figure 33 shows an application suggestion using Circuit #2 in a typical single-ended photodiode application. The "photo sensor" block represents the photodiode which generates a current proportional to light intensity which is converted back into a voltage by the "I-V Converter" block and then sampled by "Circuit 2." Table 15boffers some suggestions on how the I-V Converter stage can be modified to achieve different performance points for the photodiode.

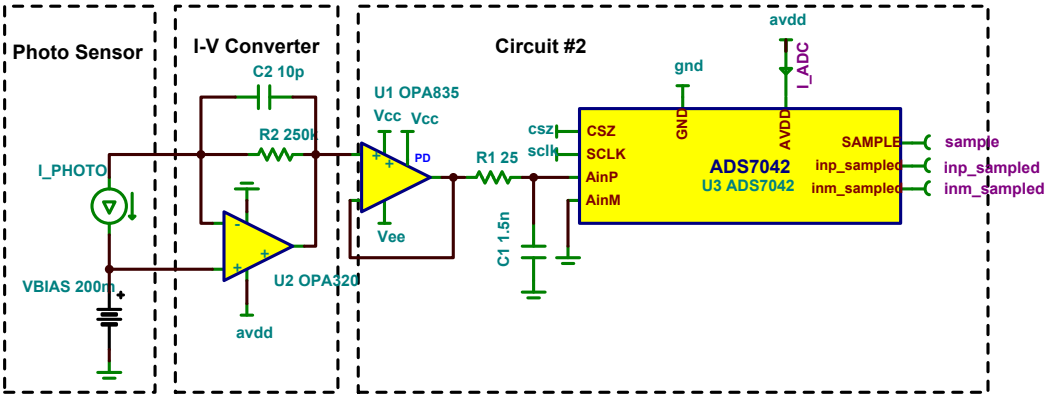

Figure 33: Application Example Using Circuit #2-Photodiode Measurement

I-V Converter (transimpedance amp)	Advantage	Disadvantage
OPAx376	Single Supply, ultra low noise, low input bias current	Good for pulsed signals < 10kHz
OPAx827	Ultra Low Noise, JFET inputs for low IB	Requires Dual supply for operation
OPAx365	Single Supply, Low noise, good BW	Higher Power
OPAx211	Ultra Low Noise	Dual Supplies, Bipolar inputs

Table 15: Amplifier Options for Modifying Figure 33

Figure 34 shows that Circuit #3 can interface directly with a tilt sensor so that ultra-low power and minimal component count can be maintained.

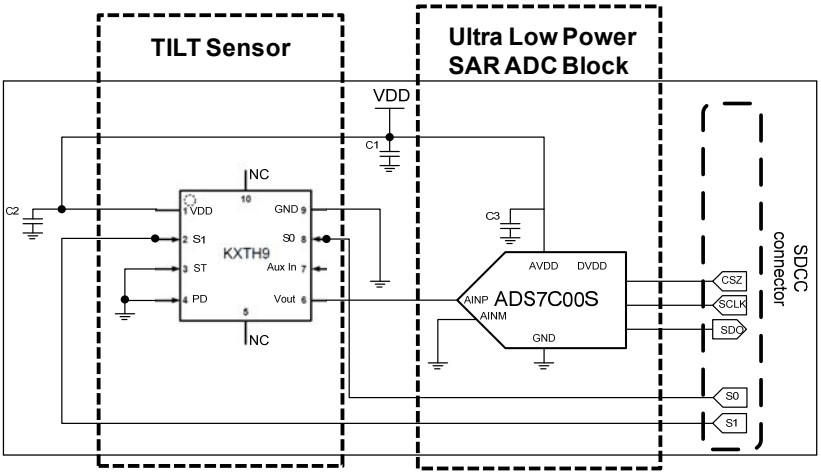

Figure 34: Application Example Using Circuit #3 for a Tilt Sensor Measurement

8 About the Authors

Amal Kumar Kundu graduated from the Indian Institute of Technology - Kharagpur in 2008, where he earned a Master of Science in analog VLSI design. He joined Texas Instruments India in 2008 as an analog design engineer, where he has worked on high speed SAR ADC design and analog front-ends (AFE) for digital X-ray applications.

Matthew Hann is currently the Product Line Manager for the Precision SAR ADC team within Texas Instruments' Precision Analog Business Unit. Matt started his career at Burr Brown in 1998 and spent 8 years as an analog test engineer focusing on precision op amp, instrumentation amp, current shunt monitor, and power amplifier test solutions. Following that, Matt spent 5 years as an analog applications engineer focusing on front end instrumentation, power amplifier drivers, temperature sensing, 4-20mA transmitters, thermal control loops, and medical instrumentation applications.

9 Acknowledgements & references

- *Special thanks to Sandeep Kasargod for his significant contributions to this design. He helped design the PCB board schematic and layout. He also helped to collect the measurement data for the design and was instrumental in many discussions during the process.*

- *Vaibhav Kumar, TI precision Designs: Verified Design: 18-bit, 1MSPS data acquisition block (DAQ) optimized for lowest distortion and noise.*
- *Vinay Agarwal, TI Precision Designs: Verified Design: 18-Bit Data Acquisition (DAQ) Block Optimized for 1-µs Full-Scale Step Response*
- *Amal Kundu & Deepak Mathew, TI Precision Designs: Verified Design: 12 Bit 1 MSPS Single Supply Dual Channel Data Acquisition System for Optical Encoders in Motor Control Application.*

Appendix A.

A.1 Electrical Schematic

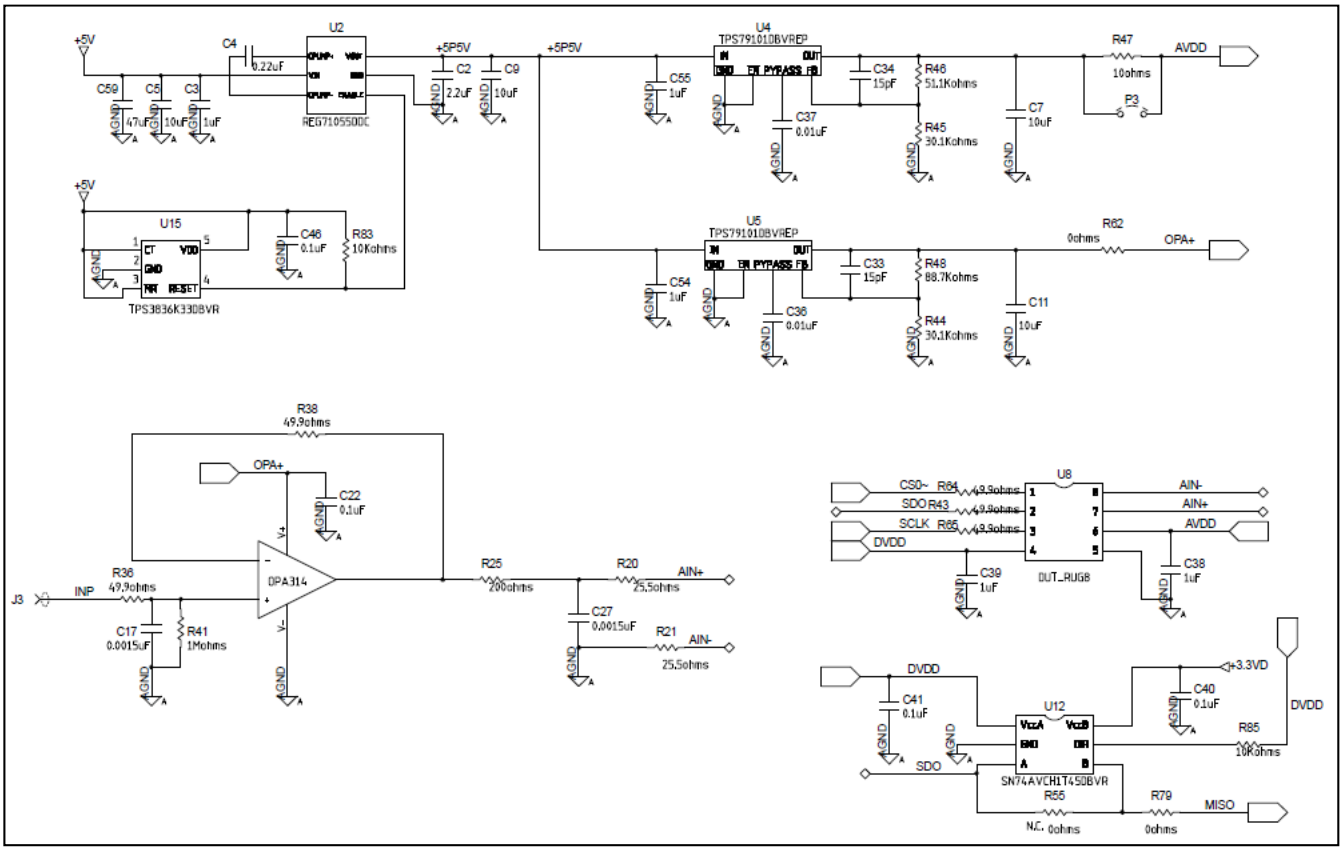

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	Qty	Reference Designators	Description	Vendor	Part Number
1	6	C1,C22,C23,C40,C41,C46	Capacitor, 0402, Ceramic, 0.1uF, 10V, 10%, X5R	MURATA	GRM155R61A104KA01
2	1	C2	Capacitor, 0402, Ceramic, 2.2uF, 4V, 20%, X5R	MURATA	GRM155R60G225ME15D
3	6	C3,C38,C39,C54,C55,C58	Capacitor, 0402, Ceramic, 1uF,10V,10%,X7S	TDK	C1005X7S1A105K050BC
4	1	C4	Capacitor, 0402, Ceramic, 0.22uF,16V,10%	MURATA	GRM155R71C224KA12
5	5	C5,C7,C9,C11,C52	Capacitor, 0603, Ceramic, 10uF,6.3V,20%,X5R	MURATA	GRM188R60J106ME47D
6	2	C17,C27	Capacitor, 0402, Ceramic, 1500pF,50V,5%,C0G/NP0	KEMET	C0402C152J5GACTU
7	2	C33,C34	Capacitor, 0402, Ceramic, 15pF,50V,1%,C0G/NP0	MURATA	GRM1555C1H150FZ01D
8	2	C36,C37	Capacitor, 0402, Ceramic, 10000pF,50V,10%,X7R	MURATA	GRM155R71H103KA88D
9	3	C56,C57,C59	Capacitor, 0805, Ceramic, 47uF,6.3V,20%,X5R	MURATA	GRM21BR60J476ME15L
10	1	J1	Connector, Female, 50P, .8mmLS	SAMTEC	ERF8-025-01-L-D-RA-L-TR
11	1	J2	Connector, Micro SD Card,SMD,8P	TYCO ELECTRONIC	5025700893
12	1	J3	SMA Jack, Edge Mount, Gold, Straight, 50Ω	SAMTEC	SMA-J-P-X-ST-EM1
13	1	L1	Inductor, 2P, Power Choke 1uH, 30%	WURTH	744029001
14	2	P2,P4	UNINSTALLED	UNINSTALLED	HEADER,MALE,2PIN,.100CC
15	1	P3	Header W/Shunt,2P,100LS TL=.125	TYCO ELECTRONICS	103321-2
16	9	R1,R2,R3,R4,R5,R6,R7,R83,R85	Resistor, 0402,10.0K,1%,1/16W	PANASONIC	ERJ-2RKF1002X
17	6	R12,R22,R62,R79,R80,R81	Resistor, 0402,0Ω,1/16W, Zero Jumper	VENKEL	CR0402-16W-000T
18	2	R13,R14	Resistor, 0402, Thick Film,5%,1/16W,1.5K	PANASONIC	ERJ-2GEJ152
19	3	R20,R21,R25	Resistor, 0402,25.5Ω,1%,1/16W	PANASONIC	ERJ-2RKF25R5X
20	5	R36,R38,R43,R64,R65	Resistor, 0402,49.9Ω,1/16W, 1%, 100ppm	VISHAY	CRCW040249R9F100
21	1	R41	Resistor, 0402, Thick Film,5%,1/16W,1.0M	PANASONIC	ERJ-2GEJ105
22	3	R44,R45,R71	Resistor, 0402, Thick Film,30.1KΩ,1%,1/10W	PANASONIC	ERJ-2RKF3012X
23	1	R46	Resistor, 0402,51.1K,1%,1/16W	PANASONIC	ERJ-2RKF5112X
24	3	R47,R75,R76	Resistor, 0402,10Ω,1/16W,1%,100ppm	VISHAY	CRCW040210R0F100
25	1	R48	Resistor, 0402, 88.7KΩ, 1/16W, 1%	VISHAY	CRCW040288K7FKED
26	5	R50,R54,R55,R78,R82	UNINSTALLED	UNINSTALLED	CRCW04020000Z0ED
27	1	R66	Resistor, 0402, Thick Film,5%,1/16W,5.6K	PANASONIC	ERJ-2GEJ562
28	1	R74	Resistor, 0402,16.2KΩ,1/16W,1%	VISHAY	CRCW040216K2FKED
29	1	R77	Resistor, 0402,3.3K,1/16W,1%,100ppm	VISHAY	CRCW04023301F100
30	1	R84	UNINSTALLED	UNINSTALLED	CRCW04021002F100

31	5	TP1,TP2,TP3,TP4,TP5	Test point, Thru-hole, Miniature, 0.1LS,120TL, Black	KEYSTONE ELECTRONICS	5001
32	1	U1	IC, I2C Compatible, Serial EEPROM, TSSOP-8	ATMEL	AT24C02C-XHM
33	1	U2	IC,60mA, 5.0V, Buck/Boost Charge Pump, TSOT23-6	TEXAS INSTRUMENTS	REG71055DDC
34	2	U4,U5	1.2~5.5V,Ultralow Noise High PSRR Fast RF 100mA LDO Linear Regulator	TEXAS INSTRUMENTS	TPS79101DBVREP
35	1	U8	IC, Low-power SAR ADC, RUG-8, 1.5x1.5x0.4mm	TEXAS INSTRUMENTS	ADS7042RUG
36	1	U10	Ultralow Power Regulator	TEXAS INSTRUMENTS	OPA835IDBV
37	1	U12	Single-Bit Dual-supply Bus Transceiver	TEXAS INSTRUMENTS	SN74AVCH1T45DBVR
38	1	U13	IC, 1.2A, High Efficient Step Down Converter with Snooze Mode, SON-8	TEXAS INSTRUMENTS	TPS62080DSG
39	1	U15	IC, Nanopower Supervisory Circuits, SOT23-5	TEXAS INSTRUMENTS	TPS3836K33DBVR
40	1	for J2	SanDisk microSDHC™ Card - 4GB	SANDISK	SDSDQ-004G-A11M

Figure A-2: Bill of Materials

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