

# PCA9536 Remote 4-Bit I<sup>2</sup>C and SMBus I/O Expander with Configuration Registers

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Low standby current consumption of 1  $\mu$ A Max
- I<sup>2</sup>C to parallel port expander
- Operating power-supply voltage range of 2.3 V to 5.5 V
- 5-V Tolerant I/O ports
- 400-kHz fast I<sup>2</sup>C bus
- Input and output configuration register
- Polarity inversion register
- Internal power-on reset
- No glitch on power up
- Power-up with all channels configured as inputs
- Noise filter on SCL/SDA inputs
- Latched outputs with high-current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD Protection exceeds JESD 22
  - 2000-V Human-body model (A114-A)
  - 200-V Machine model (A115-A)
  - 1000-V Charged-device model (C101)

## 2 Applications

- Personal electronics
  - [Wearables](#)
  - [Mobile phones](#)
  - [Gaming consoles](#)
- Servers
- Routers

## 3 Description

This 4-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.3-V to 5.5-V  $V_{CC}$  operation. It provides general-purpose remote I/O expansion for most microcontroller families through the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

The PCA9536 features 4-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs with a weak pullup to  $V_{CC}$ . However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. If no signals are applied externally to the PCA9536, the voltage level is 1, or high, because of the internal pullup resistors. The data for each input or output is stored in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register and the system controller reads all registers.

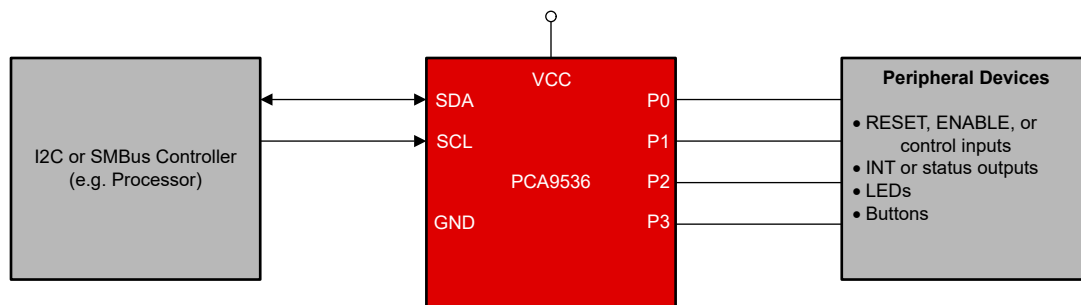
The system controller resets the PCA9536 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine.

The device outputs (latched) have high-current drive capability for directly driving LEDs, but has low current consumption.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
PCA9536	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



**Simplified Schematic**



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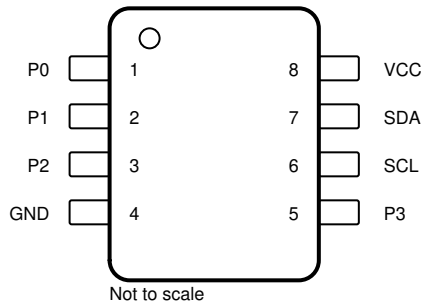
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## 4 Revision History

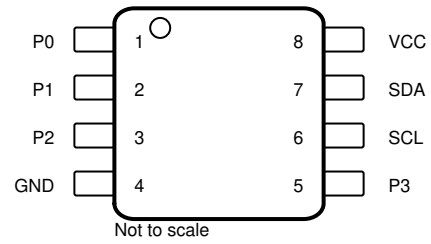
Changes from Revision G (June 2014) to Revision H (March 2022)	Page
• Changed all instances of legacy terminology to controller and target where I2C is mentioned.....	1
• Deleted the DSBGA (YZP) package information.....	1
• Added the <i>Simplified Schematic</i> to the front page.....	1
• Removed packaging information from the <i>Absolute Maximum Ratings</i> table.....	4
• Added T <sub>stg</sub> to the <i>Absolute Maximum Ratings</i> table.....	4
• Added the <i>Thermal Information</i> table.....	4
• Deleted V <sub>POR</sub> from the <i>Electrical Characteristics</i> .....	5
• Added V <sub>PORR</sub> and V <sub>PORF</sub> to the <i>Electrical Characteristics</i> .....	5
• Changed the I <sub>CC</sub> stand by mode current max values for 5.5 V from 1 to 1.8 μA; 3.6 V from 0.9 to 1.2 μA; and 2.7 V from 0.8 to 1 μA in the <i>Electrical Characteristics</i> .....	5
• Changed the t <sub>vd(data)</sub> and t <sub>vd(ack)</sub> MAX values from: 1 μs to: 3.45 μs in the <i>Standard Mode</i> timing.....	6
• Changed the t <sub>icr</sub> , t <sub>ocf</sub> , and t <sub>ocf</sub> MIN values in the <i>Fast Mode</i> timing.....	6
• Added the Overview section.....	12
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## 5 Pin Configuration and Functions



**Figure 5-1. D Package, 8-Pin SOIC (Top View)**



**Figure 5-2. DGK Package, 8-Pin VSSOP, Top View**

**Table 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	P0	I/O	P-port input-output. Push-pull design structure
2	P1	I/O	P-port input-output. Push-pull design structure
3	P2	I/O	P-port input-output. Push-pull design structure
4	GND	—	Ground
5	P3	I/O	P-port input-output. Push-pull design structure
6	SCL	I/O	Serial clock bus. Connect to $V_{CC}$ through a pullup resistor
7	SDA	I/O	Serial data bus. Connect to $V_{CC}$ through a pullup resistor
8	$V_{CC}$	—	Supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) See <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	-0.5	6	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6	V	
V <sub>O</sub>	Output voltage <sup>(2)</sup>	-0.5	6	V	
I <sub>IK</sub>	Input clamp current		V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current		V <sub>O</sub> < 0	-20	mA
I <sub>IOK</sub>	Input/output clamp current		V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>OL</sub>	Continuous output low current		V <sub>O</sub> = 0 to V <sub>CC</sub>	50	mA
I <sub>OH</sub>	Continuous output high current		V <sub>O</sub> = 0 to V <sub>CC</sub>	-50	mA
I <sub>CC</sub>	Continuous current through GND			-200	mA
	Continuous current through V <sub>CC</sub>			160	
T <sub>stg</sub>	Storage temperature	-65	150		°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		MIN	MAX	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		
		0	2000	
		0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA		V
		0.7 × V <sub>CC</sub>	5.5	
V <sub>IL</sub>	Low-level input voltage	P3–P0		V
		2	5.5	
V <sub>IL</sub>	Low-level input voltage	SCL, SDA		V
		-0.5	0.3 × V <sub>CC</sub>	
V <sub>IL</sub>	Low-level input voltage	P3–P0		V
		-0.5	0.8	
I <sub>OH</sub>	High-level output current		-10	mA
I <sub>OL</sub>	Low-level output current		25	mA
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	DGK (VSSOP)	UNIT
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	141.9	183.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	82.6	76.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	85.3	104.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	32.3	18.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	84.6	103.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	2.3 V to 5.5 V	-1.2		0	V	
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			1.2	1.6	V	
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		0.75	1		V	
V <sub>OH</sub>	P-port high-level output voltage <sup>(2)</sup>	I <sub>OH</sub> = -8 mA	2.3 V	1.8			V	
			3 V	2.6				
			4.5 V	4.1				
			4.75 V	4.1				
		I <sub>OH</sub> = -10 mA	2.3 V	1.7				
			3 V	2.5				
			4.5 V	4				
			4.75 V	4				
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	2.3 V to 5.5 V	3	10		mA	
	P-port <sup>(3)</sup>	V <sub>OL</sub> = 0.5 V	2.3 V	8	10			
			3 V	8	14			
			4.5 V	8	17			
			4.75 V	8	32			
		V <sub>OL</sub> = 0.7 V	2.3 V	10	13			
			3 V	10	19			
			4.5 V	10	24			
			4.75 V	10	44			
	I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		±1		μA
	I <sub>IH</sub>	P-port	V <sub>I</sub> = V <sub>CC</sub>	2.3 V to 5.5 V		1		μA
	I <sub>IL</sub>	P-port	V <sub>I</sub> = GND	2.3 V to 5.5 V		-100		μA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scl</sub> = 400 kHz	5.5 V		73	150	μA	
			3.6 V		9	50		
			2.7 V		7	30		
		V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scl</sub> = 100 kHz	5.5 V		14	25		
			3.6 V		9	20		
			2.7 V		6	15		
	Standby mode	V <sub>I</sub> = GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>scl</sub> = 0 kHz	5.5 V		225	350		
			3.6 V		175	250		
			2.7 V		125	200		
		V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scl</sub> = 0 kHz	5.5 V		0.25	1.8		
			3.6 V		0.2	1.2		
			2.7 V		0.1	1		
ΔI <sub>CC</sub>	Additional current in standby mode	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.3 V to 5.5 V			0.35	mA	
		Every LED I/O at V <sub>I</sub> = 4.3 V, f <sub>scl</sub> = 0 kHz	5.5 V			0.4		
C <sub>I</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		4	5	pF	
C <sub>IO</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.3 V to 5.5 V		5	6.5	pF	
	P-port				7.5	9.5		

(1) All typical values are at nominal supply voltage (2.5-, 3.3-, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) The total current sourced by all I/Os must be limited to 85 mA.

(3) Each I/O must be limited externally to a maximum of 25 mA, and the P-port (P3–P0) must be limited to a maximum current of 100 mA.

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

		MIN	MAX	UNIT
<b>Standard Mode</b>				
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time, 10-pF to 400-pF bus		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between Stop and Start	4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C Start or repeated Start condition setup time	4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C Start or repeated Start condition hold time	4		μs
t <sub>sps</sub>	I <sup>2</sup> C Stop condition setup time	4		μs
t <sub>vd(data)</sub>	Valid data time, SCL low to SDA output valid		3.45	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		3.45	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF
<b>Fast Mode</b>				
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time	20 <sup>(1)</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time	20x(V <sub>dd</sub> /5.5V) <sup>(1)</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time, 10-pF to 400-pF bus	20x(V <sub>dd</sub> /5.5V) <sup>(1)</sup>	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between Stop and Start	1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C Start or repeated Start condition setup time	0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C Start or repeated Start condition hold time	0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C Stop condition setup time	0.6		μs
t <sub>vd(data)</sub>	Valid data time, SCL low to SDA output valid		0.9	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		0.9	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

(1) C<sub>b</sub> = Total capacitive load of one bus in pF

## 6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
<b>STANDARD MODE and FAST MODE</b>					
t <sub>pv</sub>	Output data valid	SCL		200	ns
t <sub>ps</sub>	Input data setup time	P-port	100		ns
t <sub>ph</sub>	Input data hold time	P-port	1		μs

## 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

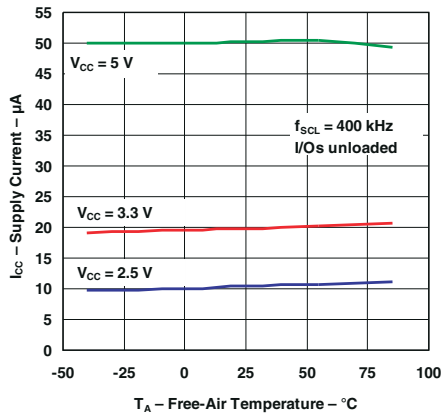


Figure 6-1. Supply Current vs Temperature

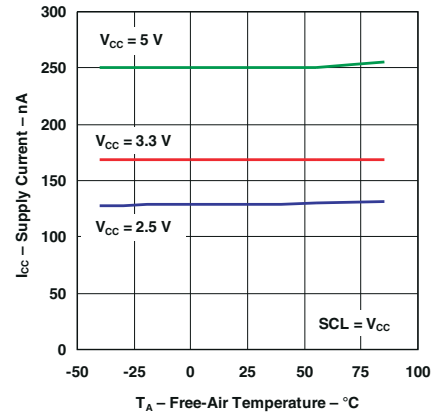


Figure 6-2. Quiescent Supply Current vs Temperature

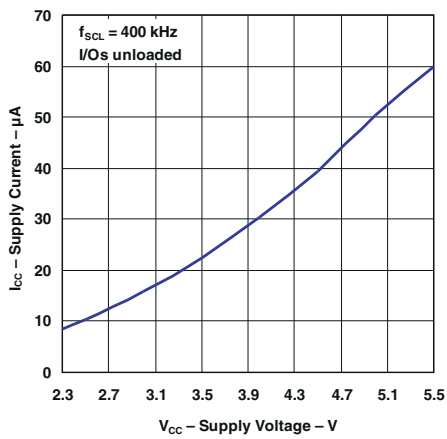


Figure 6-3. Supply Current vs Supply Voltage

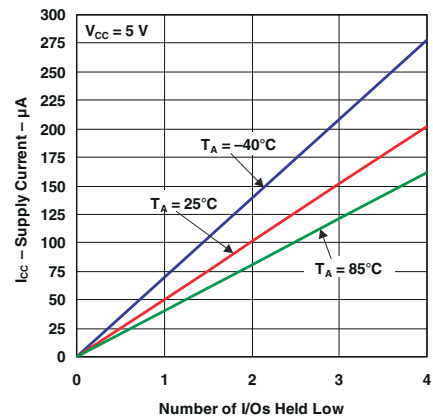


Figure 6-4. Supply Current vs Number of I/Os Held Low

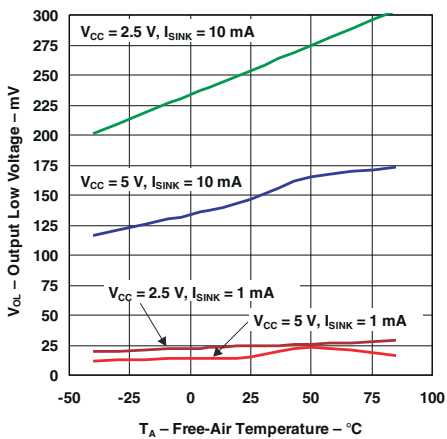


Figure 6-5. I/O Output Low Voltage vs Temperature

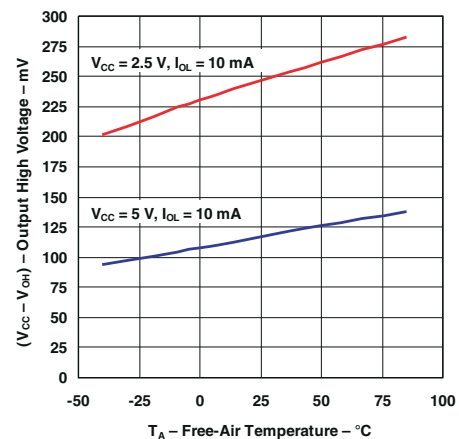


Figure 6-6. I/O Output High Voltage vs Temperature

## 6.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

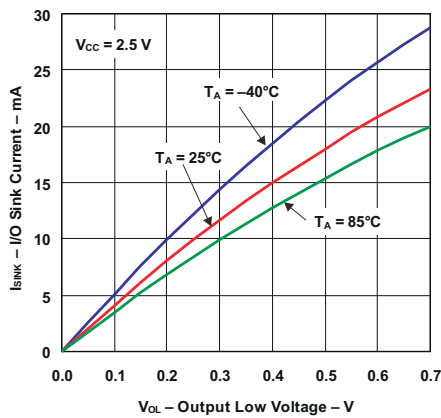


Figure 6-7. I/O Sink Current vs Output Low Voltage

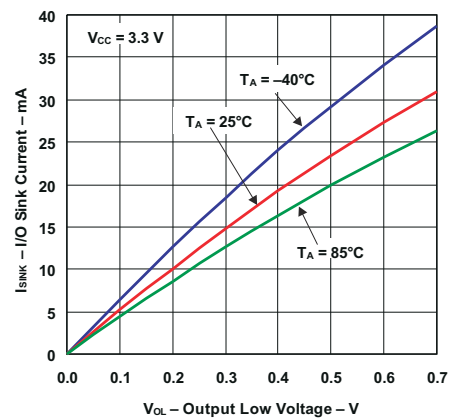


Figure 6-8. I/O Sink Current vs Output Low Voltage

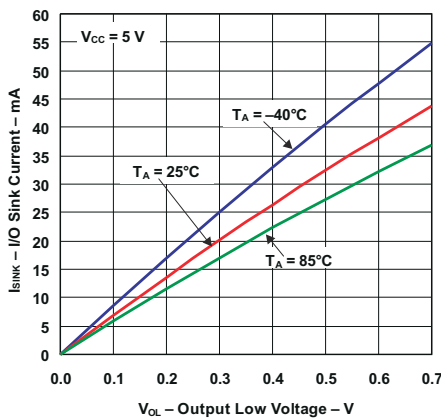


Figure 6-9. I/O Sink Current vs Output Low Voltage

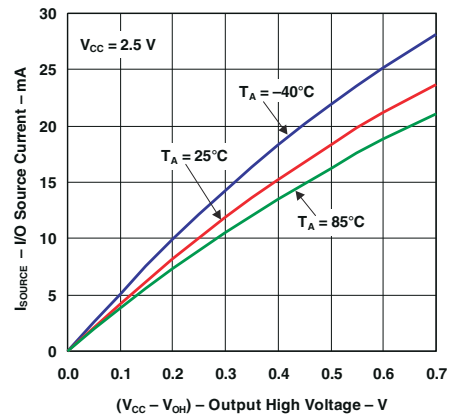


Figure 6-10. I/O Source Current vs Output High Voltage

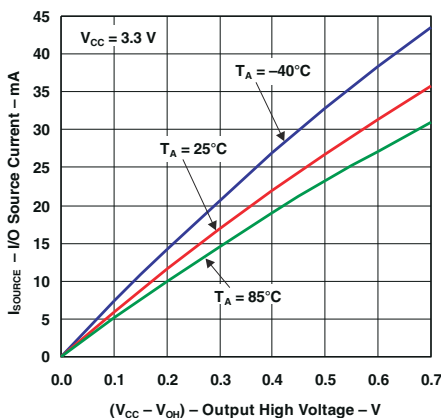


Figure 6-11. I/O Source Current vs Output High Voltage

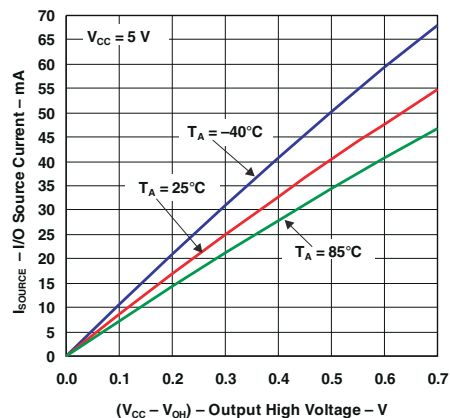


Figure 6-12. I/O Source Current vs Output High Voltage



## 6.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

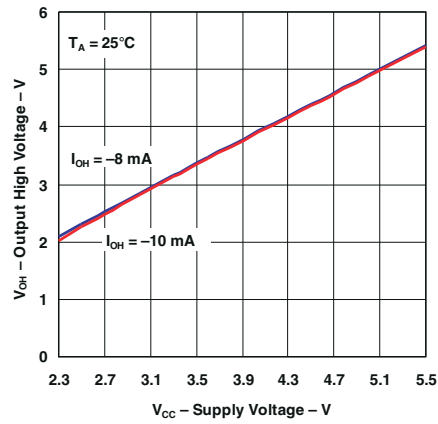
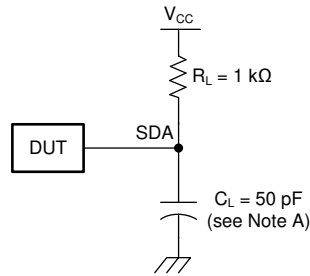
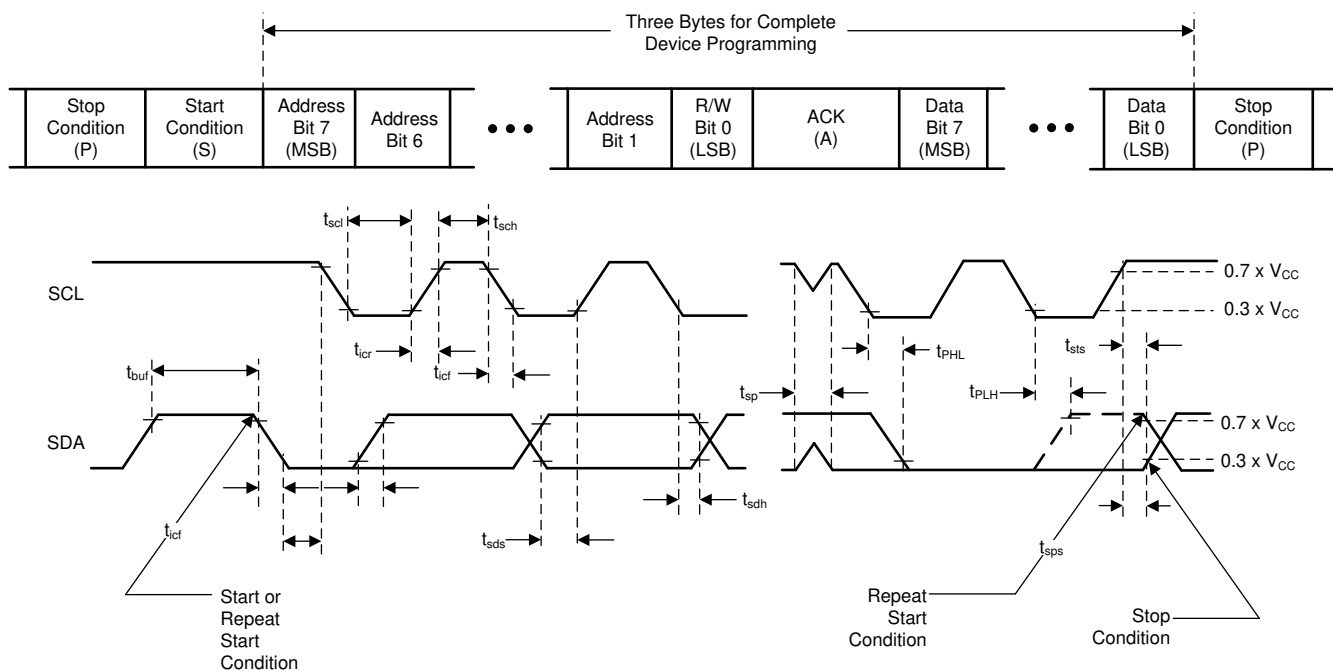


Figure 6-13. Output High Voltage vs Supply Voltage

## 7 Parameter Measurement Information



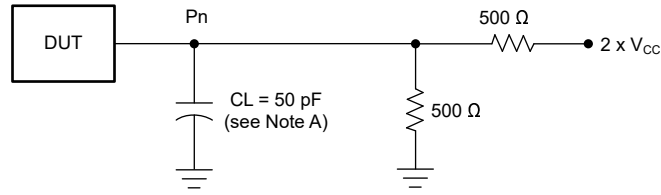
SDA LOAD CONFIGURATION



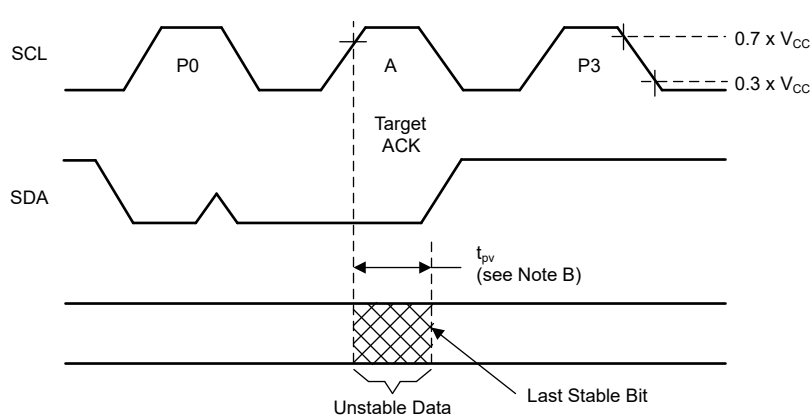
VOLTAGE WAVEFORMS

- A.  $C_L$  include probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

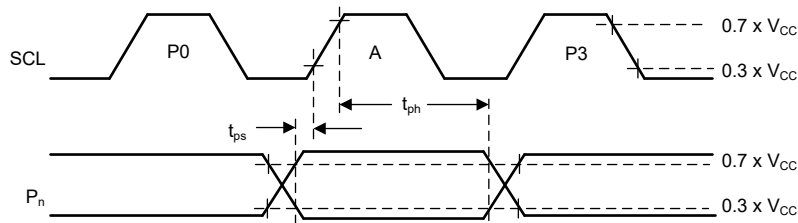
Figure 7-1. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms



P-PORT LOAD CONFIGURATION



WRITE MODE (R/W = 0)



READ MODE (R/W = 1)

- A. C<sub>L</sub> include probe and jig capacitance.
- B. t<sub>pv</sub> is measured from 0.7 x V<sub>CC</sub> on SCL to 50% I/O (P<sub>n</sub>) output.
- C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 7-2. P-Port Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The PCA9536 device is a 4-bit I/O expander for the I<sup>2</sup>C bus and is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation. It provides general-purpose remote I/O expansion for most microcontroller families through the I<sup>2</sup>C interface.

The PCA9536 consists of a configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system controller enables the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register and the system controller reads all registers.

The device outputs (latched) have high-current drive capability for directly driving LEDs.

### 8.2 Functional Block Diagram

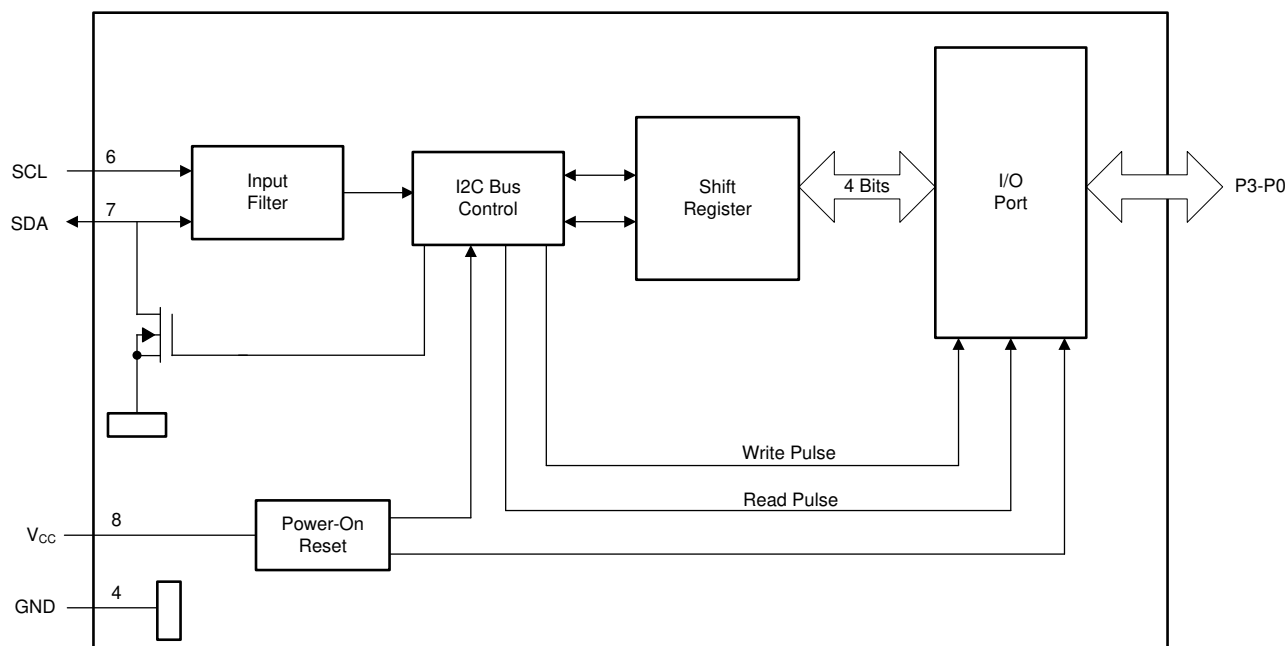
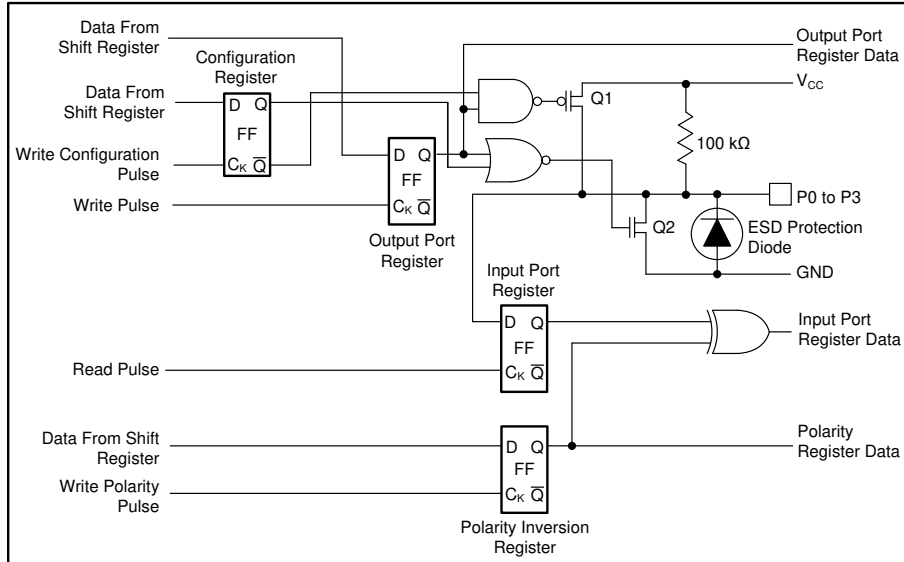


Figure 8-1. Logic Diagram



**Figure 8-2. Simplified Schematic Of P0 To P3**

## 8.3 Feature Description

### 8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in [Figure 8-2](#)) are off, creating a high-impedance input with a weak pullup (100 kΩ typical) to  $V_{CC}$ . The input voltage may be raised above  $V_{CC}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{CC}$  or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the PCA9536 in a reset condition until  $V_{CC}$  has reached  $V_{POR}$ . At that time, the reset condition is released and the PCA9536 registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that,  $V_{CC}$  must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the [Section 10.1](#) section.

### 8.4.2 Powered-Up

When power has been applied to  $V_{CC}$  above  $V_{PORR}$ , and the POR has taken place, the device is in a functioning mode. In this state, the device is ready to accept any incoming I<sup>2</sup>C requests and monitors for changes on the input ports.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a controller sending a Start condition, which is a high-to-low transition on the SDA input and output while the SCL input is high (see [Figure 8-3](#)). After the Start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W).

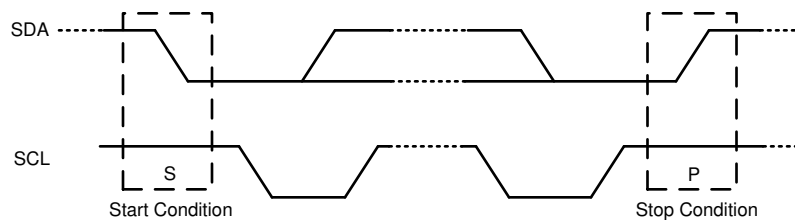
After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input and output during the high of the ACK-related clock pulse.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 8-4).

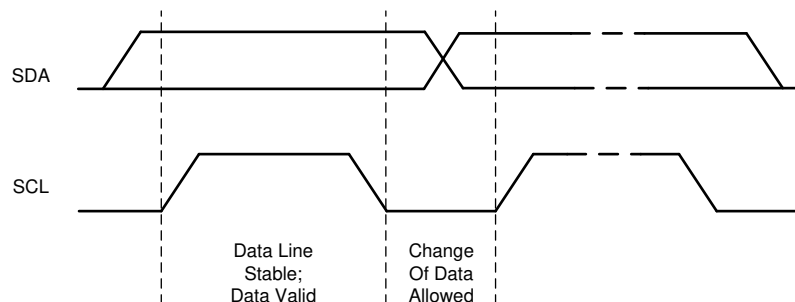
A Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high, is sent by the controller (see Figure 8-3).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 8-5). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. This is done by the controller receiver, by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.



**Figure 8-3. Definition of Start and Stop Conditions**



**Figure 8-4. Bit Transfer**

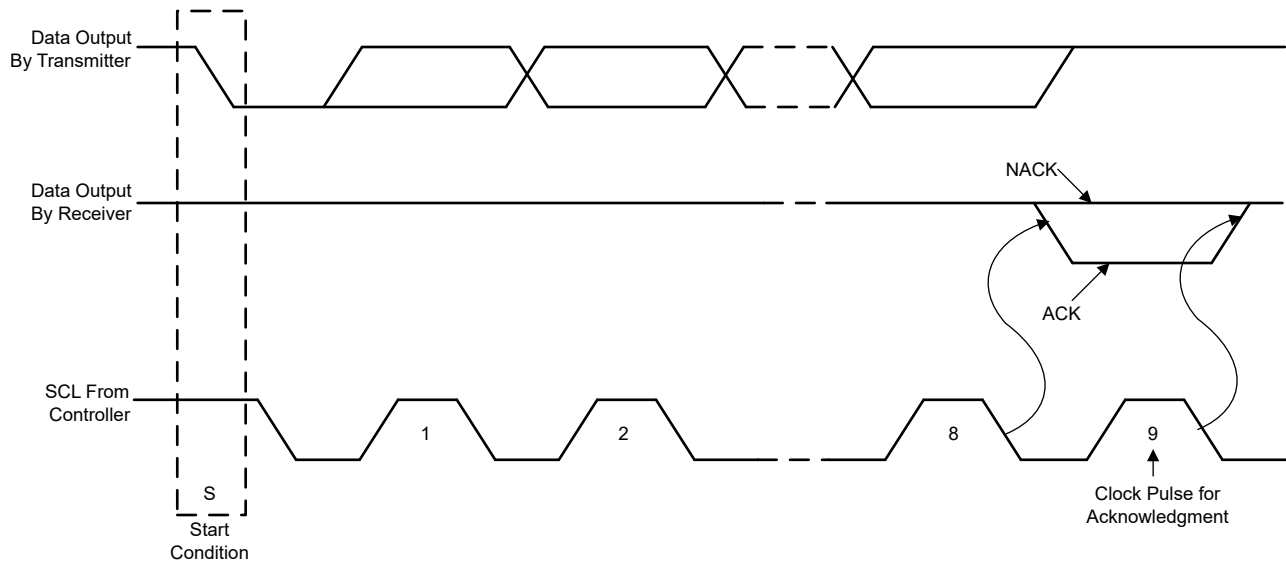


Figure 8-5. Acknowledgment on the I<sup>2</sup>C Bus

## 8.6 Register Maps

Table 8-1 shows the PCA9536 interface definition.

Table 8-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C target address	H	L	L	L	L	L	H	R/ W
Px I/O data bus	Does not affect operation of the PCA9536				P3	P2	P1	P0
	P7	P6	P5	P4				

### 8.6.1 Device Address

Figure 8-6 shows the address byte of the PCA9536.

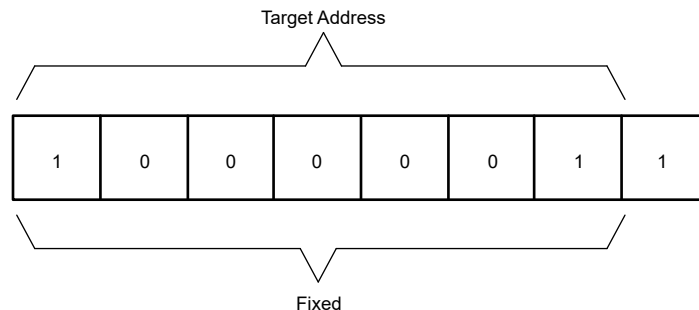


Figure 8-6. PCA9536 Address

The target address equates to 65 (decimal) and 41 (hexadecimal).

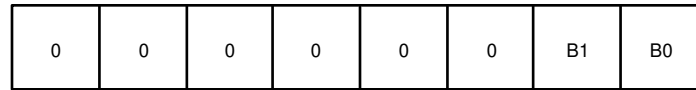
The last bit of the target address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

### 8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the PCA9536. Two bits of this data byte state the operation (read or write) and the internal register (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the addressed register is continuously accessed by reads until a new command byte is sent.

Figure 8-7 shows the PCA9536 control register bits and Table 8-2 shows the command byte.



**Figure 8-7. Control Register Bits**

**Table 8-2. Command Byte**

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0×00	Input Port	Read byte	1111 XXXX
0	1	0×01	Output Port	Read/write byte	1111 1111
1	0	0×02	Polarity Inversion	Read/write byte	0000 0000
1	1	0×03	Configuration	Read/write byte	1111 1111

### 8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. See Table 8-3.

Before a read operation, a write transmission is sent with the command byte to instruct the I<sup>2</sup>C device that the Input Port register will be accessed next.

**Table 8-3. Register 0 (Input Port Register)**

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	Not Used							
DEFAULT	1	1	1	1	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. The bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See Table 8-4.

**Table 8-4. Register 1 (Output Port Register)**

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained. See Table 8-5.

**Table 8-5. Register 2 (Polarity Inversion Register)**

BIT	N7	N6	N5	N4	N3	N2	N1	N0
	Not Used							
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See Table 8-6.



**Table 8-6. Register 3 (Configuration Register)**

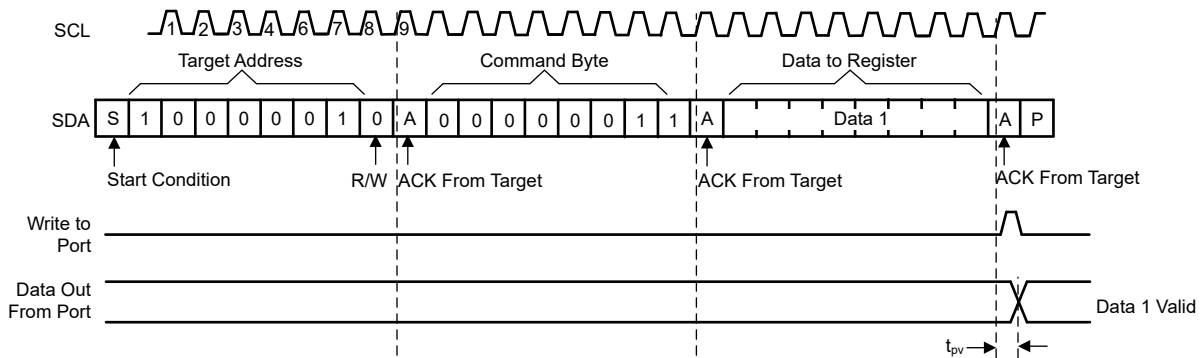
BIT	C7	C6	C5	C4	C3	C2	C1	C0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

### 8.6.4 Bus Transactions

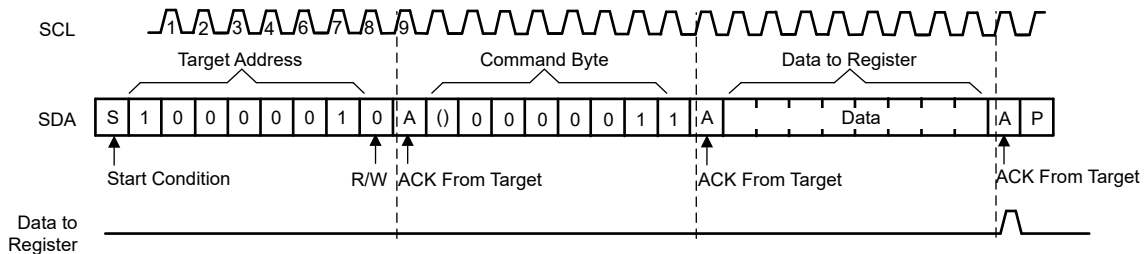
Data is exchanged between the controller and PCA9536 through write and read commands.

#### 8.6.4.1 Writes

Data is transmitted to the PCA9536 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 8-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see Figure 8-8 and Figure 8-9).



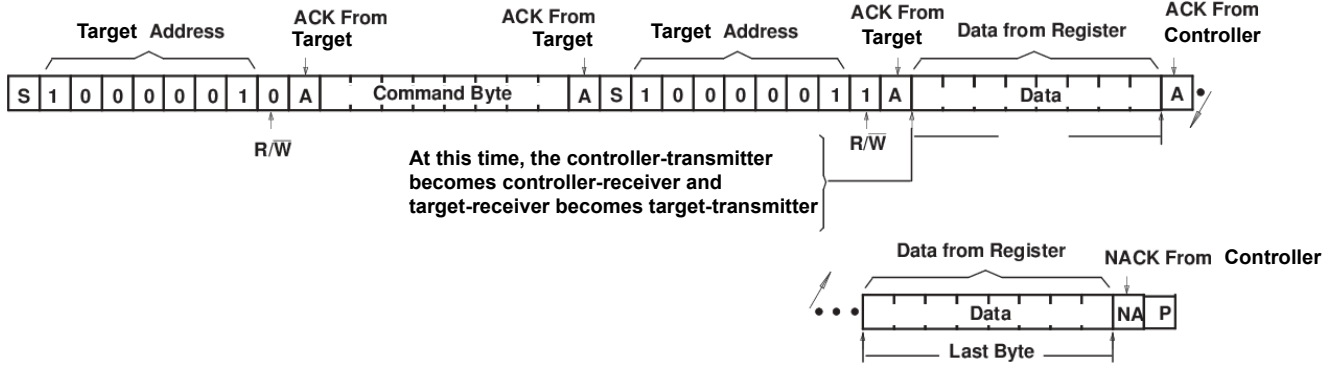
**Figure 8-8. Write to Output Port Register**



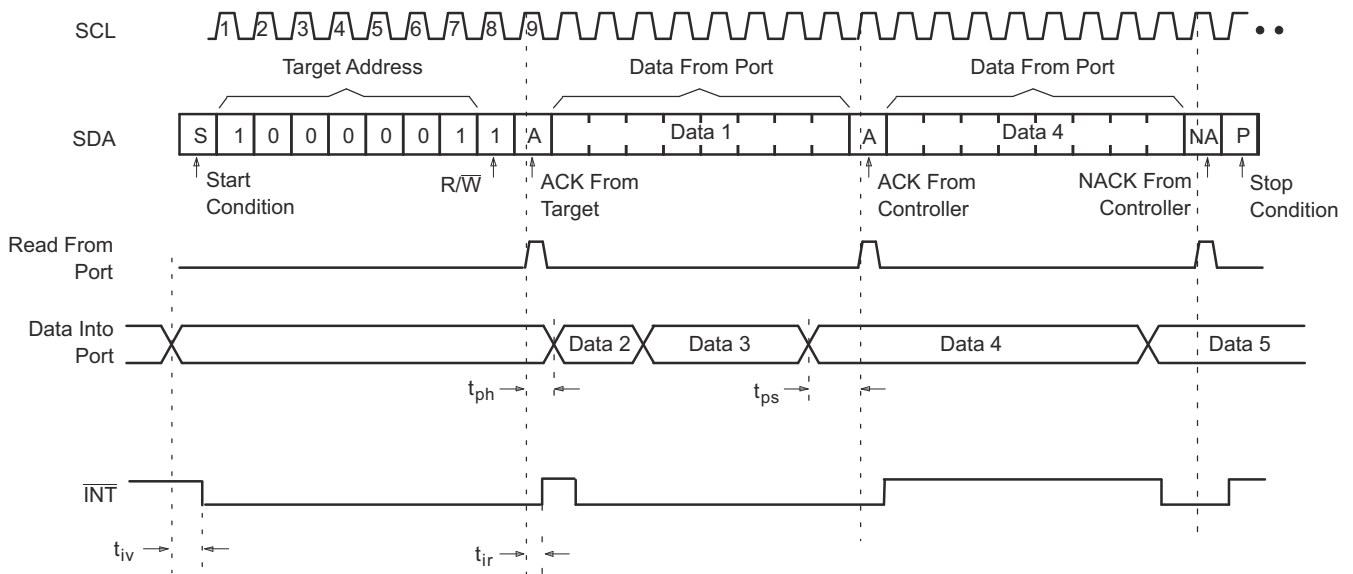
**Figure 8-9. Write to Configuration or Polarity Inversion Registers**

#### 8.6.4.2 Reads

The bus controller first must send the PCA9536 address with the LSB set to a logic 0 (see Figure 8-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9536 (see Figure 8-10 and Figure 8-11). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data.



**Figure 8-10. Read From Register**



- A. This figure assumes that the command byte previously has been programmed with 00h.
- B. Transfer of data can be stopped at any moment by a Stop condition.
- C. This figure eliminates the command byte transfer, a restart, and the target address call between the initial target address call and actual data transfer from the P-port (see [Figure 8-10](#)).

**Figure 8-11. Read Input Port Register**

## 9 Application Information Disclaimer

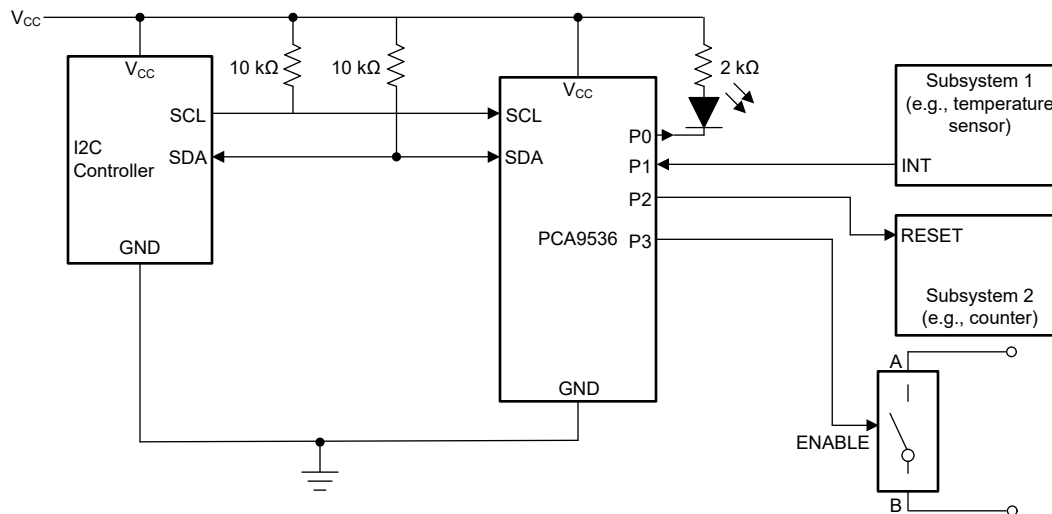
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

### 9.2 Typical Application

Figure 9-1 shows an application in which the PCA9536 can be used.



- A. Device address is 10000001.
- B. P0, P2, and P3 are configured as outputs.
- C. P1 is configured as an input.

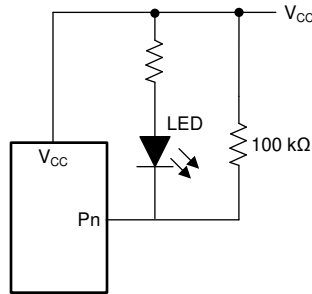
Figure 9-1. Typical Application

#### 9.2.1 Design Requirements

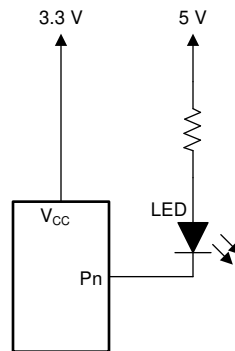
##### 9.2.1.1 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, they are normally connected to  $V_{CC}$  through a resistor as shown in Figure 9-1. The LED acts as a diode so, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The supply current,  $I_{CC}$ , increases as  $V_{IN}$  becomes lower than  $V_{CC}$  and is specified as  $\Delta I_{CC}$  in *Electrical Characteristics*.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{CC}$  when the LED is off. Figure 9-2 shows a high-value resistor in parallel with the LED. Figure 9-3 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevent additional supply-current consumption when the LED is off.



**Figure 9-2. High-Value Resistor in Parallel with the LED**



**Figure 9-3. Device Supplied by a Lower Voltage**

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_P$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in [Equation 1](#):

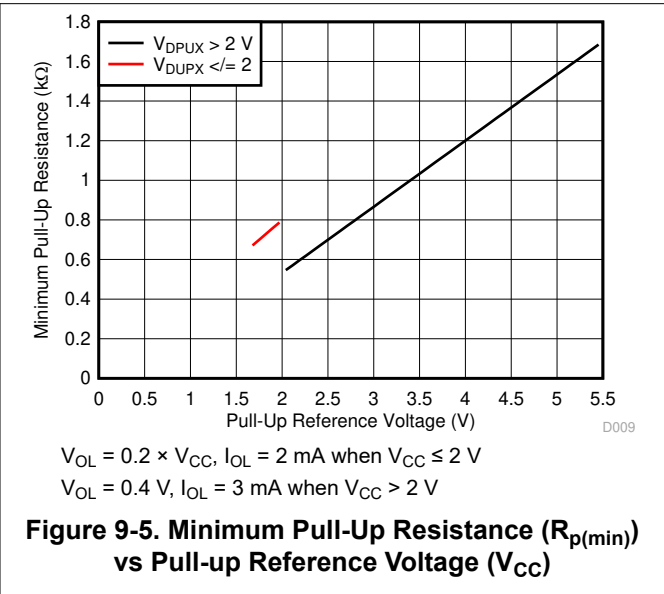
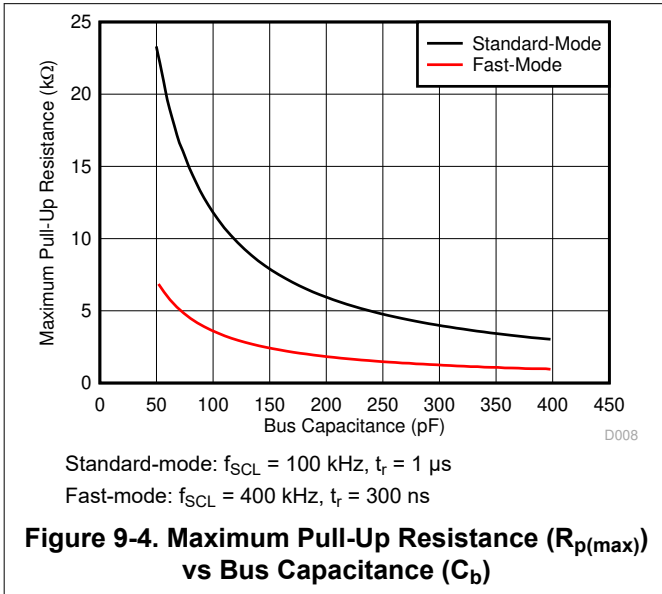
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in [Equation 2](#):

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9536,  $C_i$  for SCL or  $C_{io}$  for SDA, the capacitance of wires, connections or traces, and the capacitance of additional targets on the bus.

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

### 10.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed in [Figure 10-1](#).

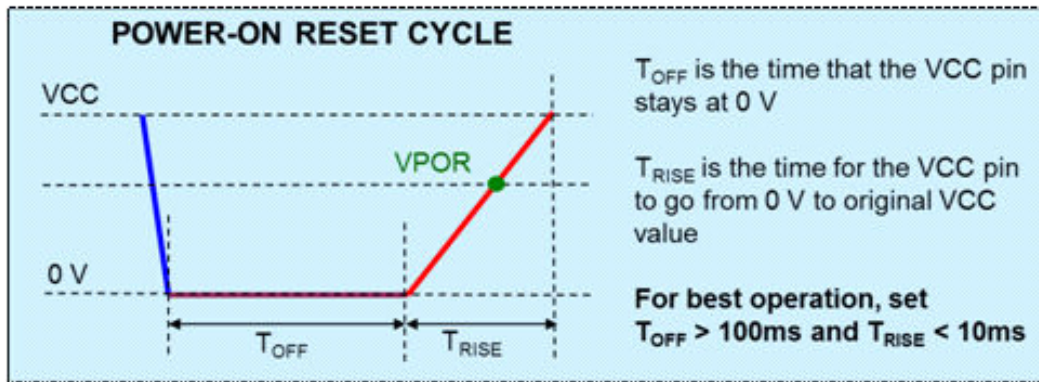


Figure 10-1. Power-On Reset Cycle

### 10.2 System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

## 11 Layout

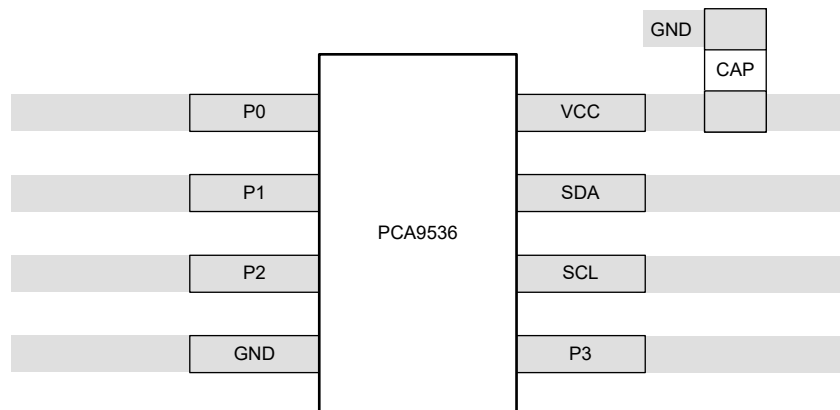
### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCA9536, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the PCA9536 as possible.

For the layout example provided, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated.

### 11.2 Layout Example



**Figure 11-1. Layout Example (DGK)**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [I2C Bus Pull-Up Resistor Calculation](#)
- [Maximum Clock Frequency of I2C Bus Using Repeaters](#)
- [Introduction to Logic](#)
- [Understanding the I2C Bus](#)
- [Choosing the Correct I2C Device for New Designs](#)

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 12.4 Trademarks

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#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9536D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	
PCA9536DG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	
PCA9536DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(7CF, 7CL)	Samples
PCA9536DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7CF, 7CL)	Samples
PCA9536DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples
PCA9536DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9536DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9536DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9536DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9536DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
PCA9536DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
PCA9536DR	SOIC	D	8	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCA9536D	D	SOIC	8	75	506.6	8	3940	4.32
PCA9536D	D	SOIC	8	75	507	8	3940	4.32
PCA9536DG4	D	SOIC	8	75	506.6	8	3940	4.32
PCA9536DG4	D	SOIC	8	75	507	8	3940	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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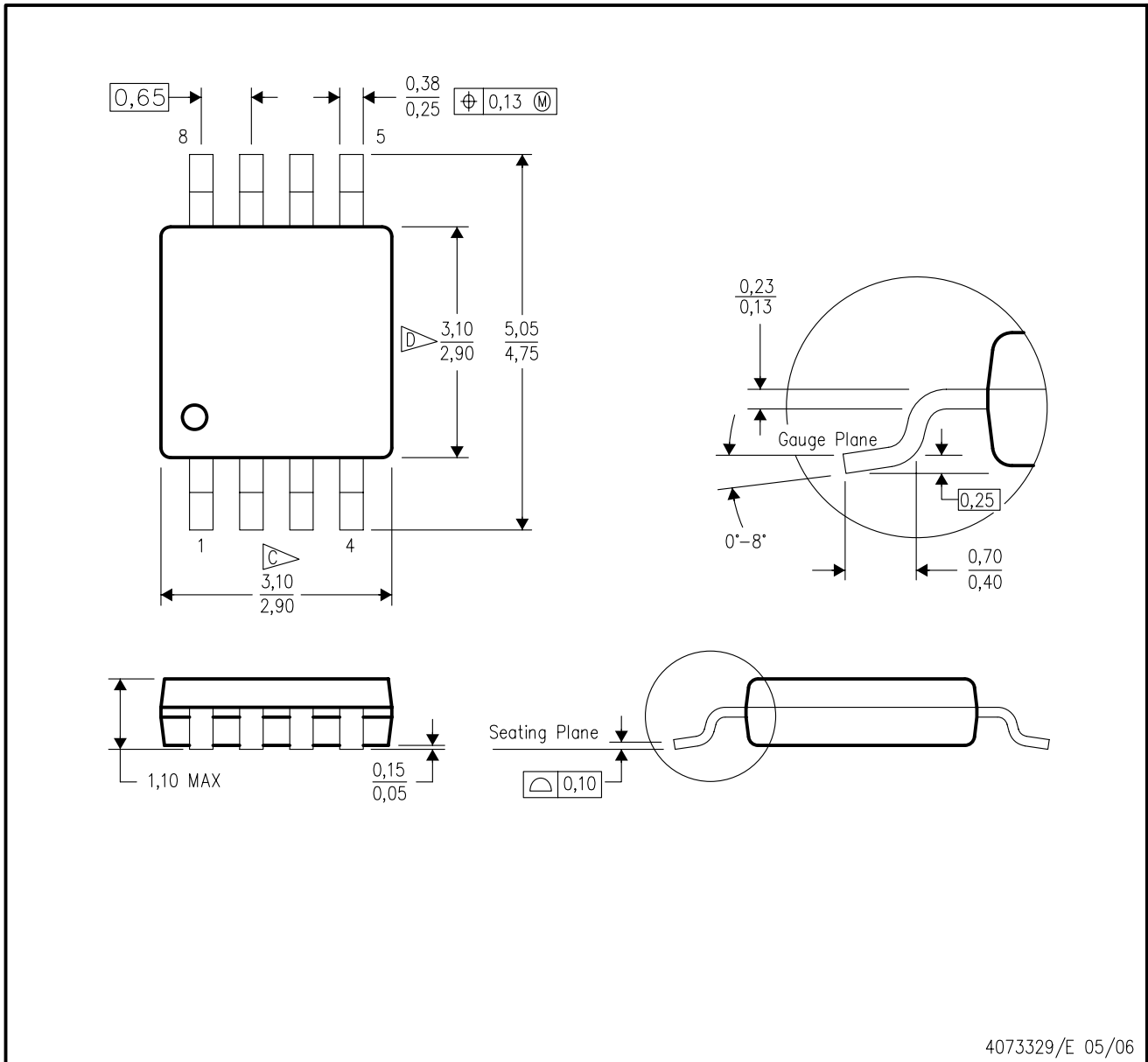
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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