Application Report
SBAA351–June 2020

PCM6xx0-Q1 Fault Diagnostic Features

ABSTRACT

The PCM6xx0-Q1 family of devices (PCM6260-Q1, PCM6240-Q1, PCM6360-Q1) are multi-channel, high-performance, analog-to-digital converters intended for automotive audio applications. This application note details the integrated fault diagnostic features of this family of devices and how they can be used for robust system design.

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Trademarks

1 Introduction

Automotive systems have to be designed to operate in a wide range of harsh environments. As greater amounts of electronics are integrated into automotive systems, the system complexity and potential for faults also increase. For automotive audio systems that rely on algorithms like beamforming, active noise cancellation, or speech recognition, multiple microphones are typically used. These algorithms depend on reliable data from microphones, and if one or more microphones in the system fail, the processing of unreliable data can lead to erroneous calculations. In these automotive audio applications, microphones may be placed in remote locations far away from the PCB, such as in a wheel well, close to the engine or at different positions in the passenger cabin, thus requiring a wire harness to interface with the rest of the electronics. Although extreme care is taken to prevent failure, over time these harnesses may degrade and result in faulty microphone connections. Texas Instruments' new family of automotive audio data converters helps to address this challenge by providing integrated diagnostic monitoring features that determine when an input fault condition has occurred. With this information, the system can decide how to respond and adjust its algorithms to handle the error.

2 Diagnostic Monitoring Architecture

Typical automotive audio applications favor the use of electret condenser microphones (ECM) for their ease of mounting, interfacing, pickup directionality, moisture, and dust protection. These ECM microphones operate between 2–10 V and thus can have large voltage swings. For accurate fault detection it is required for the ADC to interface directly with the microphone pins. For an AC-coupled application, this would require doubling the number of input pins as shown in Figure 1.

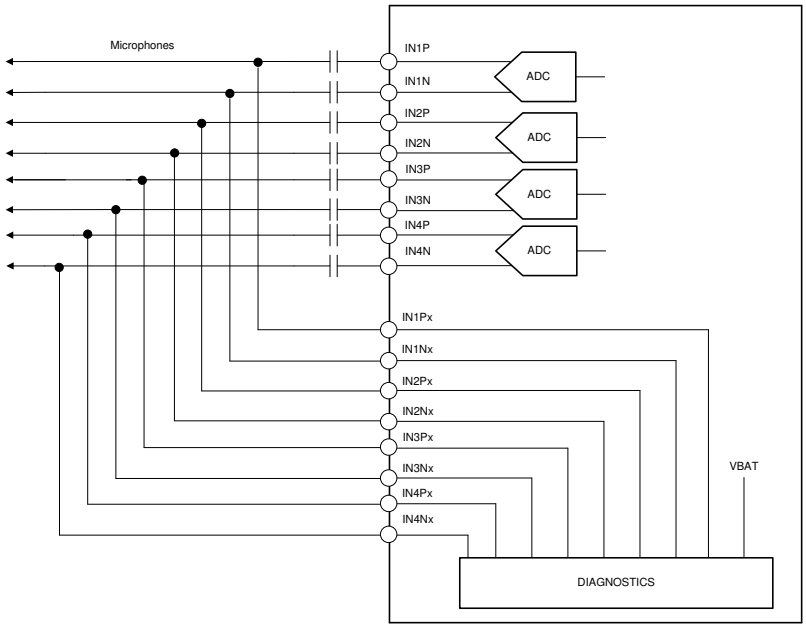


Figure 1. AC-Coupled Diagnostics

This also requires that the inputs utilize high voltage transistors to handle the 10-V_{RMS} swing directly. Together, these two factors lead to a very large solution size. For these reasons, the PCM6xx0-Q1 family uses DC coupling for fault diagnostics with an attenuator on the front end of the signal chain to allow the input and the diagnostics to operate using a single pin. This is shown in Figure 2.

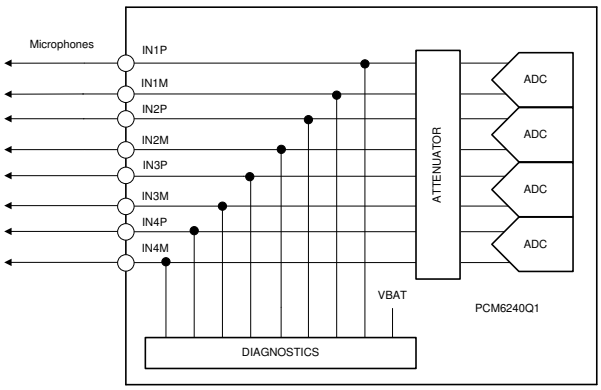


Figure 2. DC-Coupled Diagnostics

However, there are some benefits to AC coupling too: higher input swing, greater flexibility in setting the gain of an analog PGA since the PGA has no DC offset from the microphone, and more filtering flexibility. For applications that desire AC coupling with fault diagnostics, it is possible to use some channels for the AC-coupled analog inputs, and dedicate other channels to the DC-coupled diagnostics. Figure 3 shows an example using a 4-channel device. Channels 1 and 2 are AC-coupled mic inputs and channels 3 and 4 are used for mic diagnostics. In this configuration, faults on channels 1 and 2 will be recorded in the diagnostic registers for channels 3 and 4, respectively. It is not necessary to enable the primary ADCs for channels 3 and 4, only the diagnostics.

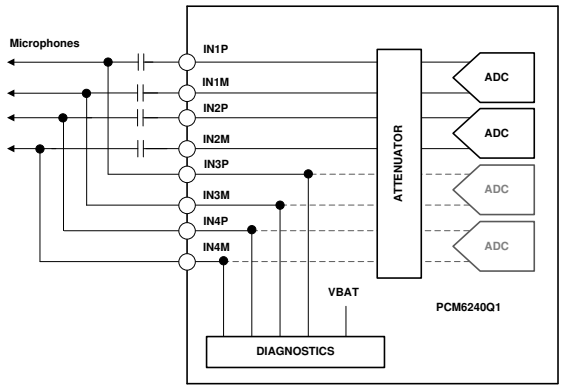


Figure 3. AC-Coupled Inputs With DC Diagnostics

Figure 4 depicts the PCM6xx0 diagnostic monitoring architecture for the fault monitoring signal chain.

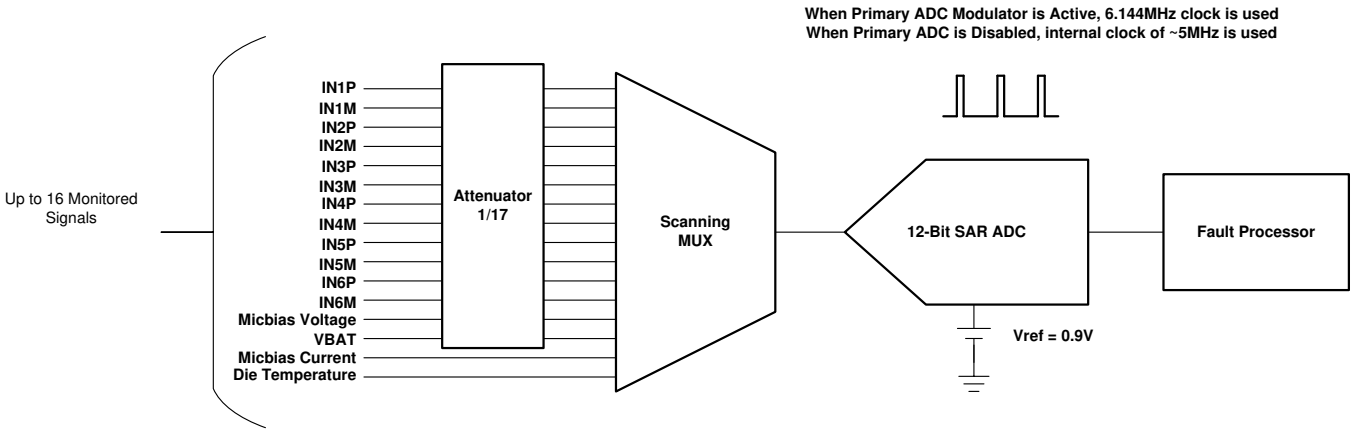


Figure 4. Diagnostic Monitoring Architecture

All of the input pins are monitored (12 pins for the 6-channel devices) along with the MICBIAS pin voltage, MICBIAS load current, VBAT_IN input, and internal die temperature. The input pins first pass through an attenuator, which scales the signal down by a factor of 17 before reaching the scanning MUX. The MUX automatically scans all inputs for which diagnostics have been enabled in a consecutive manner. The scan rate can be adjusted in the DIAG_CFG0 register (Page 0, address 0x64). Once an input is selected by the scanning MUX, 8 consecutive samples of the input are collected and averaged to improve the noise performance. Note, disabling the diagnostics for a channel is independent of disabling the channel, and diagnostics can still be read on inactive channels.

3 Monitored Faults

3.1 Microphone Faults

There are a number of ways that the microphone or the connections to it could fail depending on the system implementation. For example, microphones themselves may degrade after prolonged exposure to extreme environmental conditions, excessive vibration or impact. Over time, cables connecting microphones to other electronics in the system may also degrade due to vibration, shock, or extreme temperature.

For robust detection the PCM6xx0-Q1 monitors the input pins for the following faults:

- Inputs shorted to ground
- Inputs shorted to MICBIAS
- Input open circuit
- Input pins shorted together
- Input overvoltage detection
- Inputs shorted to VBAT

The input diagnostics of the PCM6xx0-Q1 family were designed with microphone inputs in mind, but could also be used for DC-coupled line inputs.

Most faults support user-programmable thresholds for detection. Faults can be individually enabled or disabled or masked. In order for the diagnostic monitoring to be active, MICBIAS must be turned on even if it is not actively used since a number of faults rely on its measured value. It is recommended to wait at least 10 ms after powering up MICBIAS and the PLL before enabling fault diagnostic monitoring. Each fault reading is trimmed to 8-bit accuracy, to match the threshold programmability. Once detected, faults can be set to trigger interrupts on the GPIO pins or force channels to power down automatically. Each of the above faults is described in the next sections:

3.1.1 Inputs Shorted to Ground

This fault triggers if the measured input pin voltage is less than the programmed threshold. This fault is programmable from 0 V–900 mV with a programming resolution of 60 mV.

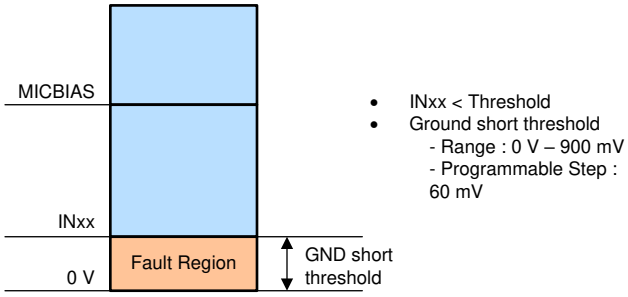


Figure 5. Input Short to GND Conditions

3.1.2 Inputs Shorted to MICBIAS

This fault is triggered if the difference between the voltage measured at the input pin and that measured at the micbias pin is greater than 0 V and less than the programmed threshold. This fault is programmable from 0 V–450 mV with a programming step size of 30 mV. This fault uses the actual voltage measured at the MICBIAS pin, which may differ slightly from the programmed MICBIAS value.

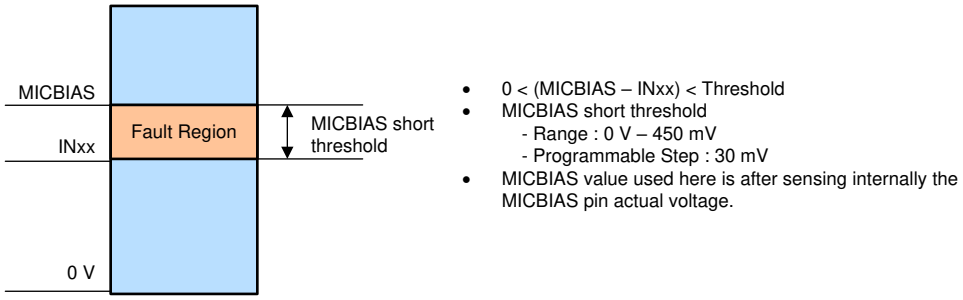


Figure 6. Input Short to MICBIAS Conditions

3.1.3 Input Open Circuit

This fault triggers when an open circuit condition is detected, which occurs from a combination of the previous two faults. This fault can trigger in two ways:

1. INxP is shorted to MICBIAS AND INxM is shorted to GND, or
2. INxP is shorted GND and INxM is shorted to MICBIAS

This fault relies on the thresholds programmed for these two respective faults.

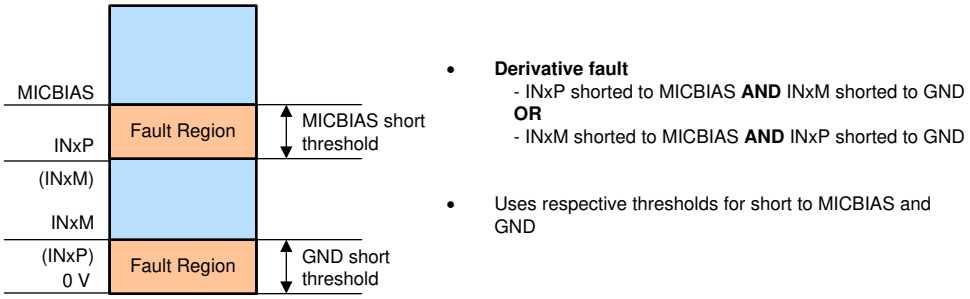


Figure 7. Input Open Circuit Conditions

3.1.4 Input Pins Shorted Together

This fault triggers when the absolute value of the difference between the input pins falls under the programmed threshold. It is programmable from 0 V–450 mV in steps of 30 mV. In a typical DC-coupled application, there will be a differential DC offset between the input pins from the microphone. If for some reason in the application this DC differential is kept below the programmed threshold this fault may trigger inadvertently.

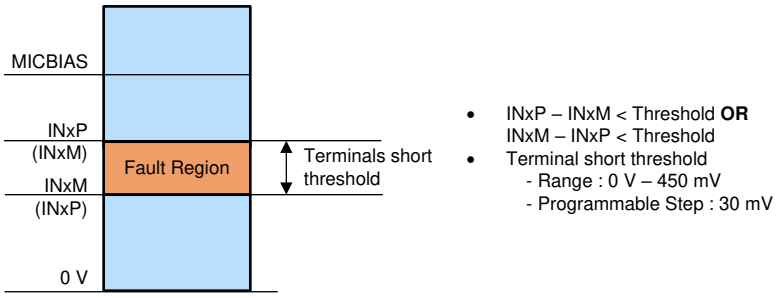
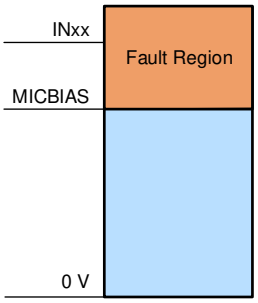


Figure 8. Inputs Shorted Conditions

3.1.5 Input Overvoltage Detection

This fault triggers when the measured input pin voltage is greater than the measured MICBIAS voltage. This threshold is not user programmable.

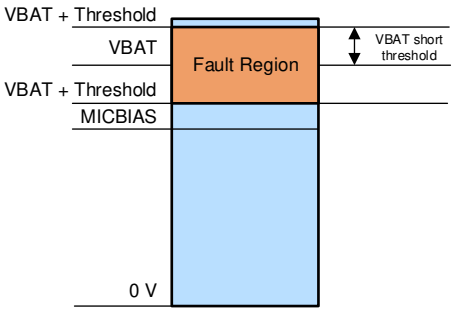


- INxx > MICBIAS
- No Programmable Threshold
- MICBIAS value used here is after sensing internally the MICBIAS pin actual voltage.

Figure 9. Input Overvoltage Conditions

3.1.6 Inputs Shorted to VBAT

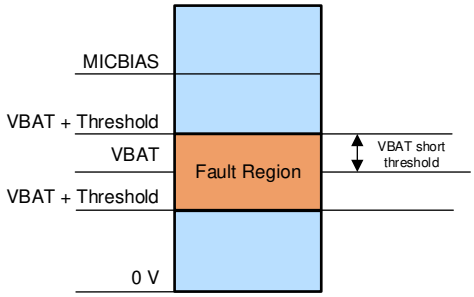
This fault triggers when the absolute value of the difference between the voltage applied to the VBAT pin and the input pin is less than the programmed threshold. The programmable range is 0 V–450 mV in steps of 30 mV.



- |VBAT – INxx| < Threshold
- VBAT short threshold
  - Range : 0 V – 450 mV
  - Programmable Step : 30 mV
- MICBIAS value used here is after sensing internally the MICBIAS pin actual voltage.
- Max readable voltage is ~11.7 V therefore VBAT and/or INxx pins voltage above this will be detected as short.

Figure 10. Input Short to VBAT Conditions When VBAT > MICBIAS

In most automotive applications, the battery voltage is not expected to dip below MICBIAS, which has a maximum programmable value of 9 V. As long as VBAT is greater than MICBIAS, then a short to VBAT fault will also produce an overvoltage fault. In rare cases it may be possible that VBAT is less than MICBIAS. This might occur if the battery is heavily loaded or a voltage divider is used prior to VBAT_IN. In these cases it is possible that the fault can falsely trigger based on the signal level on the INxx pin. To avoid or minimize false detections, it is recommended to use the debounce and averaging features described in Section 6.3. The debounce for this specific condition can be programmed independently from the other faults, or detection of this fault can be disabled altogether.



- VBAT < MICBIAS **AND**
- |VBAT – INxx| < Threshold
- VBAT short threshold
  - - Range : 0 V – 450 mV
  - - Programmable Step : 30 mV
- MICBIAS value used here is after sensing internally the MICBIAS pin actual voltage

Figure 11. Input Short to VBAT Conditions When VBAT < MICBIAS

3.2 Other Faults

3.2.1 MICBIAS Overvoltage

If the MICBIAS pin gets pulled to a voltage higher than what is set in the BIAS_CFG register (P0_R58), then a MICBIAS overvoltage fault will trigger. This may occur for instance if MICBIAS is shorted to VBAT. When this fault is triggered the device sets the overvoltage status flag in the INT_LTCH3 (P0_R55_D5) and INT_LIVE registers. The threshold for overvoltage detection can be adjusted in the MBIAS_OV_CFG register (P1_R85).

3.2.1.1 MBIAS_OV_CFG Register (page = 0x01, address = 0x55) [reset = 40h]

This register is the MICBIAS overvoltage configuration register.

Figure 12. MBIAS_OV_CFG Register

7	6	5	4	3	2	1	0
MBIAS_OV_THRES[2:0]			Reserved				
RW-2h			R-0h				

Table 1. MBIAS_OV_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MBIAS_OV_THRES[2:0]	RW	2h	MICBIAS overvoltage fault detection threshold above MICBIAS programmed voltage. 0d = No threshold over programmed voltage 1d = 10 mV (typ) threshold over programmed voltage 2d = 40 mV (typ) threshold over programmed voltage (default) 3d to 6d = Threshold value is set as per configuration with step size of 30mV (typ) 7d = 190 mV (typ) threshold over programmed voltage (default)
4-0	Reserved	R	0h	Reserved

3.2.2 MICBIAS Overcurrent

The MICBIAS pin has an integrated overcurrent protection circuit that protects the device from damage due to excessive current draw. The MICBIAS pin is specified up to 80-mA continuous current draw. Though the exact current that triggers an overcurrent protection fault will vary device-to-device, the minimum threshold that it may trigger at is 85 mA. Once the overcurrent protection has been triggered, the device sets the overcurrent status flag in the INT_LTCH0 (P0_R44_D4 bit) register and limits the output current of the MICBIAS pin.

3.2.3 MICBIAS Load Current

Separate from the overcurrent protection, an internal current sensor monitors the loading on the MICBIAS pin of the device. This can be programmed to trigger a fault if the current exceeds the maximum programmed value or falls under the minimum expected load. Note that the programmed threshold is only used for fault detection and does not limit the current supplied by the MICBIAS pin. The high and low current thresholds can be programmed from 0 mA to 99.9 mA with a resolution of 0.54 mA. These are programmed in MBDIAG_CFG0 (Page 0, address 0x38) and MBDIAG_CFG1 (Page 0, address 0x39). Since the device is only specified up to 80 mA, it is not recommended to set the high load current threshold greater than 80 mA.

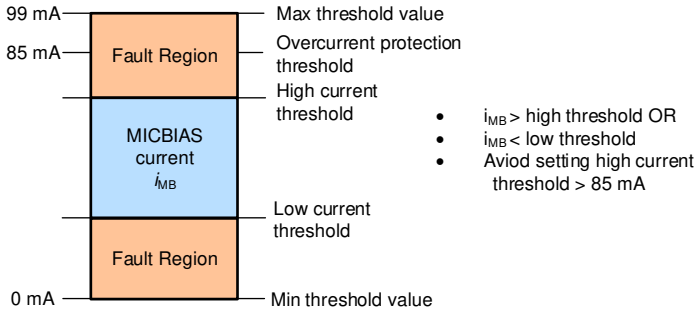


Figure 13. MICBIAS Load Current Conditions

3.2.3.1 MBDIAG_CFG0 Register (page = 0x00, address = 0x38) [reset = BAh]

This register is the MICBIAS diagnostic configuration register 0.

Figure 14. MBDIAG_CFG0 Register

7	6	5	4	3	2	1	0
MBIAS_HIGH_CURR_THRS[7:0]							
RW-BAh							

Table 2. MBDIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_HIGH_CURR_THRS[7:0]	RW	BAh	Threshold for MICBIAS high load current fault diagnostic. 0d to 56d = Reserved 57d = High load current threshold is set as 0 mA (typ) 58d = High load current threshold is set as 0.54 mA (typ) 59d = High load current threshold is set as 1.08 mA (typ) 60d to 185d = High load current threshold is set as per configuration 186d = High load current threshold is set as 69.66 mA (typ) 187d to 241d = High load current threshold is set as per configuration 242d = High load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved

3.2.3.2 MBDIAG_CFG1 Register (page = 0x00, address = 0x39) [reset = 4Bh]

This register is the MICBIAS diagnostic configuration register 1.

Figure 15. MBDIAG_CFG1 Register

7	6	5	4	3	2	1	0
MBIAS_LOW_CURR_THRS[7:0]							
RW-4Bh							

Table 3. MBDIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_LOW_CURR_THRS[7:0]	RW	4Bh	Threshold for MICBIAS low load current fault diagnostic. 0d to 56d = Reserved 57d = Low load current threshold is set as 0 mA (typ) 58d = Low load current threshold is set as 0.54 mA (typ) 59d = Low load current threshold is set as 1.08 mA (typ) 60d to 74d = Low load current threshold is set as per configuration 75d = Low load current threshold is set as 9.72 mA (typ) 76d to 241d = Low load current threshold is set as per configuration 242d = Low load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved

3.2.4 Overtemperature Fault

An overtemperature protection circuit monitors the die temperature and sets the status flag in the INT_LTCH0 (P0_R44_D5) register whenever the die junction temperature exceeds the supported level. The exact level at which this fault triggers will vary device-to-device, but will not occur within the specified operating range and is intended to protect the IC from damage.

4 Enabling Diagnostics and Programming Thresholds

The primary diagnostic configuration registers are registers 100 through 104. These registers control which channels will be scanned for faults and the thresholds for each of the faults. The first of these registers, DIAG_CFG0 (P0_R100), allows the user to enable/disable diagnostic monitoring on each of the input channels respectively.

Bit 0 of DIAG_CFG0 controls diagnostic monitoring on AC-coupled channels. Although the microphone connectivity cannot be diagnosed when using AC coupling, this does provide pin level monitoring of the ADC to determine if any shorts have occurred at the PCB level.

Bit 1 of DIAG_CFG0 controls whether the INxM pins are monitored for single-ended input channels. This may be useful in pseudo-differential input configurations where INxM is held at a constant voltage but is not grounded. It also can be used if the ground connection is located away from the board or for detecting a loss of ground condition.

4.1 DIAG_CFG0 Register (page = 0x00, address = 0x64) [reset = 0h]

This register is configuration register 0 for input fault diagnostics setting.

Figure 16. DIAG_CFG0 Register

7	6	5	4	3	2	1	0
CH1_DIAG_EN	CH2_DIAG_EN	CH3_DIAG_EN	CH4_DIAG_EN	CH5_DIAG_EN	CH6_DIAG_EN	INCL_SE_INM	INCL_AC_COUP
RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

Table 4. DIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_DIAG_EN	RW	0h	Channel 1 input (IN1P and IN1M) scan for diagnostics. 0b = Diagnostic disabled 1b = Diagnostic enabled
6	CH2_DIAG_EN	RW	0h	Channel 2 input (IN2P and IN2M) scan for diagnostics. 0b = Diagnostic disabled 1b = Diagnostic enabled
5	CH3_DIAG_EN	RW	0h	Channel 3 input (IN3P and IN3M) scan for diagnostics. 0b = Diagnostic disabled 1b = Diagnostic enabled
4	CH4_DIAG_EN	RW	0h	Channel 4 input (IN4P and IN4M) scan for diagnostics. 0b = Diagnostic disabled 1b = Diagnostic enabled
3	CH5_DIAG_EN	RW	0h	Channel 5-input (IN5P and IN5M) scan for diagnostics. Applicable only for PCM6x60-Q1. 0b = Diagnostic disabled 1b = Diagnostic enabled
2	CH6_DIAG_EN	RW	0h	Channel 6 input (IN6P and IN6M) scan for diagnostics. Applicable only for PCM6x60-Q1. 0b = Diagnostic disabled 1b = Diagnostic enabled
1	INCL_SE_INM	RW	0h	INxM pin diagnostics scan selection for single-ended configuration. 0b = INxM pins of single-ended channels are excluded for diagnosis 1b = INxM pins of single-ended channels are included for diagnosis
0	INCL_AC_COUP	RW	0h	AC-coupled channels pins scan selection for diagnostics. 0b = INxP and INxM pins of AC-coupled channels are excluded for diagnosis 1b = INxP and INxM pins of AC-coupled channels are included for diagnosis

With DC-coupled inputs, a broad selection of microphones to choose from, and flexibility in how those microphones may be biased, applications will differ in their expected signal levels. Threshold programmability ensures each fault can be set to a reasonable level tailored to the application. The default values for these thresholds are set to be most commonly used values.

DIAG_CFG1 allows the user to configure the thresholds used for the INxP to INxM terminal short detection and the short to VBAT_IN detection.

4.2 DIAG_CFG1 Register (page = 0x00, address = 0x65) [reset = 37h]

This register is configuration register 1 for input fault diagnostics setting.

Figure 17. DIAG_CFG1 Register

7	6	5	4	3	2	1	0
DIAG_SHT_TERM[3:0]				DIAG_SHT_VBAT_IN[3:0]			
RW-3h				RW-7h			

Table 5. DIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_TERM[3:0]	RW	3h	INxP and INxM terminal short detect threshold. 0d = INxP and INxM terminal short detect threshold value is 0 mV (typ) 1d = INxP and INxM terminal short detect threshold value is 30 mV (typ) 2d = INxP and INxM terminal short detect threshold value is 60 mV (typ) 10d to 13d = INxP and INxM terminal short detect threshold value is set as per configuration 14d = INxP and INxM terminal short detect threshold value is 420 mV (typ) 15d = INxP and INxM terminal short detect threshold value is 450 mV (typ)
3-0	DIAG_SHT_VBAT_IN[3:0]	RW	7h	Short to VBAT_IN detect threshold. 0d = Short to VBAT_IN detect threshold value is 0 mV (typ) 1d = Short to VBAT_IN detect threshold value is 30 mV (typ) 2d = Short to VBAT_IN detect threshold value is 60 mV (typ) 10d to 13d = Short to VBAT_IN detect threshold value is set as per configuration 14d = Short to VBAT_IN detect threshold value is 420 mV (typ) 15d = Short to VBAT_IN detect threshold value is 450 mV (typ)

DIAG_CFG2 similarly allows the user to configure the thresholds used for short to ground detection and short to MICBIAS.

4.3 DIAG_CFG2 Register (page = 0x00, address = 0x66) [reset = 87h]

This register is configuration register 2 for input fault diagnostics setting.

Figure 18. DIAG_CFG2 Register

7	6	5	4	3	2	1	0
DIAG_SHT_GND[3:0]				DIAG_SHT_MICBIAS[3:0]			
RW-8h				RW-7h			

Table 6. DIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_GND[3:0]	RW	8h	Short to ground detect threshold. 0d = Short to ground detect threshold value is 0 mV (typ) 1d = Short to ground detect threshold value is 60 mV (typ) 2d = Short to ground detect threshold value is 120 mV (typ) 10d to 13d = Short to ground detect threshold value is set as per configuration 14d = Short to ground detect threshold value is 840 mV (typ) 15d = Short to ground detect threshold value is 900 mV (typ)
3-0	DIAG_SHT_MICBIAS[3:0]	RW	7h	Short to MICBIAS detect threshold. 0d = Short to MICBIAS detect threshold value is 0 mV (typ) 1d = Short to MICBIAS detect threshold value is 30 mV (typ) 2d = Short to MICBIAS detect threshold value is 60 mV (typ) 10d to 13d = Short to MICBIAS detect threshold value is set as per configuration 14d = Short to MICBIAS detect threshold value is 420 mV (typ) 15d = Short to MICBIAS detect threshold value is 450 mV (typ)

DIAG_CFG3 contains advanced monitoring feature settings. Bit 0 controls threshold scaling. Setting this bit high will double the value of the configured thresholds, effectively expanding the range of a 450-mV threshold to 900 mV. This setting applies to all diagnostic thresholds. See Section 6.3.2.1 for the DIAG_CFG3 register definition.

5 Fault Diagnostic Setup Procedure

Figure 19 shows the suggested flow for setting up fault diagnostics. Each feature is described in more detail in the following sections. Some applications may not use all features or can rely on the default values in the configuration registers. At minimum, the user must power up MICBIAS and enable the channel diagnostics.

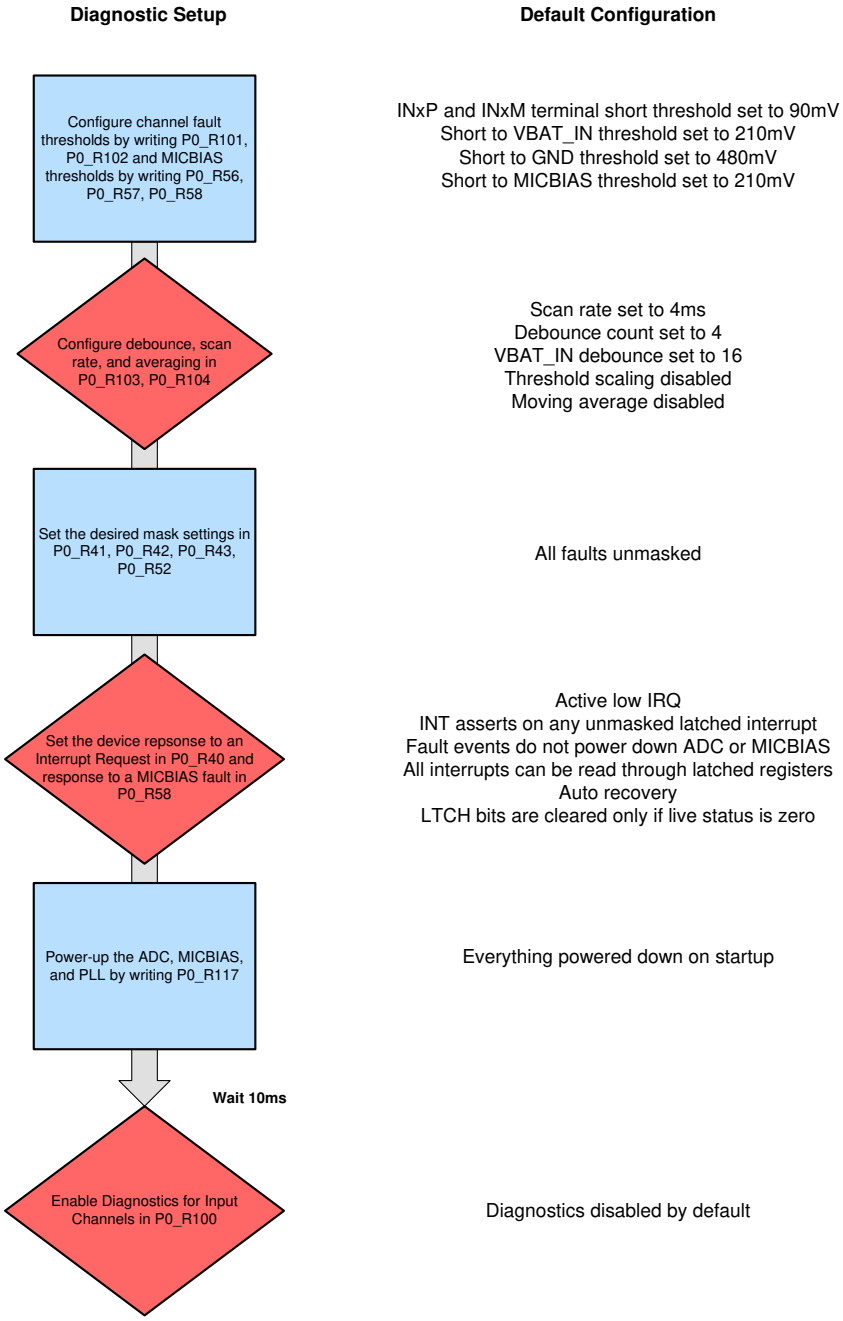


Figure 19. Diagnostic Setup Procedure

6 Fault Reporting

Faults are reported in live and latched status registers based on the settings used for fault detection.

6.1 Live Registers

The live registers, P1_R45 to P1_R55, are updated continuously with each new scan and report the most recent measurements recorded by the diagnostics processor. The CHx_LIVE register (P1_R45) contains a summary of present faults allowing the user to determine which channels have active faults.

6.1.1 CHx_LIVE Register (page = 0x01, address = 0x2D) [reset = 0h]

This register is the live Interrupt status register for channel level diagnostic summary.

Figure 20. CHx_LIVE Register

7	6	5	4	3	2	1	0
STS_CHx_LIVE[7]	STS_CHx_LIVE[6]	STS_CHx_LIVE[5]	STS_CHx_LIVE[4]	STS_CHx_LIVE[3]	STS_CHx_LIVE[2]	STS_CHx_LIVE[1]	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7. CHx_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LIVE[7]	R	0h	Status of CH1_LIVE. 0b = No faults occurred in channel 1 1b = At least a fault has occurred in channel 1
6	STS_CHx_LIVE[6]	R	0h	Status of CH2_LIVE. 0b = No faults occurred in channel 2 1b = At least a fault has occurred in channel 2
5	STS_CHx_LIVE[5]	R	0h	Status of CH3_LIVE. 0b = No faults occurred in channel 3 1b = At least a fault has occurred in channel 3
4	STS_CHx_LIVE[4]	R	0h	Status of CH4_LIVE. 0b = No faults occurred in channel 4 1b = At least a fault has occurred in channel 4
3	STS_CHx_LIVE[3]	R	0h	Status of CH5_LIVE. Applicable only for PCM6x60-Q1. 0b = No faults occurred in channel 5 1b = At least a fault has occurred in channel 5
2	STS_CHx_LIVE[2]	R	0h	Status of CH6_LIVE. Applicable only for PCM6x60-Q1. 0b = No faults occurred in channel 6 1b = At least a fault has occurred in channel 6
1	STS_CHx_LIVE[1]	R	0h	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS. 0b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in at least one channel
0	Reserved	R	0h	Reserved

The respective CH_LIVE registers (P1_R46 to P1_R51) contain the details of exactly which faults have occurred on a given channel. Section 6.1.2 shows the CH1_LIVE register for reference.

6.1.2 CH1_LIVE Register (page = 0x01, address = 0x2E) [reset = 0h]

This register is the live Interrupt status register for channel 1 fault diagnostic

Figure 21. CH1_LIVE Register

7	6	5	4	3	2	1	0
CH1_LIVE[7]	CH1_LIVE[6]	CH1_LIVE[5]	CH1_LIVE[4]	CH1_LIVE[3]	CH1_LIVE[2]	CH1_LIVE[1]	CH1_LIVE[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8. CH1_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_LIVE[7]	R	0h	Channel 1 open input fault status. 0b = No open input detected 1b = Open input detected
6	CH1_LIVE[6]	R	0h	Channel 1 input pair short fault status. 0b = No input pair short detected 1b = Input short to each other detected
5	CH1_LIVE[5]	R	0h	Channel 1 IN1P short to ground fault status. 0b = IN1P no short to ground detected 1b = IN1P short to ground detected
4	CH1_LIVE[4]	R	0h	Channel 1 IN1M short to ground fault status. 0b = IN1M no short to ground detected 1b = IN1M short to ground detected
3	CH1_LIVE[3]	R	0h	Channel 1 IN1P short to MICBIAS fault status. 0b = IN1P no short to MICBIAS detected 1b = IN1P short to MICBIAS detected
2	CH1_LIVE[2]	R	0h	Channel 1 IN1M short to MICBIAS fault status. 0b = IN1M no short to MICBIAS detected 1b = IN1M short to MICBIAS detected
1	CH1_LIVE[1]	R	0h	Channel 1 IN1P short to VBAT_IN fault status. 0b = IN1P no short to VBAT_IN detected 1b = IN1P short to VBAT_IN detected
0	CH1_LIVE[0]	R	0h	Channel 1 IN1M short to VBAT_IN fault status. 0b = IN1M no short to VBAT_IN detected 1b = IN1M short to VBAT_IN detected

In addition to the channel registers, there are also interrupt registers that contain various faults. The first of these registers, INT_LIVE0 (P1_R44), contains the self-protection fault flags as well as the ASI bus clock error and PLL lock status. The PLL lock status is not a fault, but provides a way to monitor when the state of the PLL changes. For more information on ASI bus clock errors, see the data sheet.

6.1.3 INT_LIVE0 Register (page = 0x01, address = 0x2C) [reset = 0h]

This register is the live Interrupt readback register 0.

Figure 22. INT_LIVE0 Register

7	6	5	4	3	2	1	0
INT_LIVE0[7]	INT_LIVE0[6]	INT_LIVE0[5]	INT_LIVE0[4]	Reserved	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 9. INT_LIVE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE0[7]	R	0h	Fault status for an ASI bus clock error. 0b = No fault detected 1b = Fault detected
6	INT_LIVE0[6]	R	0h	Status of PLL lock. 0b = No PLL lock detected 1b = PLL lock detected
5	INT_LIVE0[5]	R	0h	Fault status for boost or MICBIAS overtemperature. 0b = No fault detected 1b = Fault detected
4	INT_LIVE0[4]	R	0h	Fault status for boost or MICBIAS overcurrent. 0b = No fault detected 1b = Fault detected
3	Reserved	R	0h	Reserved
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

INT_LIVE1 (P1_R53) contains the overvoltage fault status for each of the INxP pins of the device. Similarly, INT_LIVE2 (P1_R54) contains the overvoltage fault status for each of the INxM pins.

6.1.4 INT_LIVE1 Register (page = 0x01, address = 0x35) [reset = 0h]

This register is the live Interrupt readback register 1.

Figure 23. INT_LIVE1 Register

7	6	5	4	3	2	1	0
INT_LIVE1[7]	INT_LIVE1[6]	INT_LIVE1[5]	INT_LIVE1[4]	INT_LIVE1[3]	INT_LIVE1[2]	Reserved	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 10. INT_LIVE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE1[7]	R	0h	Channel 1 IN1P overvoltage fault status. 0b = No IN1P overvoltage fault detected 1b = IN1P overvoltage fault has detected
6	INT_LIVE1[6]	R	0h	Channel 2 IN2P overvoltage fault status. 0b = No IN2P overvoltage fault detected 1b = IN2P overvoltage fault has detected
5	INT_LIVE1[5]	R	0h	Channel 3 IN3P overvoltage fault status. 0b = No IN3P overvoltage fault detected 1b = IN3P overvoltage fault has detected
4	INT_LIVE1[4]	R	0h	Channel 4 IN4P overvoltage fault status. 0b = No IN4P overvoltage fault detected 1b = IN4P overvoltage fault has detected
3	INT_LIVE1[3]	R	0h	Channel 5 IN5P overvoltage fault status. Applicable only for PCM6x60-Q1. 0b = No IN5P overvoltage fault detected 1b = IN5P overvoltage fault has detected
2	INT_LIVE1[2]	R	0h	Channel 6 IN6P overvoltage fault status. Applicable only for PCM6x60-Q1. 0b = No IN6P overvoltage fault detected 1b = IN6P overvoltage fault has detected
1-0	Reserved	R	0h	Reserved

The last of the interrupt fault registers, INT_LIVE3 (P1_R55), contains the MICBIAS faults that do not pertain to the device's self-protection features.

6.1.5 INT_LIVE3 Register (page = 0x01, address = 0x37) [reset = 0h]

This register is the live Interrupt readback register 3.

Figure 24. INT_LIVE3 Register

7	6	5	4	3	2	1	0
INT_LIVE3[7]	INT_LIVE3[6]	INT_LIVE3[5]	Reserved				
R-0h	R-0h	R-0h	R-0h				

Table 11. INT_LIVE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE3[7]	R	0h	Fault status for MICBIAS high current. 0b = No fault detected 1b = Fault detected
6	INT_LIVE3[6]	R	0h	Fault status for MICBIAS low current 0b = No fault detected 1b = Fault detected
5	INT_LIVE3[5]	R	0h	Fault status for MICBIAS overvoltage. 0b = No fault detected 1b = Fault detected
4-0	Reserved	R	0h	Reserved

6.2 Latched Registers

The latched registers are set up to mirror the live registers. The latched status of each diagnostic fault is reported by the channel in P0_R46 to P0_R55, and a latched summary of all channels is reported in CHx_LTCH, P0_R45. The latched registers are latched when the associated bit in the live fault registers transitions from a ‘0’ to a ‘1’ and the conditions set in the fault filtering registers have been met. A transition of any bit in the latched register from a ‘0’ to ‘1’ triggers an interrupt request. By default, latched registers are cleared after reading only if the fault is no longer present and the associated live register reports ‘0’, otherwise the register remains latched. There is an additional mode in which the latched registers will clear regardless of the status of the associated live registers. This is useful for identifying unique faults as only one interrupt will be generated per fault. This can be enabled by setting the LTCH_CLR_ON_READ bit to ‘1’ in the INT_CFG register.

6.2.1 Clearing Latched Registers

Most of the latched registers in the device are self-clearing and will reset upon reading as previously described. However, the mapping of some registers causes them to clear only when another latched register is read. Registers that exhibit this behavior include a description in the register map stating which register needs to be read in order for the bit to clear. This applies to the INxM short to VBAT_IN faults in the channel latch registers as well as the INxP and INxM overvoltage status bits in INT_LTCH1 and INT_LTCH2. It is recommended to read all latched registers any time a fault is detected to ensure all bits are cleared. To make sure no faults are missed, a recommended read sequence is provided in Section 7.3.

6.3 Fault Filtering and Response Time

The DIAG_CFG3 and DIAG_CFG4 registers contain a number of settings that allow the user to adjust the response time of the device to a fault condition. These settings control how often the MUX switches to check for faults and how long a fault must be present before being latched in the associated latched register.

6.3.1 Debounce

A debounce filter can be applied to diagnostic measurements. This debounce is analogous to the switch debounce often used in analog circuitry. Once a fault condition occurs, with debounce enabled, the device does not trigger a fault until it counts the programmed number of consecutive values within fault thresholds. The debounce can be programmed for 4, 8, or 16 counts to filter out transient events.

All faults share the same debounce setting with the exception of VBAT_IN short when VBAT_IN is less than MICBIAS. Since in this circumstance false triggers are more likely to occur under normal operating conditions, the debounce setting for this fault can be programmed independently to 8 or 16 counts. The debounce settings are contained in the DIAG_CFG3 register (Page 0, address 0x67)

6.3.2 Scan Rate

When diagnostics are enabled, the fault diagnostic signal chain is constantly scanning the input channels. This muxing occurs automatically, but the rate at which the channels are scanned can be adjusted in DIAG_CFG3. The repetition rate can be set to 1 ms, 4 ms, 8 ms, or set to continuously scan as fast as possible. The default rate is 4 ms. The scan rate is the time between the end of one scan cycle and the beginning of the next. Since the sample rate of the diagnostic ADC is typically much faster than the scan rate, the scan rate is effectively the time between fault readings.

For the fastest response time and greatest signal integrity for the record channel, it is recommended to use the continuous back-to-back scan mode. This causes the diagnostic ADC to sample at the same rate as the audio ADC and eliminates the small amount of coupling distortion that may arise from discontinuities in the diagnostic sampling. The power consumption of the diagnostic signal chain scales with the scan repetition rate. In back-to-back continuous scanning, the AVDD current can be expected to increase by approximately 2.5 mA compared to the 4-ms scan rate setting. For this reason, it is not recommended to scan continuously in power sensitive applications unless a system is particularly prone to faults and fast response time is needed.

6.3.2.1 DIAG_CFG3 Register (page = 0x00, address = 0x67) [reset = B8h]

This register is configuration register 3 for input fault diagnostics setting.

Figure 25. DIAG_CFG3 Register

7	6	5	4	3	2	1	0
REP_RATE[1:0]		Reserved		FAULT_DBNCE_SEL[1:0]		VSHORT_DBNCE	DIAG_2X_THRES
RW-2h		RW-3h		RW-2h		RW-0h	RW-0h

Table 12. DIAG_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	REP_RATE[1:0]	RW	2h	Fault monitoring scan repetition rate. 0d = Continuous back to back scanning of selected channels input pins without any idle time 1d = Fault monitoring repetition rate of 1 ms for selected channels input pins scanning 2d = Fault monitoring repetition rate of 4 ms for selected channels input pins scanning 3d = Fault monitoring repetition rate of 8 ms for selected channels input pins scanning
5-4	Reserved	RW	3h	Reserved
3-2	FAULT_DBNCE_SEL[1:0]	RW	2h	Debounce count for all the faults (except VBAT_IN short when VBAT_IN < MICBIAS). 0b = 16 counts for debounce to filter-out any false faults detection 1b = 8 counts for debounce to filter-out any false faults detection 2b = 4 counts for debounce to filter-out any false faults detection 3b = No debounce count
1	VSHORT_DBNCE	RW	0h	VBAT_IN short debounce count only when VBAT_IN < MICBIAS. 0b = 16 counts for debounce to filter-out any false faults detection 1b = 8 counts for debounce to filter-out any false faults detection
0	DIAG_2X_THRES	RW	0h	Diagnostic thresholds range scale. 0d = Thresholds same as configured in P0_R101 and P0_R102 1d = All the configuration thresholds get scaled by 2 ×

6.3.3 Moving Average

For more robust detection, the fault monitoring can be based on the moving average of the diagnostic signal. With this setting enabled, each new sample is averaged with the previous set of samples and if a fault occurs the latched registers will not latch until the average of the samples crosses the programmed threshold. This acts as a simple FIR filter and helps avoid triggering faults from transient events in the system.

If debounce and moving average are used together, then the latched register will not latch until the moving average of consecutive samples crosses the programmed threshold and remains there for the programmed debounce count. The moving average can be set to weight new and old data equally, or skewed to give old data 0.75 weightage and new data 0.25 weightage to further improve transient immunity.

The moving average setting is common to all input channels, but can be enabled or disabled independently for the MICBIAS load current and overtemperature faults to achieve faster response times for these faults. Moving average settings are contained in the DIAG_CFG4 register (Page 0, address 0x68)

6.3.3.1 DIAG_CFG4 Register (page = 0x00, address = 0x68) [reset = 0h]

This register is configuration register 4 for input fault diagnostics setting.

Figure 26. DIAG_CFG4 Register

7	6	5	4	3	2	1	0
DIAG_MOV_AVG_CFG[1:0]		MOV_AVG_DIS_MBIAS_LOAD	MOV_AVG_DIS_TEMP_SENS	Reserved			
RW-0h		RW-0h	RW-0h	R-0h			

Table 13. DIAG_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIAG_MOV_AVG_CFG[1:0]	RW	0h	Moving average configuration. 0d = Moving average disabled 1d = Moving average enabled with 0.5 weightage for old scanned data and new scanned data 2d = Moving average enabled with 0.75 weightage for old scanned data and 0.25 weightage for new scanned data 3d = Reserved
5	MOV_AVG_DIS_MBIAS_LOAD	RW	0h	Moving average configuration for MICBIAS high and low load current fault detection 0b = Moving average as defined by DIAG_MOV_AVG_CFG setting 1b = Moving average is forced disabled for MICBIAS load current fault detection to achieve faster response time
4	MOV_AVG_DIS_TEMP_SENS	RW	0h	Moving average configuration for overtemperature fault detection 0b = Moving average as defined by DIAG_MOV_AVG_CFG setting 1b = Moving average is forced disabled for overtemperature fault detection to achieve faster response time
3-0	Reserved	R	0h	Reserved

6.3.4 Response Time

If the moving average feature is not used, the fault response time can be calculated as the scan rate multiplied by the debounce setting. For example, a debounce of 8 and scan rate of 4 ms would require a fault to be present for 32 ms before latching the corresponding fault register. This is useful for filtering out transient behavior such as the startup response of a microphone.

If the moving average feature is used, then the exact response time will depend on the nature of the fault and the amplitude of the input signal causing the fault. This setting can be useful in particularly noisy applications in which the microphone may be prone to saturate for a portion of the time.

Setting the scan rate to continuous provides the fastest response. The exact response time depends on many factors. To simplify calculation, Equation 1 shows how to calculate the effective response time in back-to-back scan mode.

$$\text{Response Time} = (450 \times N + 1000) \times \text{DIAG\_CLK\_PERIOD} \quad (1)$$

where

- N is the number of channels (1 to 6) enabled for diagnostics scan using page-0, register-100d
- and DIAG_CLK_PERIOD is the period of the clock used for the diagnostic state-machine

The diagnostic clock period will depend on whether valid clocks are present and the sample rate. The diagnostic clock frequency will be 6.144 MHz for all ASI sample rate multiples and submultiples of 48 kHz. Similarly, it will be 5.644 MHz for all ASI sample rate multiples and submultiples of 44.1 kHz. If no clocks are present or there is an error in the clocks, then the diagnostic clock will default to the 5-MHz (typical) clock generated using the internal on-chip oscillator.

Live registers will always report the most recent reading and are not influenced by the debounce or moving average settings. The faults in INT_LTCH0 are also not affected by these filter settings.

7 Responding to a Fault

By default, once a fault is detected, an internal interrupt request (IRQ) will be generated. The user can control which faults will generate interrupts using the INT_MASK1, P0_R42 and INT_MASK2, P0_R43 registers. Setting a mask bit to '1' means the corresponding fault is masked and will no longer trigger an interrupt, though the fault will still be recorded in the latched registers as long as the LTCH_READ_CFG bit in the INT_CFG register is set to '0'. Settings in INT_CFG apply to faults for all channels.

The internal IRQ signal can be output on any of the GPIO pins and used to alert the host processor to a fault condition. If the GPIO pins on the PCM6xx0-Q1 is used for another function or there is not an available GPI pin on the host processor, then the user can also choose to periodically poll the fault registers.

The settings in the INT_CFG, P0_R40 register dictate how the device will handle interrupts. The user can program the polarity of the interrupt for output on a GPIO with the INT_POL bit. The INT_EVENT bits set how often an interrupt will assert for a given event. The PD_ON_FLT_CFG bits control whether faults will automatically power down MICBIAS and the affected ADC channels. The user can choose to power down from unmasked faults only, or from any detected fault regardless of mask settings. The PD_ON_FLT_RCV_CFG bit sets whether the device will automatically re-power once the interrupt is no longer asserted, or wait for manual programming from the host. For more information on manual recovery mode, see Section 7.2 Note that ASI bus clock errors will always power down the ADC channels and the device will recover as soon as the error is resolved.

7.1 INT_CFG Register (page = 0x00, address = 0x28) [reset = 0h]

This register is the interrupt configuration register.

Figure 27. INT_CFG Register

7	6	5	4	3	2	1	0
INT_POL	INT_EVENT[1:0]		PD_ON_FLT_CFG[1:0]		LTCH_READ_CFG	PD_ON_FLT_RCV_CFG	LTCH_CLR_ON_READ
RW-0h	RW-0h		RW-0h		RW-0h	RW-0h	RW-0h

Table 14. INT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POL	RW	0h	Interrupt polarity. 0b = Active low (IRQZ) 1b = Active high (IRQ)
6-5	INT_EVENT[1:0]	RW	0h	Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event 1d = INT asserts on any unmasked interrupts event 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	PD_ON_FLT_CFG[1:0]	RW	0h	Powerdown configuration when fault detected for any channel or MICBIAS fault detected. 0d = Faults event are not used for ADC and MICBIAS power down. It is recommend to set these bits as 2d to shutdown the blocks for which fault occurred. 1d = Only unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings 2d = Both masked or unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings. 3d = Reserved
2	LTCH_READ_CFG	RW	0h	Interrupt latch registers readback configuration. 0b = All interrupts can be read through the LTCH registers 1b = Only unmasked interrupts can be read through the LTCH registers

Table 14. INT_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PD_ON_FLT_RCV_CFG	RW	0h	Recovery configuration for ADC channels when fault goes away. 0b = Auto recovery, ADC channels are re-powered up when fault goes away 1b = Manual recovery, ADC channels are required to power-up manually using P0_R119 when fault goes away
0	LTCH_CLR_ON_READ	RW	0h	Configuration for clearing LTCH register bits. 0 = LTCH register bits are cleared on register read only if live status is zero 1 = LTCH register bits are cleared on register read irrespective of live status and set only if live status goes again low to high

In addition to the mask settings, MBDIAG_CFG2, P0_R58 allows the user to select which MICBIAS faults will be used for powerdown of MICBIAS and all ADC channels.

7.1.1 MBDIAG_CFG2 Register (page = 0x00, address = 0x3A) [reset = 10h]

This register is the MICBIAS diagnostic configuration register 2.

Figure 28. MBDIAG_CFG2 Register

7	6	5	4	3	2	1	0
PD_MBIAS_FAULT1	PD_MBIAS_FAULT2	PD_MBIAS_FAULT3	PD_MBIAS_FAULT4	Reserved	Reserved		
RW-0h	RW-0h	RW-0h	RW-1h	RW-0h	R-0h		

Table 15. MBDIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PD_MBIAS_FAULT1	RW	0h	Powerdown configuration of MICBIAS fault 1 0b = No powerdown when MICBIAS fault detected 1b = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1b = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
6	PD_MBIAS_FAULT2	RW	0h	Powerdown configuration of MICBIAS fault 2 0b = No powerdown when MICBIAS fault detected 1b = MICBIAS and all ADC channels gets powerdown when overvoltage fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1b = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
5	PD_MBIAS_FAULT3	RW	0h	Powerdown configuration of MICBIAS fault 3 0b = No powerdown when MICBIAS fault detected 1b = MICBIAS and all ADC channels gets powerdown when overtemperature fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1b = MICBIAS and all ADC channels gets powerdown when overvoltage fault occurs and P0_R40, PD_ON_FLT_CFG = 2d
4	PD_MBIAS_FAULT4	RW	1h	Powerdown configuration of MICBIAS fault 4 0b = No powerdown when MICBIAS fault detected 1b = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d 1b = MICBIAS and all ADC channels gets powerdown when overtemperature fault occurs and P0_R40, PD_ON_FLT_CFG = 2d. It is recommended to use this setting to protect chip from overtemperature fault.
3	Reserved	RW	0h	Reserved
2-0	Reserved	R	0h	Reserved

The exact fault controlled by each bit in MBDIAG_CFG2 changes depending on the PD_ON_FLT_CFG setting in the INT_CFG register. For clarity, Table 16 highlights these definitions.

Table 16. MBDIAG_CFG2 Fault Assignments

Bit Name	Bit Definition	
	PD_ON_FLT_CFG = 1d	PD_ON_FLT_CFG = 2d
PD_MBIAS_FAULT1	MICBIAS and all ADC channels power down when low current fault occurs	MICBIAS and all ADC channels power down when high current fault occurs
PD_MBIAS_FAULT2	MICBIAS and all ADC channels power down when overvoltage fault occurs	MICBIAS and all ADC channels power down when low current fault occurs
PD_MBIAS_FAULT3	MICBIAS and all ADC channels power down when overtemperature fault occurs	MICBIAS and all ADC channels power down when overvoltage fault occurs
PD_MBIAS_FAULT4	MICBIAS and all ADC channels power down when high current fault occurs	MICBIAS and all ADC channels power down when overtemperature fault occurs

7.2 Manual Recovery Sequence

In some applications users may want to wait for input from the host processor before powering back up after a fault has occurred and MICBIAS and ADC channels have been shut down. For this purpose, the PD_ON_FLT_RCV_CFG bit in INT_CFG, P0_R40 can be set to '1' to enable manual recovery mode. In this mode, the device waits for a write of '1' to the MAN_RCV_PD_FLT_CHK bit in the DEV_STS1, P0_R119 register before initiating the startup sequence. The proper sequence for initiating a manual recovery is as follows:

1. Remove all the trigger/event in system which caused the MICBIAS fault
2. Reset PD_MBIAS_HIGH_CURR_FLT and PD_MBIAS_LOW_CURR_FLT bits in P0_R58
3. Set MAN_RCV_PD_FLT_CHK (P0_R119_D0)
4. Wait for at least 10 ms
5. Set PD_MBIAS_HIGH_CURR_FLT and PD_MBIAS_LOW_CURR_FLT bits in P0_R58 as required

It is important not to skip step 2 in this sequence, otherwise the device may fail to startup properly even if faults are no longer present.

7.3 Recommended Fault Register Read Sequence

Once a fault has occurred and an interrupt has been generated, the diagnostic registers can be used to determine present faults. For most applications, the latched registers will be used to identify faults since they may have been transient and no longer reflected in the live registers. When reading latched registers, it is recommended to read each of the latched fault registers to ensure all errors are detected and the latches are reset accordingly. The exact sequence of register reads that should occur will depend on the application and mask settings. The following is provided as a default recommended sequence to avoid missing faults.

1. Read INT_LTCH0 register to determine if any clock, PLL, overtemperature, or overcurrent faults have occurred.
2. Read the Chx_LTCH register to determine which input channels, if any, experienced faults.
3. If a channel has experienced a fault, first read the INT_LTCH1 and INT_LTCH2 registers to determine if an overvoltage fault has occurred.
4. Read the associated CH_LTCH register for the channels identified in step 1 to determine which other faults may have occurred.

Since reading the overvoltage registers in INT_LTCH1 and INT_LTCH2 will clear the short to VBAT_IN bits in the Chx_LTCH registers, it is possible to not detect a short to VBAT_IN if it was a transient short. It is preferred to detect an overvoltage since any short to VBAT_IN will also trigger an overvoltage fault as long as VBAT_IN > MICBIAS (as will be the case in most applications). Furthermore, a short to VBAT_IN is less likely to be transient in nature, and thus could still be read in the respective latched or live register depending on the LTCH_CLR_ON_READ setting.

8 Diagnostic Monitoring Registers

In addition to the latched and live fault registers, the raw data used for fault calculation is stored in diagnostic monitoring registers (P1_R90 to P1_R121). These registers provide voltage readings for each of the input channels, VBAT_IN, and MICBIAS as well as the MICBIAS load and internal die temperature. The MICBIAS load and die temperature registers have unique transfer functions detailed in the following sections. These registers can be used to bypass the on-chip fault processing and develop unique fault algorithms from the raw data. They may also be useful during system debug.

8.1 Voltage Measurements

The raw channel voltage data used for fault calculation is stored as 12-bit SAR ADC code in binary format and can be read from the associated page-1 registers. Data is packed as first MSB byte in one register and then LSB nibble in a second register and is appended with a 4-bit channel-ID. The VBAT_IN, MICBIAS, and channel diagnostic monitoring registers are contained in page 1 registers 90 to 117. Equation 2 is used to convert the raw data to input source voltage.

$$\mathrm{VIN(V)} = \left(\left(0.9 \times \frac{\mathrm{READ\_DATA}}{4095}\right) - 0.211764\right) \times 17 \tag{2}$$

The supported monitoring range is from 0 V to 11.7 V. However, since the readings are only trimmed to 8-bit accuracy, the gain error may prevent reliable reading of voltages greater than 10.8 V as the diagnostic ADC saturates. This means that any overvoltage condition greater than 10.8 V will be reported as a short to VBAT as long as the VBAT is also greater than 10.8 V.

The DIAGDATA_CFG register (page 1: 0x59) allow the user to select whether the SAR data registers are updated continuously or held during register read back. By default, data update is held while registers are being read. If the moving average feature is used, then data must be updated continuously.

8.2 MICBIAS Load Current

The MICBIAS load data is broken into two page 1 registers. DIAG_MON_MSB_MBLOAD (Page 1, address 0x78) contains the MSB data byte of the MICBIAS load current and DIAG_MON_LSB_MBLOAD (Page 1, address 0x79) contains the LSB data nibble of the MICBIAS load current. The supported monitoring range is from 0 mA to 80 mA. Equation 3 shows how to convert this raw binary data to the MICBIAS load current.

$$\mathrm{MICBIAS\ Load\ Current\ (mA)} = \left(\left(0.9 \times \frac{\mathrm{READ\_DATA}}{4095}\right) - 0.2\right) \times 153.8462 \tag{3}$$

The MICBIAS load current measurement is not trimmed for gain and offset error and is intended only as an auxiliary feature for applications that want a rough estimate of the load conditions. The accuracy is approximately the same as the threshold step size of 0.54 mA. If precision load monitoring is required, it is recommended to use an external sensor.

8.3 Internal Die Temperature

An internal diode provides a rough measure of the device die temperature. This temperature monitor is not the same as that used by the overtemperature fault detect circuitry. The supported monitoring range is from –40°C to +150°C and the temperature can be calculated with Equation 4.

$$\mathrm{Temperature(°C)} = 0.1141 \times (3565 - \mathrm{READ\_DATA}) - 40 \tag{4}$$

The die temperature measurement is not trimmed for gain and offset error and is intended only as an auxiliary feature for applications that want a rough estimate of the die temperature. The accuracy of the die temperature sensor is not specified and will vary depending on board layout. However, a rough characterization of the sensor typically shows accuracy around ±5°C. If precision temperature readings are required, it is recommended to use an external sensor.

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