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TI Precision Designs: CerTIfied Design

Digitally Calibrated Bridge Sensor Signal Conditioner with 4mA to 20mA Current Loop Output

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Circuit Description

This bridge sensor conditioner module delivers a well-regulated current output to a ground-referenced load. The first stage uses a mixed-signal programmable gain amplifier (PGA) to provide linearization and temperature compensation to a differential bridge sensor voltage. The second stage converts the PGA output voltage into current and transmits the current over a standard 4 mA to 20 mA current loop. Additional circuitry protects the module against electrostatic discharge (ESD), electrical fast transients (EFT), radiated and conducted electromagnetic interference (EMI), and surge.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
PGA309	Product Folder
XTR117	Product Folder

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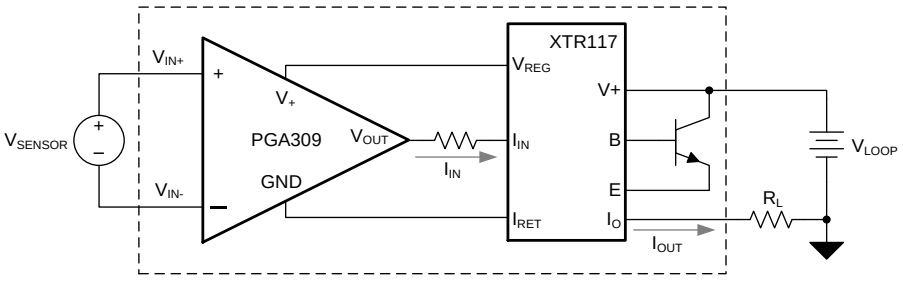
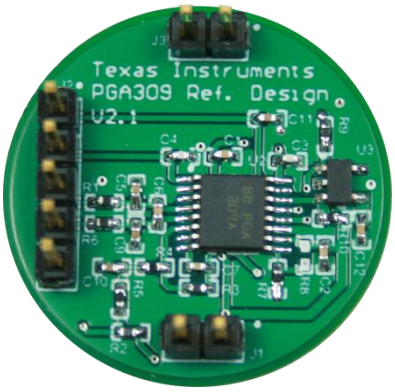




1 Design Summary

The design requirements are as follows:

- Current Loop Supply Voltage: 7.5 V – 40 V dc
- Sensor Voltage Full-Scale Sensitivity: 1 mV/V – 245 mV/V
- Output: 4 mA – 20 mA dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design. Since the module can be calibrated for a wide range of sensors, the input voltage values shown are only representative of one system. Refer to the PGA309 sensor configuration spreadsheet in the supplementary design archive for details on the input sensor configuration used in this design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Measured
Output Error (%FSR over temperature and pressure)	0.1	0.04
Output Current Noise (μA_{PP})	15	6
Max Sensor Nonlinearity (%)	±3	±4

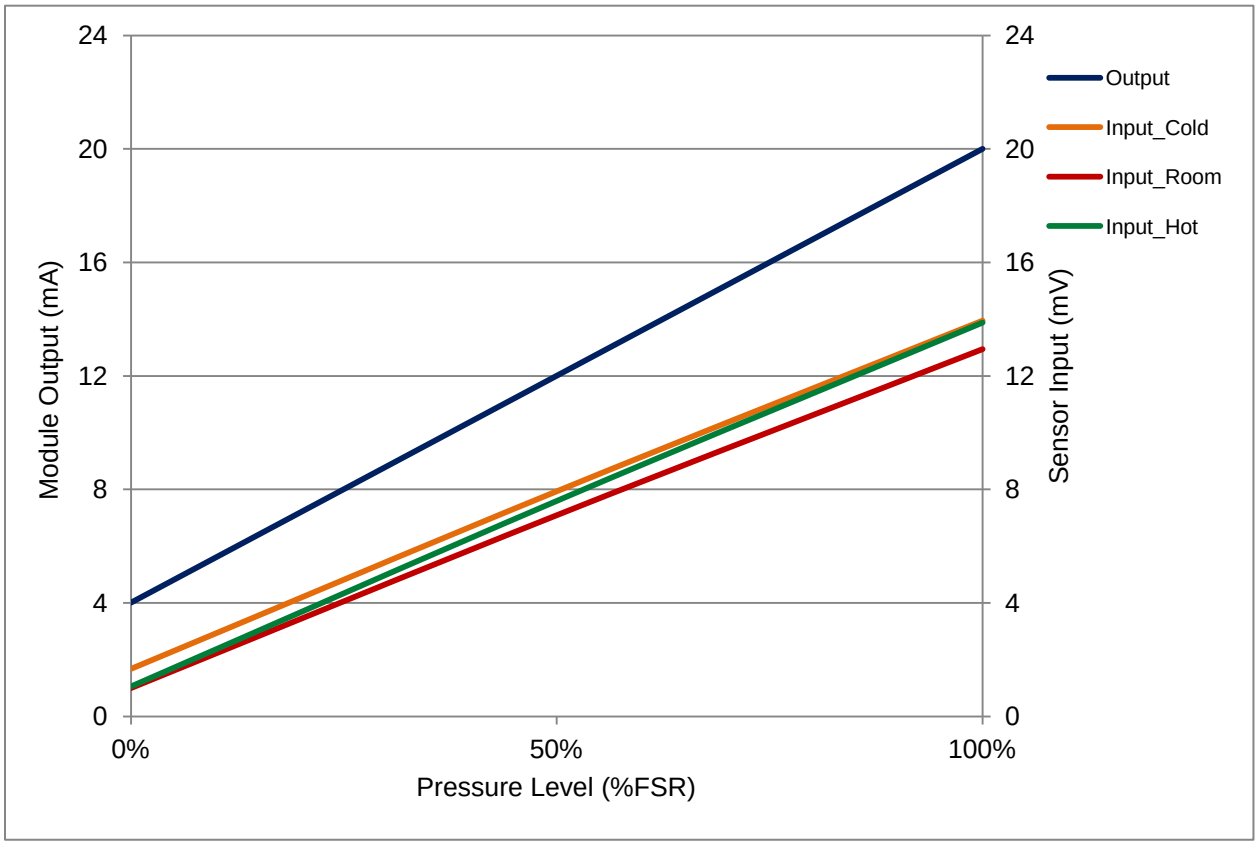


Figure 1: Measured Transfer Function

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The transfer function of the circuit is based on the relationship between the input voltage, V_{SENSOR}, the gain and offset blocks in the PGA309, and the input currents to the XTR117. In the first stage, the bridge sensor differential input voltage, V_{SENSOR}, is conditioned and linearized by the PGA309 in order to produce V_{OUT}. In the second stage, V_{OUT} is converted to a current by a series resistance and is then added to a constant reference current to create I_{IN}, the total current input to the XTR117. I_{IN} is amplified by the fixed current gain of the XTR117 and transmitted over a two-wire current loop.

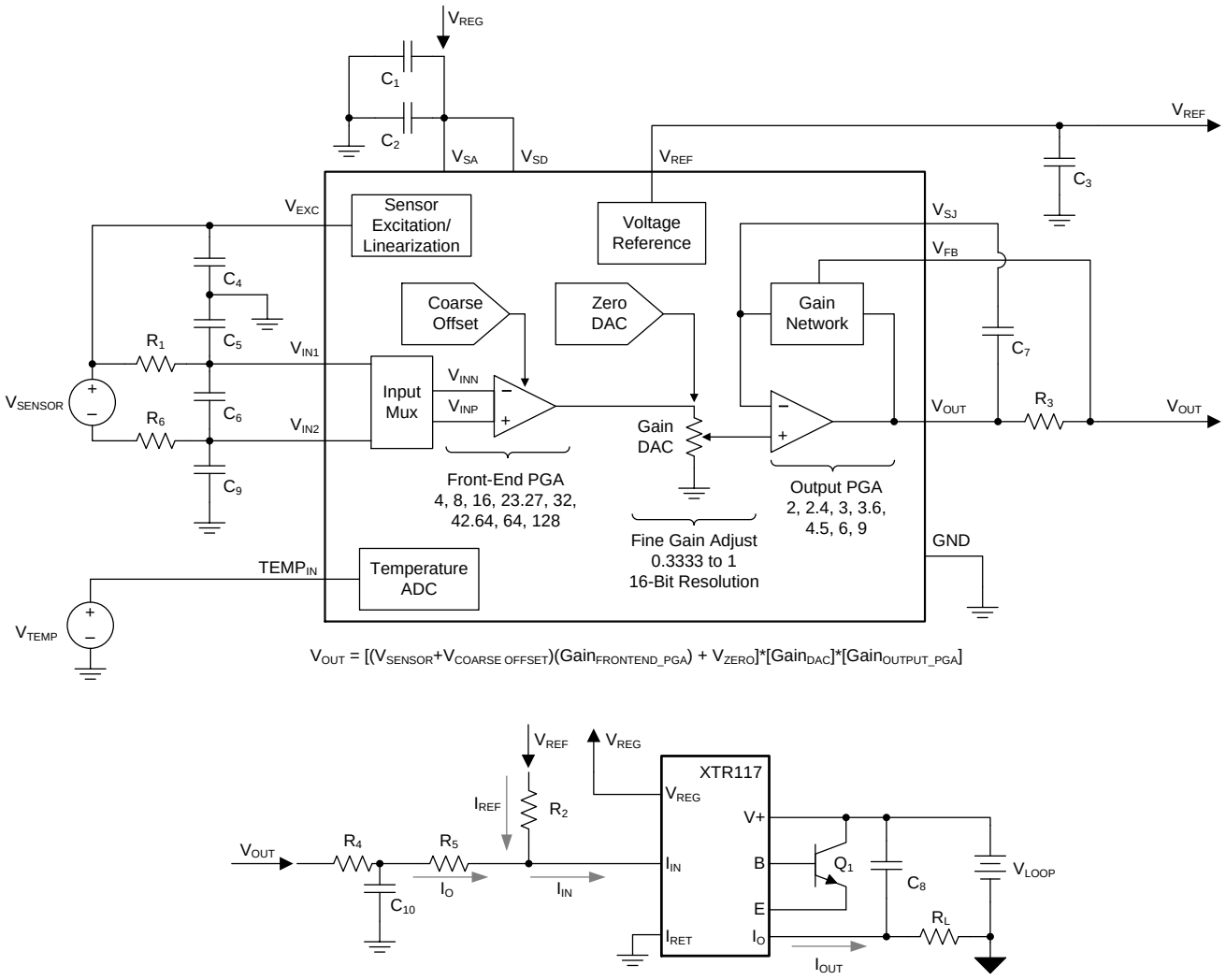


Figure 2: Complete Circuit Schematic

The transfer function for this design is defined by the following equations:

$$V_{OUT} = \left[(V_{SENSOR} + V_{COARSE\ OFFSET}) * \left(Gain_{FRONTEND\_PGA}\right) + V_{ZERO}\right] * [Gain_{DAC}] * \left[Gain_{OUTPUT\_PGA}\right] \quad (1)$$

$$I_O = \frac{V_{OUT}}{R_4 + R_5} \quad (2)$$

$$I_{REF} = \frac{V_{REF}}{R_2} \quad (3)$$

$$I_{IN} = I_O + I_{REF} \quad (4)$$

$$I_{OUT} = I_{IN} * 100 \quad (5)$$

2.1 First Stage: Voltage-output Bridge Sensor Signal Conditioner

The first stage of the circuit uses the PGA309 to condition a differential bridge sensor voltage. The output voltage of the PGA309, V_{OUT}, can be digitally calibrated to very accurate values (error less than 0.1% of full scale). To ensure that the input signal is as free of noise as possible, a low-pass filter network is placed between the sensor output and the PGA309 input pins.

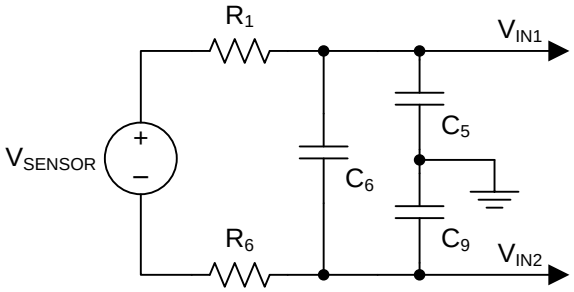


Figure 3: Sensor Voltage Input Filter

The input filter has both a common-mode component and a differential component. Since the sensor voltage signal is a dc signal, the cutoff frequencies of this filter can be set very low in order to attenuate any ac noise which may be present.

The cutoff frequencies of the filter are defined by the following equations:

$$R_1 = R_6;\ C_5 = C_9;\ C_6 = 10 * C_5 \quad (6)$$

$$f_{C\_DIFF} = \frac{1}{2 * \pi * 2R_1 * (10C_5 + \frac{1}{2}C_5)} = \frac{1}{42 * \pi * R_1 * C_5}\ \text{Hz} \quad (7)$$

$$f_{C\_CM} = \frac{1}{2 * \pi * R_1 * C_5}\ \text{Hz} \quad (8)$$

The desired cutoff frequency for the differential filter is f_{C_DIFF} = 20 Hz in order to attenuate practically all differential ac noise. The cutoff for the common-mode filter should be set at least a decade higher in order to avoid converting common-mode noise pickup (such as 60 Hz noise) to a differential signal which would be amplified by the PGA309. Solving for R_1 and C_5 in order to set the desired differential filter frequency will achieve this automatically since C_6, the common-mode filter capacitor, is set to ten times the value of C_5.

A simple way to calculate the required passive component values is to select a common value for C_5, usually 10 nF, and solve for R_1. By rearranging the terms of the equations above, the required value of R_1 is defined as:

$$R_1 = \frac{1}{42 * \pi * C_5 * f_{C\_DIFF}} \quad (9)$$

Substituting C_5 = 10 nF and f_{C_DIFF} = 20 Hz in the equation above yields the following ideal value for R_1:

$$R_1 = 37.9\ k\Omega$$

Given this ideal value, 39.2 kΩ was selected as a nearby 1% standard value. Using the final circuit values of R_1 = 39.2 kΩ and C_5 = 10 nF, the final cutoff frequencies of the filter are:

$$f_{C\_DIFF} = 19.3\ Hz$$

$$f_{C\_CM} = 406\ Hz$$

Once the sensor voltage signal reaches the PGA309, the gain, offset, and linearization circuitry inside the device performs the required signal conditioning. There are six key functional blocks within the PGA309:

1. **Linearization DAC:** adjusts the bridge sensor excitation voltage, V_{EXC}, in order to compensate for the inherent nonlinearity of the sensor.
2. **Coarse Offset DAC:** adds a dc voltage offset to the input of the front-end PGA.
3. **Front-end PGA:** provides gain from 4 V/V to 128 V/V.
4. **Zero DAC:** adds a fine dc voltage offset to the output of the front-end PGA.
5. **Gain DAC:** attenuates the output of the front-end PGA by up to 1/3.
6. **Output PGA:** provides gain from 2 V/V to 9 V/V.

Each of these functional blocks is digitally programmed to a specific value either by registers inside the PGA309 or by an external EEPROM. These values should be calibrated either over a one-wire or I^2C digital interface. A full description of the calibration algorithm is given in the supplementary design archive.

The equations defining the transfer function of the PGA309 are given at the beginning of Section 2. For a detailed explanation of the internal circuitry of the PGA309, see Section 2 of the PGA309 User's Guide.

2.2 Second Stage: V-I Converter and Current Transmitter

The second stage of the circuit uses a series resistance, R_4 + R_5, to convert V_{OUT} to a current, I_O. From a dc perspective R_4 and R_5 could be replaced with a single resistor, but the two-resistor topology allows an additional first-order low-pass filter to be easily implemented.

The fixed reference voltage of the PGA309, V_{REF}, is used with R_2 to create a constant offset current, I_{REF}. I_O and I_{REF} are summed to generate I_{IN}, the total input current to the XTR117. The XTR117 amplifies I_{IN} and transmits the resulting output current, I_{OUT}, over a two-wire current loop. The current gain of the XTR117 is fixed at 100 A/A, so in order to achieve I_{OUT} = 4 mA to 20 mA, I_{IN} must equal 40 µA to 200 µA.

The most straightforward approach to selecting the components for this stage is as follows:

1. Define the target PGA309 V_{OUT} and XTR117 I_{OUT} range as is best suited for the application.
2. Calculate the values of R_4 and R_5 based on the output voltage and output current span defined in the previous step.
3. Calculate the value of R_2 needed to generate the desired minimum XTR117 output current.
4. Calculate the value of C_{10} which will create the desired low-pass filter cutoff frequency at the input of the XTR117.

2.2.1 Define the Target V_{OUT} and I_{OUT} Range

The target range for the linear output current of the XTR117 is simple to define, as it should follow the 4 mA to 20 mA industrial standard. However, it is advantageous to design for a wider output range in order to accommodate possible over-scale and under-scale fault conditions. The actual range specified is dependent on the needs of the end application, but for this reference design the target output current range is set as follows:

$$I_{OUT\_MAX} = 25\ mA$$

$$I_{OUT\_MIN} = 2.85\ mA$$

The output voltage of the PGA309 can swing within 100 mV of its power supply rails, so the required output voltage range is set to these limits with an additional 50 mV of headroom.

$$V_{OUT\_MAX} = 4.85\ V$$

$$V_{OUT\_MIN} = 0.15\ V$$

2.2.2 R_4 and R_5 Calculation

R_4 and R_5 convert the PGA309 output voltage, V_{OUT}, to a current, defined in this design as I_O. The required total series resistance of R_4 and R_5 can be calculated from the target I_{OUT} and V_{OUT} range defined in the previous step. The XTR117 current gain of 100 A/A is also taken into consideration.

$$(R_4 + R_5) = \frac{V_{OUT_{MAX}} - V_{OUT_{MIN}}}{\frac{I_{OUT_{MAX}}}{100} - \frac{I_{OUT_{MIN}}}{100}} = \frac{4.85\ V - 0.15\ V}{250\ \mu A - 28.5\ \mu A} = 21.2\ k\Omega \quad (10)$$

The series combination of R_4 and R_5 should equal 21.2 kΩ, and a simple way to determine the value of each resistor is to pick a common value for R_5 and solve for R_4. If R_5 is selected to be 10 kΩ, the value of R_4 can easily be calculated using the following equation:

$$R_4 = 21.2\ k\Omega - 10\ k\Omega = 11.2\ k\Omega \quad (11)$$

The closest 1% standard resistor value is 11.3 kΩ, which is the value selected for this design.

2.2.3 R_2 Calculation

In Section 2.2.1 the minimum output current, I_{OUT_MIN}, was defined to be 2.85 mA. The actual minimum output current can be calculated using the following equation:

$$I_{OUT\_MIN\_actual} = \frac{V_{OUT\_MIN}}{R_4 + R_5} * 100 = \frac{0.15\ V}{21.3\ k\Omega} * 100 = 704.225\ \mu A \quad (12)$$

Given this result, it is clear that additional current is needed to achieve the desired output. The voltage reference of the PGA309, V_{REF}, can be used with R_2 to create this additional current, called I_{REF}. The required values of I_{REF} and R_2 can be calculated using the following equations:

$$I_{REF} = I_{OUT\_MIN} - I_{OUT\_MIN\_actual} = 2.85\ mA - 704.225\ \mu A = 2.146\ mA \quad (13)$$

$$R_2 = \frac{V_{REF}}{I_{REF}} = \frac{4.096\ V}{2.146\ mA} = 190.9\ k\Omega \quad (14)$$

The closest 1% standard resistor value is 191 kΩ, which is the value selected for this design. The approximate value of the minimum and maximum output currents can now be calculated. Any error will be corrected during the calibration process.

$$I_{OUT\_MIN} = \left(\frac{V_{OUT\_MIN}}{R_4 + R_5} + \frac{V_{REF}}{R_2}\right) * 100 = \left(\frac{0.15\ V}{21.3\ k\Omega} + \frac{4.096\ V}{191\ k\Omega}\right) * 100 = 2.85\ mA \quad (15)$$

$$I_{OUT\_MAX} = \left(\frac{V_{OUT\_MAX}}{R_4 + R_5} + \frac{V_{REF}}{R_2}\right) * 100 = \left(\frac{4.85\ V}{21.3\ k\Omega} + \frac{4.096\ V}{191\ k\Omega}\right) * 100 = 24.91\ mA \quad (16)$$

2.2.4 C_{10} Calculation

R_4 and C_{10} create a low-pass filter to reduce high-frequency noise generated by the PGA309 before the signal reaches the XTR117 input pins. The cutoff frequency of the filter is defined as:

$$f_C = \frac{1}{2 * \pi * R_4 * C_{10}} \quad (17)$$

The PGA309 generates noise at 2 kHz and above, so the desired cutoff frequency of the filter is 1.4 kHz. This ensures that significant attenuation is achieved by 2 kHz. Since the value of R_4 has already been determined, the terms in Equation 13 can be rearranged to solve for C_{10}.

$$C_{10} = \frac{1}{2 * \pi * R_4 * f_C} = \frac{1}{2 * \pi * 11.3\ k\Omega * 1.4\ kHz} = 10.06\ nF \quad (18)$$

10 nF is a standard capacitor value, which is the value selected for this design.

3 Component Selection

3.1 Semiconductor Selection

This reference design is atypical in that a specific device must be used in order to achieve the functionality described in this document. For proper bridge sensor signal conditioning, including temperature compensation, the PGA309 is required. No other device includes the complete feature set needed for this application.

The requirements for the current transmitter in the second stage are fairly straightforward. The device must be a two-wire transmitter able to handle a wide loop supply voltage range, accept a current input, and power other circuitry with an integrated voltage regulator. The XTR117 is a high-precision two wire transmitter with a loop supply range of 7.5 V to 40 V, a maximum input current of 250 µA, and an internal 5 V voltage regulator. The low quiescent current of the XTR117 ensures that power consumption requirements are met, and low span error drift will reduce total system errors after calibration.

3.2 Transistor Selection

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8 W with high loop voltage (40 V) and 20 mA output current. Virtually any NPN transistor with sufficient voltage, current, and power rating is suitable for this design. Case style and thermal mounting considerations often influence the choice for any given application.

The FCX690BTA NPN transistor was chosen in this design because it exceeds all key specifications and takes up a minimal amount of PCB area with its small SOT-89 package.

3.3 Passive Component Selection

The passive components with the greatest impact on this design are the resistors and capacitors in the PGA309 input filter network, R_1, R_6, C_5, C_6, and C_9, and the resistors and capacitors in the XTR117 input filter and voltage-to-current conversion network, R_4, C_{10}, R_5, and R_2.

In most applications, the cutoff frequencies of the filters do not need to be extremely accurate. In this case, resistor tolerance of ±1% and capacitor tolerance of ±10% are sufficient. Select tighter tolerances if required by the application. Also, there is typically no need for very high-precision or very low-temperature-coefficient resistors in the voltage-to-current conversion circuitry as any errors will be calibrated out and the circuitry is usually installed in a sealed enclosure with a very stable thermal environment.

Other passive components in this design may be selected for 1% or greater tolerance as they will not directly affect the transfer function of this design. Ensure that all capacitors selected have sufficient voltage ratings.

3.4 Protection Component Selection

Several additional circuit components ensure that the system has sufficient protection to pass a series of EMC (electromagnetic compatibility) tests which expose the system to extreme electrical conditions including ESD (electrostatic discharge), EFT (electrical fast transients), surge (simulates a lightning strike), and EMI (electromagnetic interference). If a system is able to pass these tests, it is robust enough to survive in some of the harshest electrical environments.

Protection against ESD, EFT, and surge is provided by a Schottky diode and two TVS (transient voltage suppressor) diodes. The BAS70-TP Schottky diode ensures that no current flows through the current loop when the power terminals are connected in reverse polarity. This diode protects against reverse voltages up to 70V, and the small SOT-23 package takes up a minimal amount of PCB area.

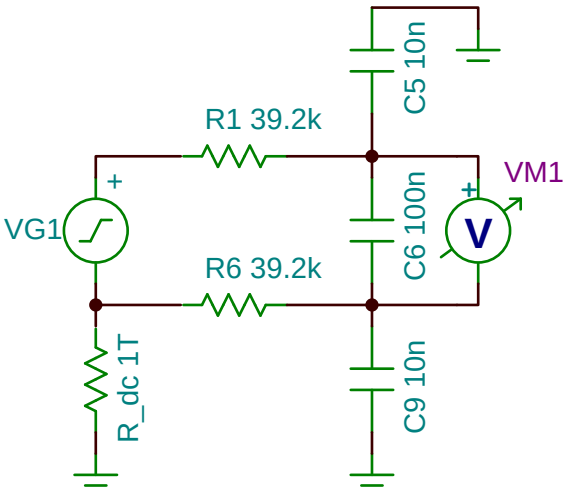
Since the loop supply voltage of the system can reach up to 40 V, the TVS diode near the XTR117 should have a breakdown voltage slightly higher than 40 V. Similarly, the TVS diode near the PGA309 should have a breakdown voltage slightly higher than 5 V. The diodes must also be bidirectional, have a reverse leakage current of 5 µA or less in order to not significantly impact the accuracy of the current output, and have a response time of less than 1 ns in order to properly handle the various test conditions. Based on these requirements the SMBJ40CA and SMBJ5V0CA were selected to protect the XTR117 and PGA309, respectively.

Protection against EMI is provided by a pair of ferrite beads in series with the current loop supply. These components should have high impedance at the most critical ac frequencies, a current rating greater than the maximum loop current, and a low dc resistance to prevent significant voltage drops during normal operation. The HZ0603C601R-10 meets these requirements and is available in a small 0603 package.

4 Simulation

At the time of writing no simulation models are available for the PGA309 and XTR117, so it is currently not possible to simulate the full functionality of the system. However, the filter networks in the system are made of passive components, so they can be easily modeled in order to verify their transfer characteristics. The TINA-TI™ schematics shown in Figure 4 through Figure 9 include the component values obtained during the design process.

4.1 PGA309 Input Filter (Differential)



PGA309 Input Filter – Differential

$f_C = 1/(2*\pi*2R_1*(10C_5+0.5C_5))$

$f_C = 1/(42*\pi*39.2k\Omega*10nF)$

$f_C = 19.33$ Hz

Figure 4: PGA309 Input Filter (Differential) – Schematic

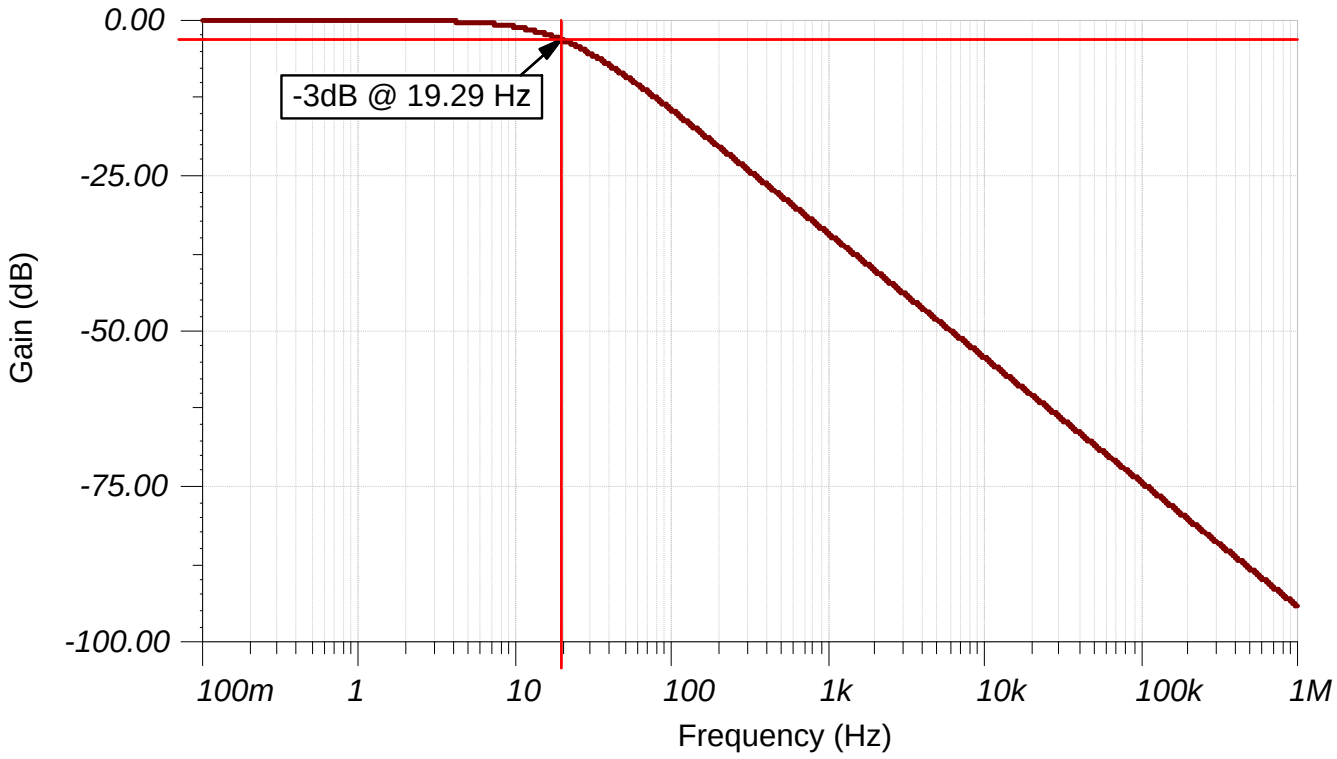
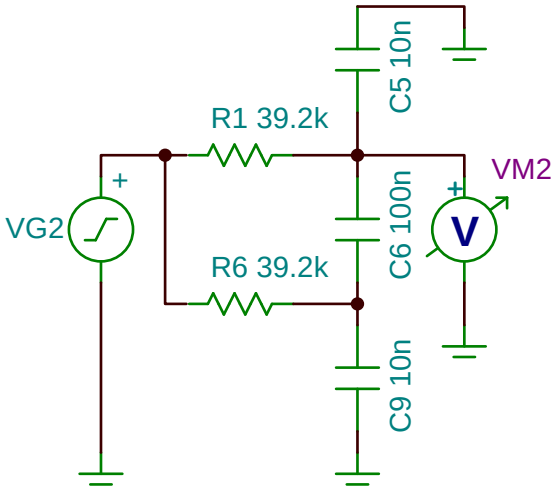


Figure 5: PGA309 Input Filter (Differential) – Transfer Characteristic

4.2 PGA309 Input Filter (Common-mode)



PGA309 Input Filter – Common-Mode

$f_C = 1/(2*\pi*R_1*C_5)$

$f_C = 1/(2*\pi*39.2k\Omega*10nF)$

$f_C = 406$ Hz

Figure 6: PGA309 Input Filter (Common-Mode) – Schematic

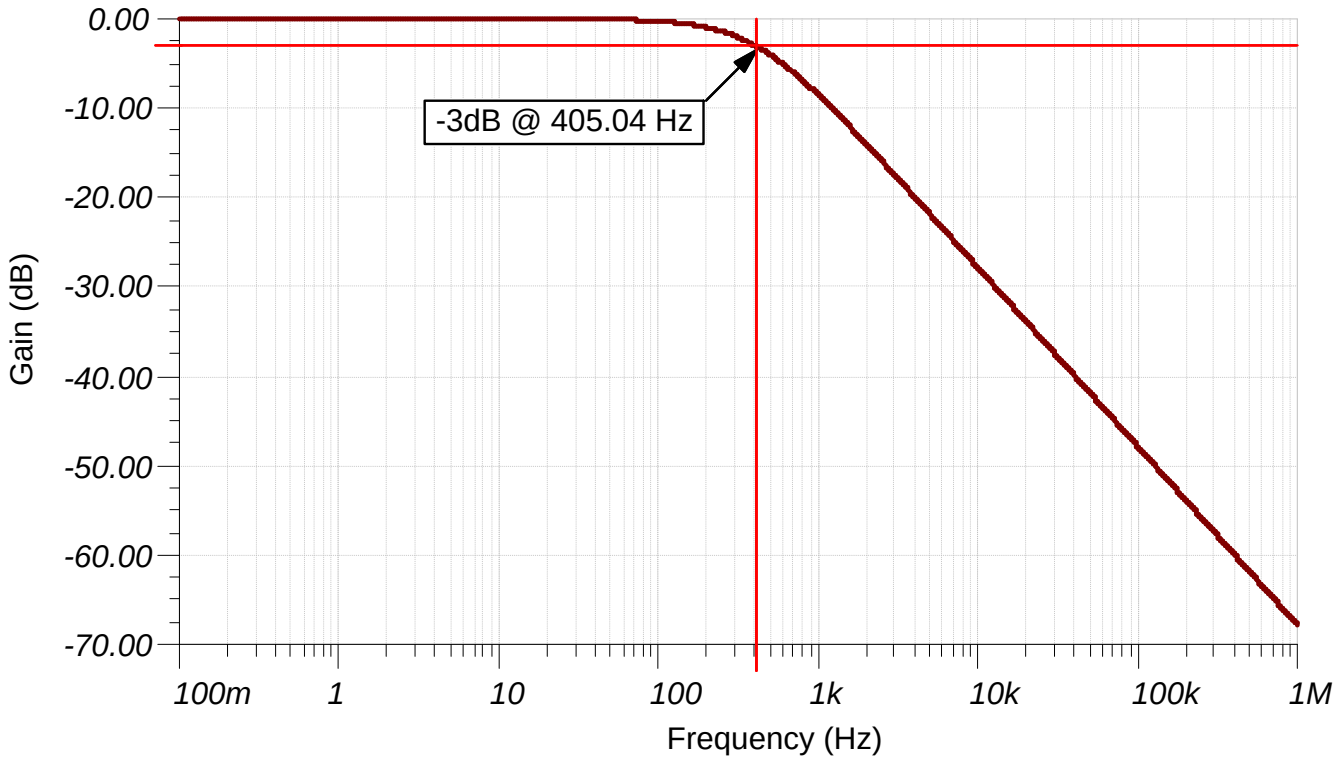


Figure 7: PGA309 Input Filter (Common-Mode) – Transfer Characteristic

4.3 XTR117 Input Filter

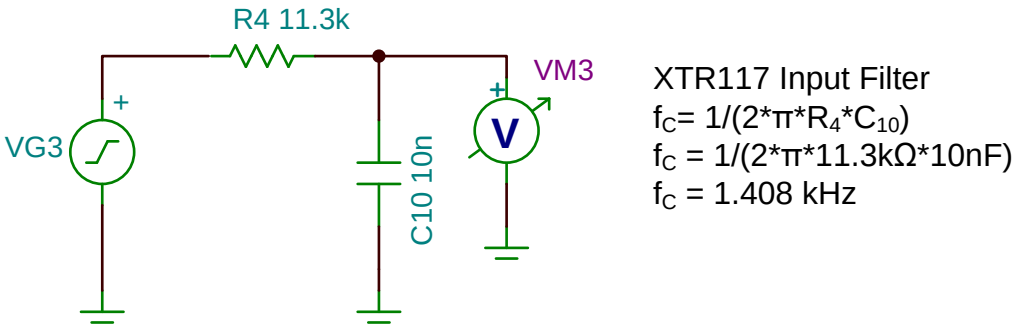


Figure 8: XTR117 Input Filter – Schematic

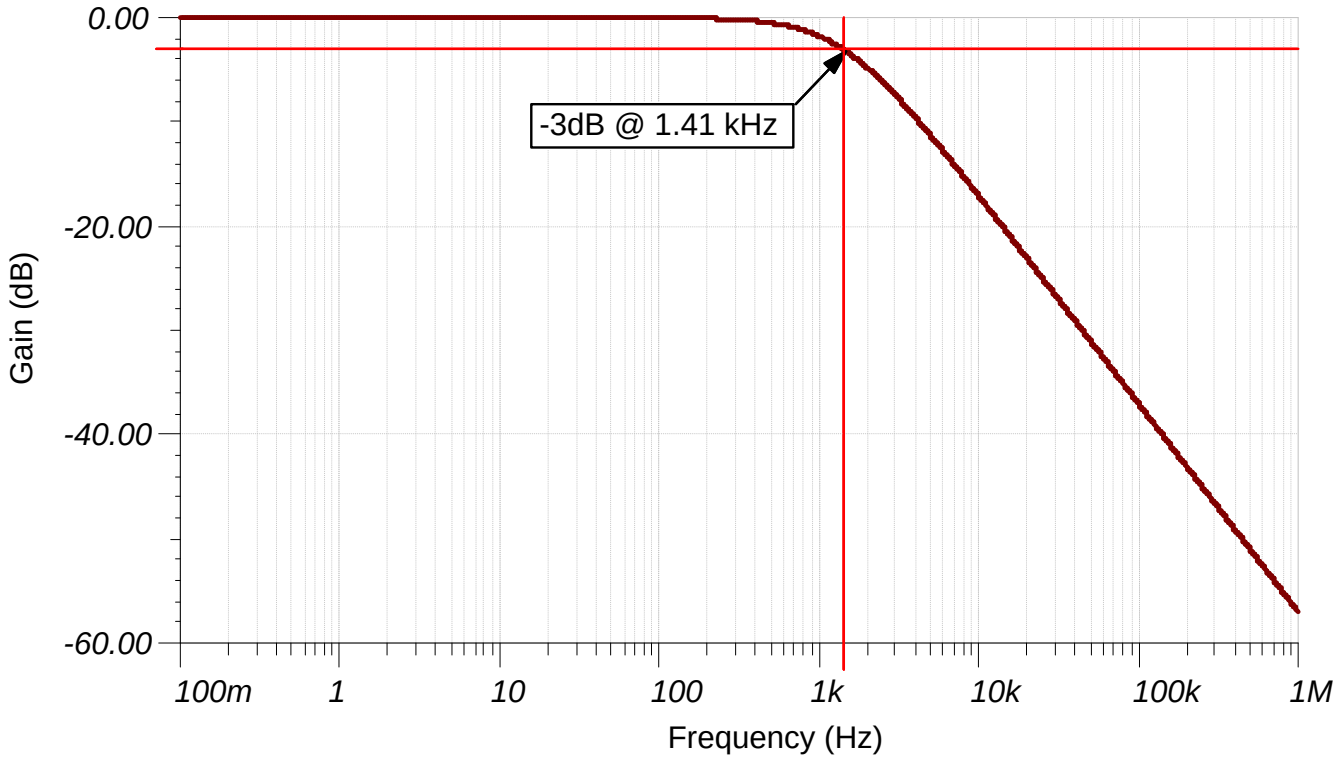


Figure 9: XTR117 Input Filter – Transfer Characteristic

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB board used in this design is in the shape of a circle with a 1 inch diameter. This shape and size is very typical among sensor module systems and allows the design to be easily implemented in a real product with minimal modifications. Because of this very small size, component placement is very dense and efficient routing is critical. The high-level approach to this layout is to place the first stage components – the PGA309 (U2) and supporting circuitry – on the top layer and the second stage components – the XTR117 (U1) and supporting circuitry, as well as the protection components – on the bottom layer.

Connections to the external bridge sensor are made at J2, and the differential bridge sensor signal traces are short and direct to the PGA309 input pins. The digital communication traces (1W, SDA, SCL) are routed away from the analog signal traces to prevent unwanted crosstalk. All decoupling capacitors are located very close to their associated power pins. A solid copper plane on both layers provides an excellent low-impedance path to ground. Connections to the current loop supply are made at J3, and the one-wire digital interface connects at J1.

Heat produced by the power dissipation in Q_1 can cause ambient temperature changes which can influence the performance of the XTR117. To minimize this effect, Q_1 is placed as far away from the XTR117 as possible.

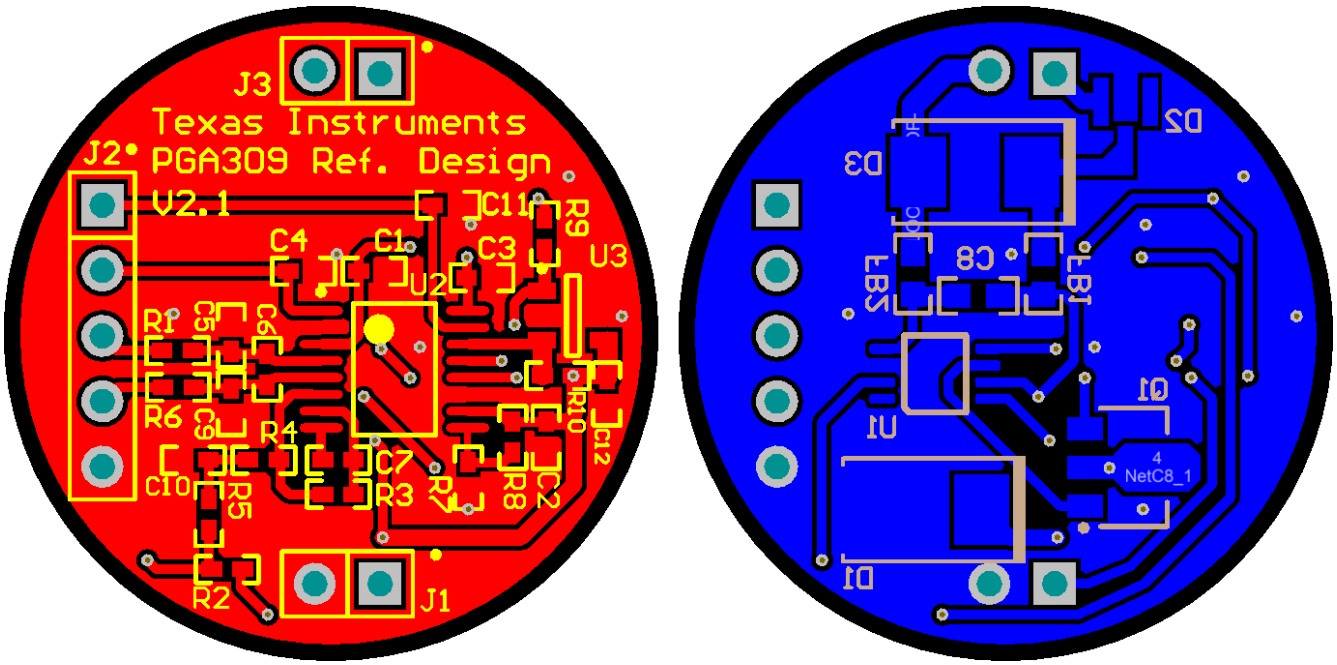


Figure 10: PCB Layout

6 Verification & Measured Performance

6.1 Bench Test Setup

The circuit defined by this reference design is intended to represent a functional block which, in a real application, would only be part of a greater complete system. Because of this, additional hardware and software are required to calibrate and test the design. The required test setup consists of the components listed below. Additional documentation and downloads are available by clicking the link on each component's name. Figure 11 and Figure 12 show the full bench test setup and a screenshot of the software after a successful calibration.

1. Sensor Emulator EVM: emulates bridge sensor pressure and temperature signals. Its output characteristics are user-configurable and can be determined by using the PGA309 Sensor Configuration spreadsheet in the supplementary design .zip file.
2. USB-DAQ Platform: generates digital communication signals, connects to current loop power supply, measures module output
3. PGA309EVM-USB Software: controls digital communication with the PGA309 and performs all calibration calculations based on measurements from USB-DAQ Platform
4. Steel paint can: acts as an enclosure for the reference design module and improves performance by blocking extrinsic noise.

Figure 11: Bench Test Setup

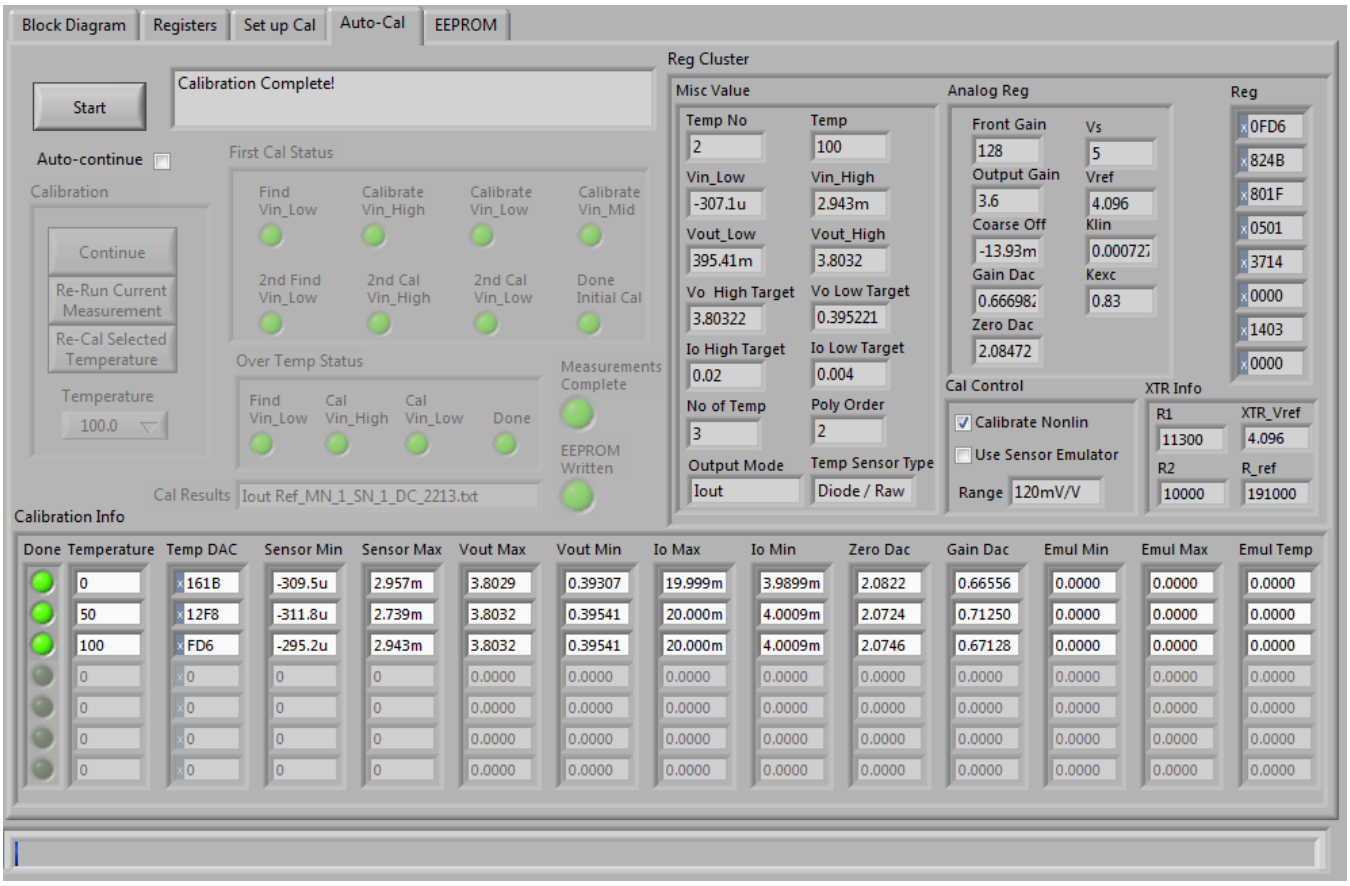


Figure 12: PGA309EVM-USB Software (Post-Calibration)

6.2 Module Output Error

The system was allowed to soak at maximum output power for ten minutes in order to reach thermal equilibrium. Next, the output of the module was calibrated at 0%, 50%, and 100% pressure across three temperature points (“cold,” “room temperature,” “hot”). This creates a total of nine test conditions - one for each combination of pressure and temperature. The desired behavior is that the output of the module will remain within 0.1% of the ideal value, regardless of temperature. Table 2 lists the ideal output for each pressure condition, as well as the minimum and maximum allowable output.

Table 2. Module Output Specifications

Pressure Signal (%FSR)	Ideal Output (mA)	Minimum Output (mA)	Maximum Output (mA)
0	4	3.984	4.016
50	12	11.984	12.016
100	20	19.984	20.016

The error of the module’s output is determined using the standard equation for error as a percent of full-scale range. This equation is defined as:

$$\text{Error}_{\%\text{FSR}} = \frac{\text{Value}_{\text{MEASURED}} - \text{Value}_{\text{IDEAL}}}{\text{Span}} * 100 \quad (19)$$

Once calibration was complete, each pressure and temperature condition was tested for ten minutes. During this time the output was recorded with a data acquisition program and exported to a spreadsheet. The average output value was determined and the error was calculated. Figure 13 gives the results of the test. This result is only indicative of the behavior of one system, so results may vary.

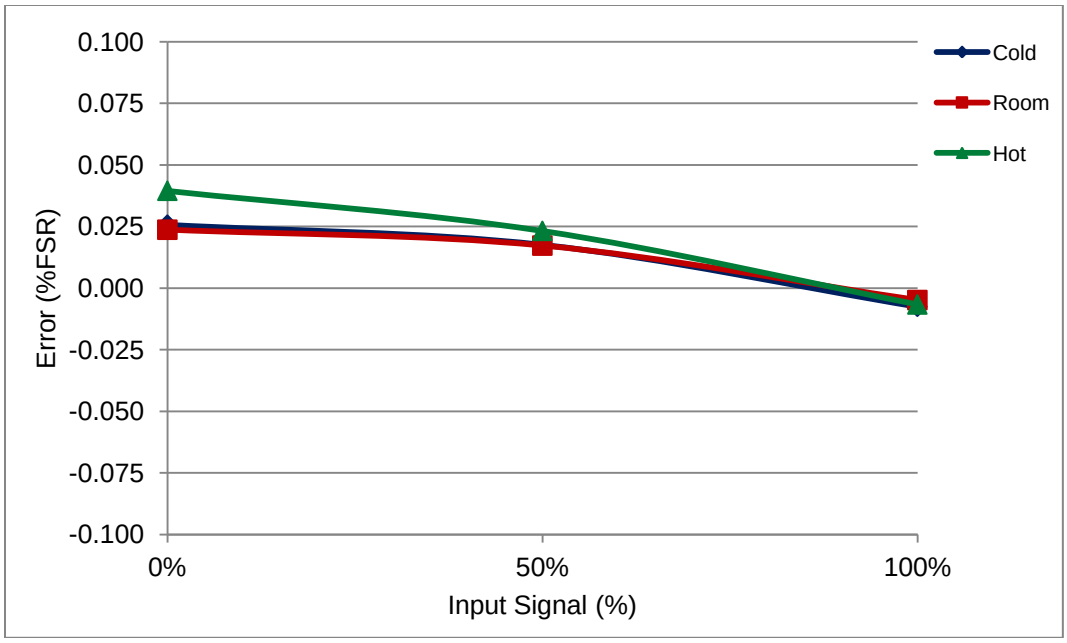


Figure 13: Module Output Error Test Result

6.3 Module Output Noise

After the output error test described in Section 6.2, the system was placed inside a sealed steel paint can to simulate a real-world product in a sealed metal enclosure. The can acts as an effective barrier against extrinsic noise, ensuring that any noise measured originates within the circuit. The can is shown in Figure 14.

Figure 14: Steel Paint Can

The input signal was set to 100% at room temperature and the system output was recorded. Figure 15 gives the results of the test. This result is only indicative of the behavior of one system, so results may vary.

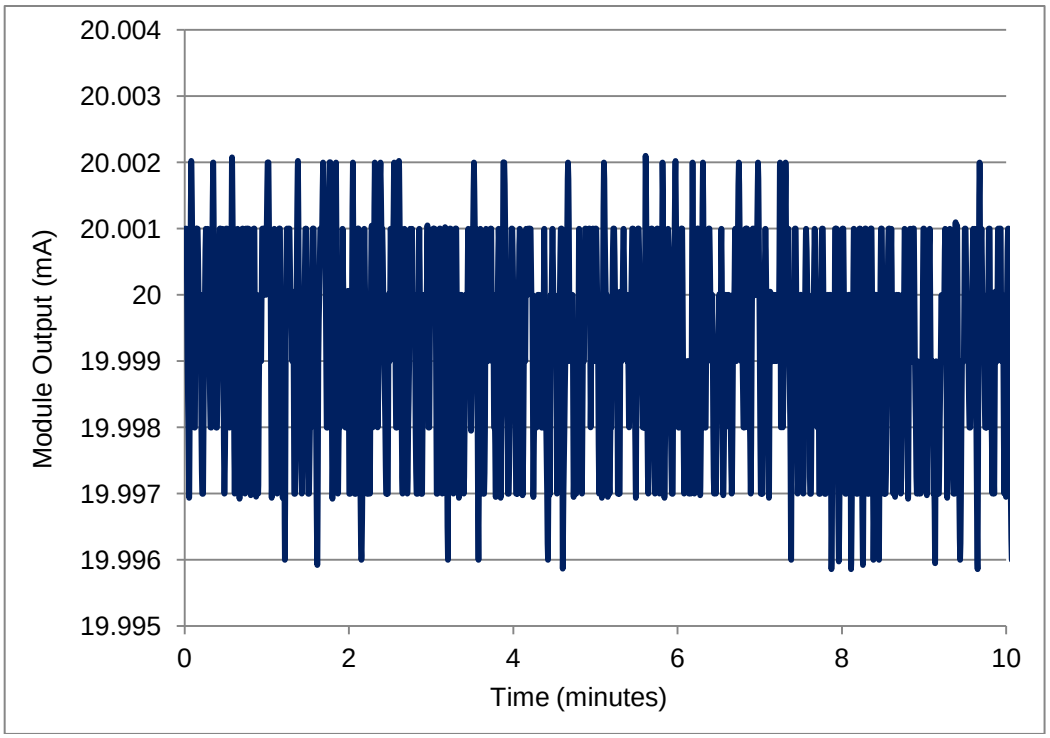


Figure 15: Module Output Noise Test Result

6.4 Maximum Sensor Nonlinearity

The characteristics of the bridge sensor at the input to the PGA309 can vary greatly from application to application. In order to handle this variation, the PGA309 must have a wide adjustment capability. Table 3 lists the adjustment range of the PGA309 for several bridge sensor parameters.

Table 3. PGA309 Sensor Adjustment Capability

Full-scale Sensitivity	1 mV/V to 245 mV/V
Span Drift	> ±3300 ppmFS/°C
Span Drift Nonlinearity	≥ 10%
Zero Offset	±200%FS
Zero Offset Drift	> ±3300 ppmFS/°C
Zero Offset Drift Nonlinearity	≥ 10%
Sensor Impedance	> 200 Ω

One key specification which is not listed is the maximum pressure nonlinearity of the sensor – the second-order nonlinearity of the sensor output voltage versus applied pressure signal (given in % of span). An example of this nonlinearity is given in Figure 16.

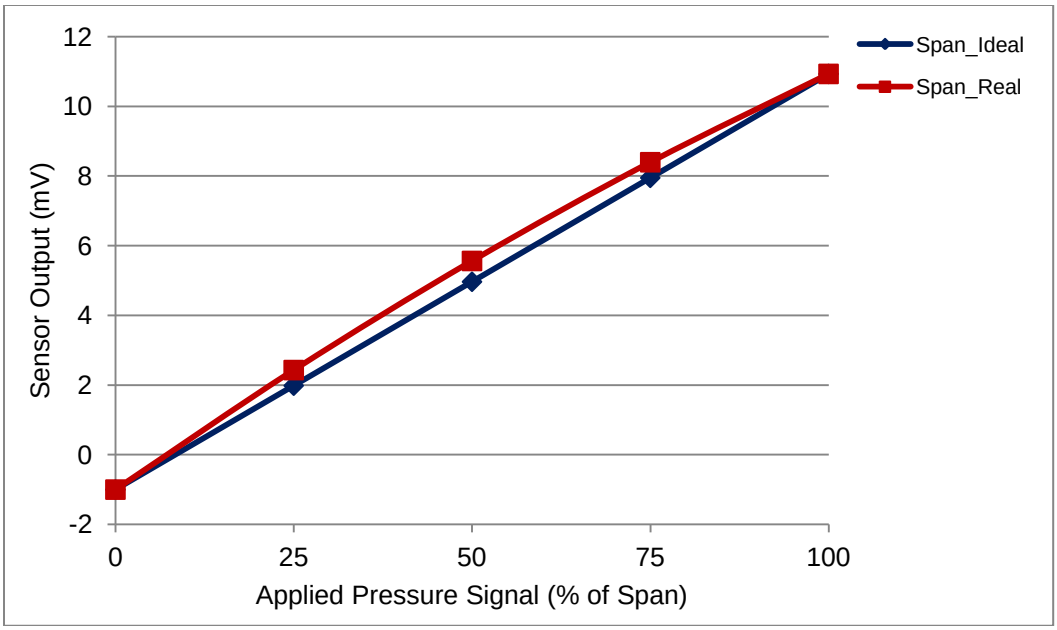


Figure 16: Sensor Output, Ideal vs. +4% Nonlinearity

The reason this maximum nonlinearity is not specified is because there is no single specification which applies to every system. The PGA309 supply, reference and output voltages, as well as the bridge sensor span and offset, all affect the maximum nonlinearity. See Section 2.6 in the PGA309 User's Guide for a detailed explanation of the linearization function.

Knowing this, only the maximum nonlinearity of **our test system** can be determined. Again, the results of this test only apply to **this specific configuration** – refer to the PGA309 sensor configuration spreadsheet in the supplementary design archive for the bridge sensor characteristics used.

Testing this capability is straightforward. The nonlinearity of the emulated pressure signal was initially set to zero, then incremented until the system failed to calibrate. Since the nonlinearity can be positive or negative, the test was repeated in both the positive and negative directions.

Table 4. PGA309 Pressure Sensor Nonlinearity Adjustment Capability

Maximum Nonlinearity	+4%
Minimum Nonlinearity	-4%

6.5 Measured Result Summary

Table 5. Comparison of Design Goal and Measured Performance

	Goal	Measured
Output Error (%FSR over temperature and pressure)	0.1	0.04
Output Current Noise (μA_{PP})	15	6
Max Sensor Nonlinearity (%)	±3	±4

7 Certification Testing Results

Since every product is different, there is typically no standard definition of a pass/fail condition for the various certification tests. Rather, the designer of the product defines the pass/fail condition for the specific product under test.

The intended behavior for this design is that it will maintain its calibrated output current with less than 0.1% error, so the pass/fail condition for each test is that the output current error remains within the ±0.1% error range.

Detailed descriptions of each test, including the hardware setup and signal levels applied to the unit under test, are given in Appendix B.

7.1 IEC 61000-4-2: ESD (Electrostatic Discharge)

ESD testing had little effect on the output of the module. It was able to maintain accurate performance across all conditions listed in Table 6. Figure 17 displays a capture of the output of the module during all of the ESD tests. As shown, at no point during the testing did the data deviate outside of the specified values. After the testing was complete there was not a measurable deviation from the pre-test conditions.

Table 6. ESD Test Result

Test	Result	Class
Vertically Coupled Discharge – 8 kV	Pass	A
Horizontally Coupled Discharge – 8 kV	Pass	A
Contact Discharge – 8 kV	Pass	A
Air Discharge – 15 kV	Pass	A

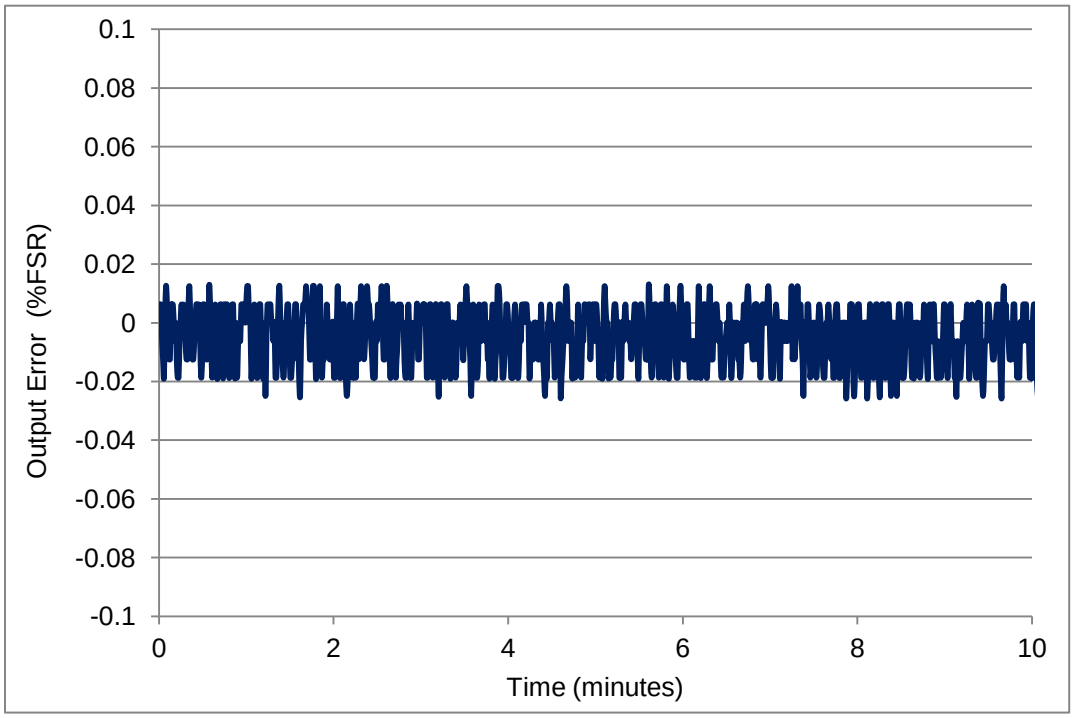


Figure 17: Module Output Error during ESD Tests

7.2 IEC 61000-4-3: Radiated EMI Immunity

Exposure to an electromagnetic field of 3 V/m caused some variation in the output of the module, especially at lower frequencies. However, the module never operated outside of the ±0.1% error range and was able to pass all conditions listed in Table 7. Figure 18 displays a capture of the output of the module during these tests. Installing the module inside the shielded paint can significantly reduced the variation at the output. After the testing was complete there was not a measurable deviation from the pre-test conditions.

Table 7. Radiated EMI Immunity Test Result – 3 V/m

Test	Result	Class
Vertical – Bare PCB	Pass	A
Vertical – Inside Paint Can	Pass	A
Horizontal – Bare PCB	Pass	A
Horizontal – Inside Paint Can	Pass	A

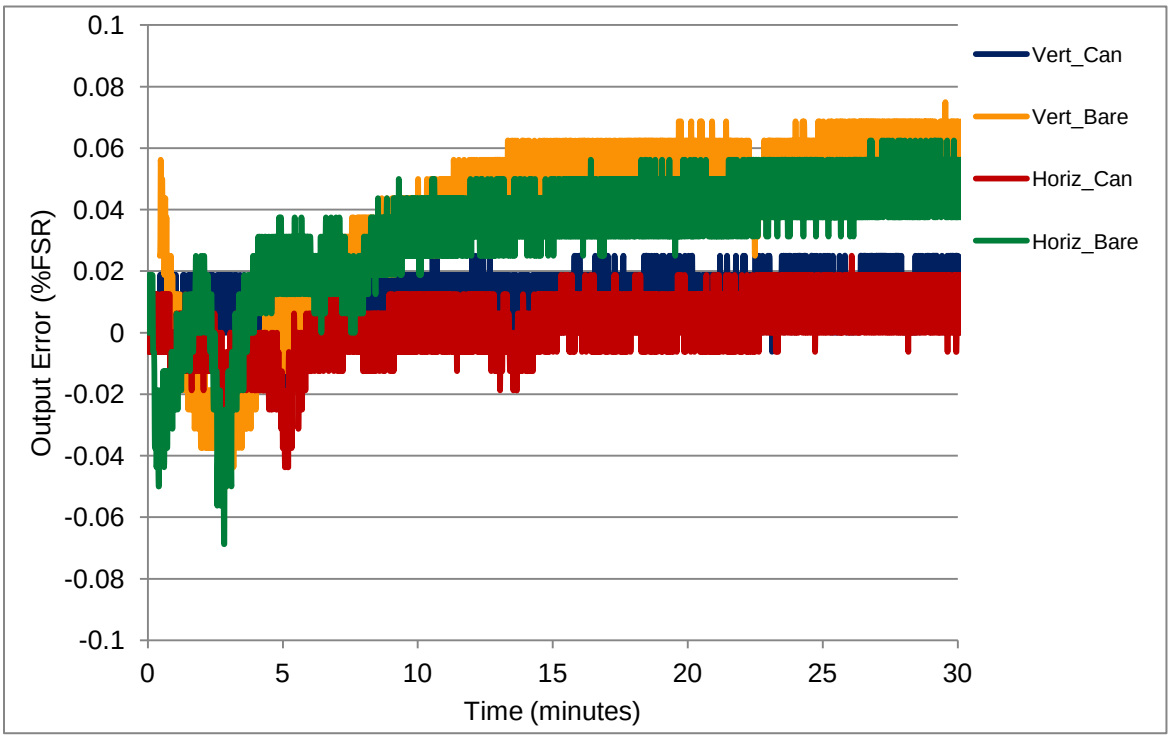


Figure 18: Radiated Immunity Test – 3 V/m

Exposure to an electromagnetic field of 10 V/m caused significant variation in the output of the module, especially at lower frequencies. In most tests the module operated outside the ±0.1% error range while the electromagnetic field was applied. However, after the testing was complete there was not a measurable deviation from the pre-test conditions and the module was able to pass all conditions listed in Table 8. Figure 19 displays a capture of the output of the module during these tests. Installing the module inside the paint can significantly reduced the variation at the output.

Table 8. Radiated EMI Immunity Test Result – 10 V/m

Test	Result	Class
Vertical – Bare PCB	Pass	B
Vertical – Inside Paint Can	Pass	B
Horizontal – Bare PCB	Pass	B
Horizontal – Inside Paint Can	Pass	A

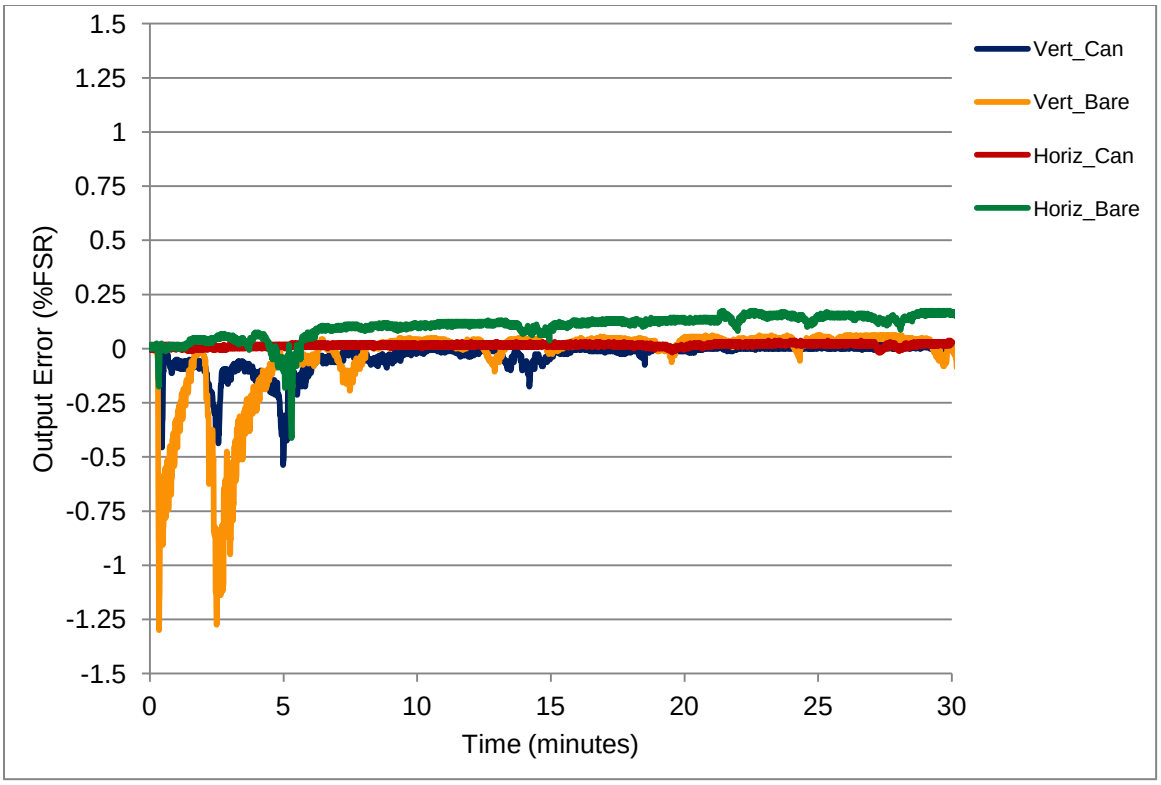


Figure 19: Radiated Immunity Test – 10 V/m

7.3 IEC 61000-4-4: EFT (Electrical Fast Transients)

EFT testing had little effect on the output of the module. It was able to maintain accurate performance across all conditions listed in Table 9. Figure 20 displays a capture of the output of the module during all of the EFT tests. As shown, at no point during the testing did the data deviate outside of the specified values. After the testing was complete there was not a measurable deviation from the pre-test conditions

Table 9. EFT Test Result

Test	Result	Class
2 kV – I/O and Power +	Pass	A
2 kV – I/O and Power -	Pass	A
4 kV – I/O and Power +	Pass	A
4 kV – I/O and Power -	Pass	A

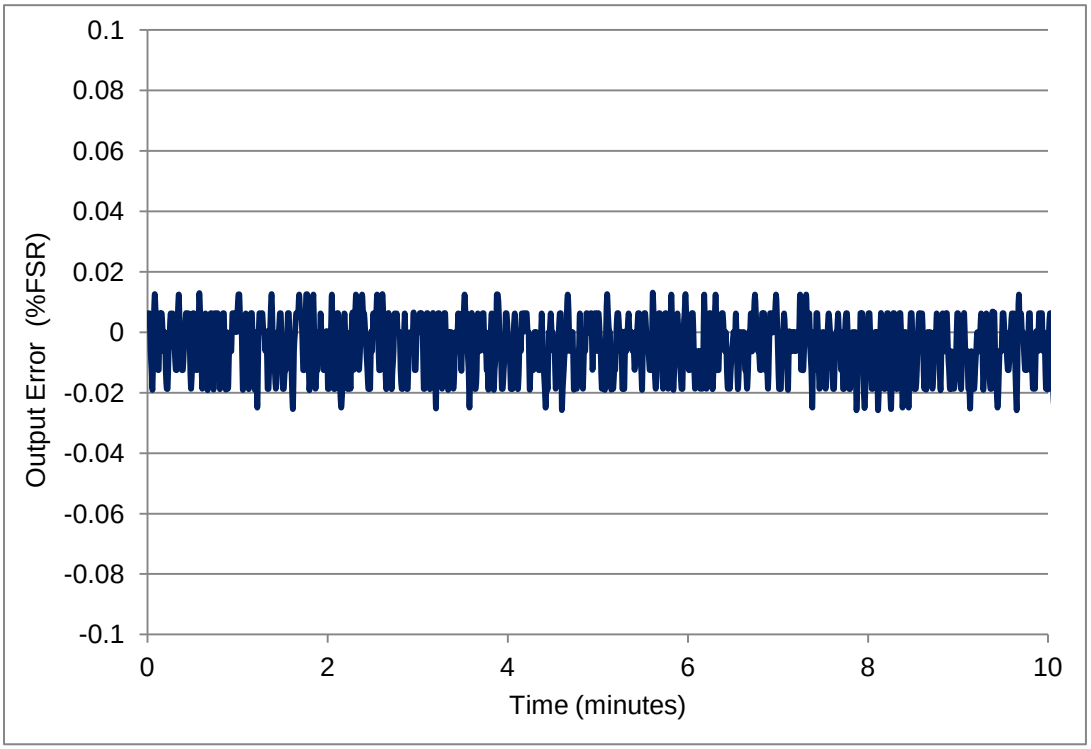


Figure 20: Module Output Error during EFT Tests

7.4 IEC 61000-4-5: Surge

The surge tests caused some dc offset and glitches at the output, but the module never operated outside of the ±0.1% error range and was able to pass all conditions listed in Table 10. Figure 21 displays a capture of the output of the module during all of the surge tests. After the testing was complete there was not a measurable deviation from the pre-test conditions.

Table 10. Surge Test Result

Test	Result	Class
500 V – I/O and Power	Pass	A
1 kV – I/O and Power	Pass	A
2 kV – I/O and Power	Pass	A
5 kV – I/O and Power	Pass	A

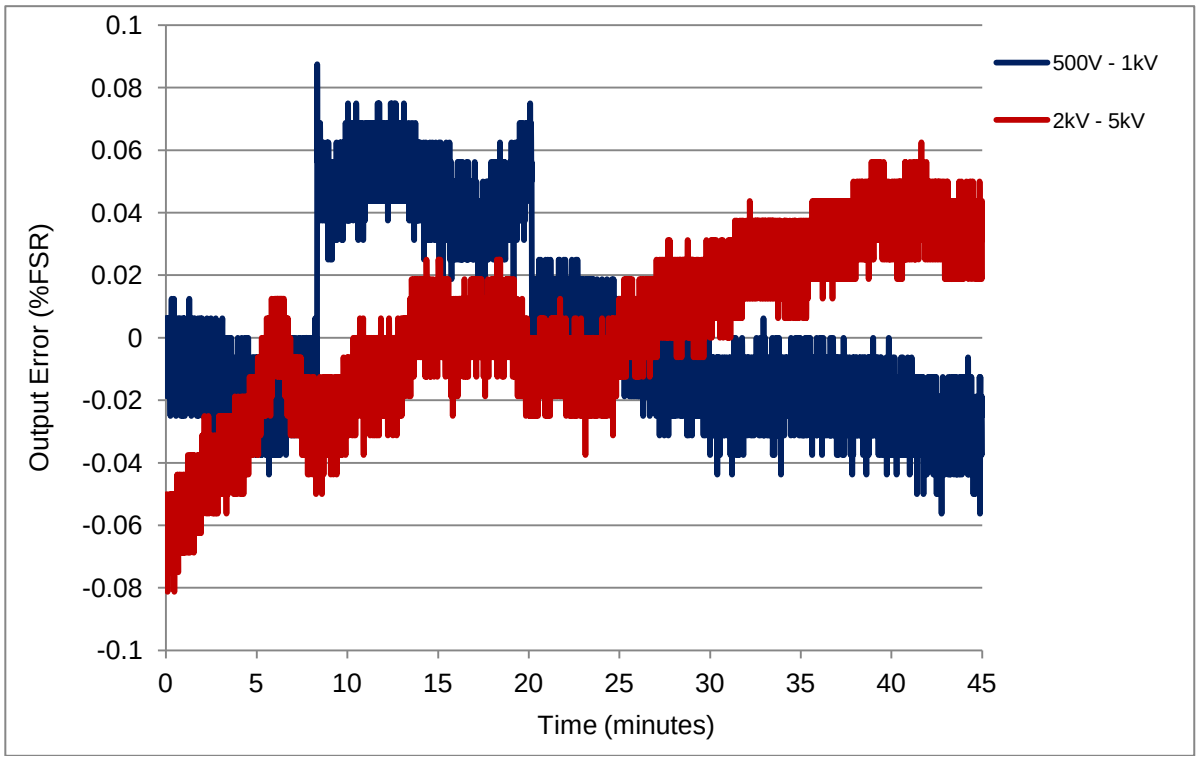


Figure 21: Module Output Error during Surge Tests

7.5 IEC 61000-5-6: Conducted EMI Immunity

The conducted EMI tests caused some variation at the output, but the module never operated outside of the ±0.1% error range and was able to pass all conditions listed in Table 11. Figure 22 displays a capture of the output of the module during these tests. After the testing was complete there was not a measurable deviation from the pre-test conditions.

Table 11. Conducted EMI Immunity Test Result

Test	Result	Class
10 V/m – I/O and Power	Pass	A

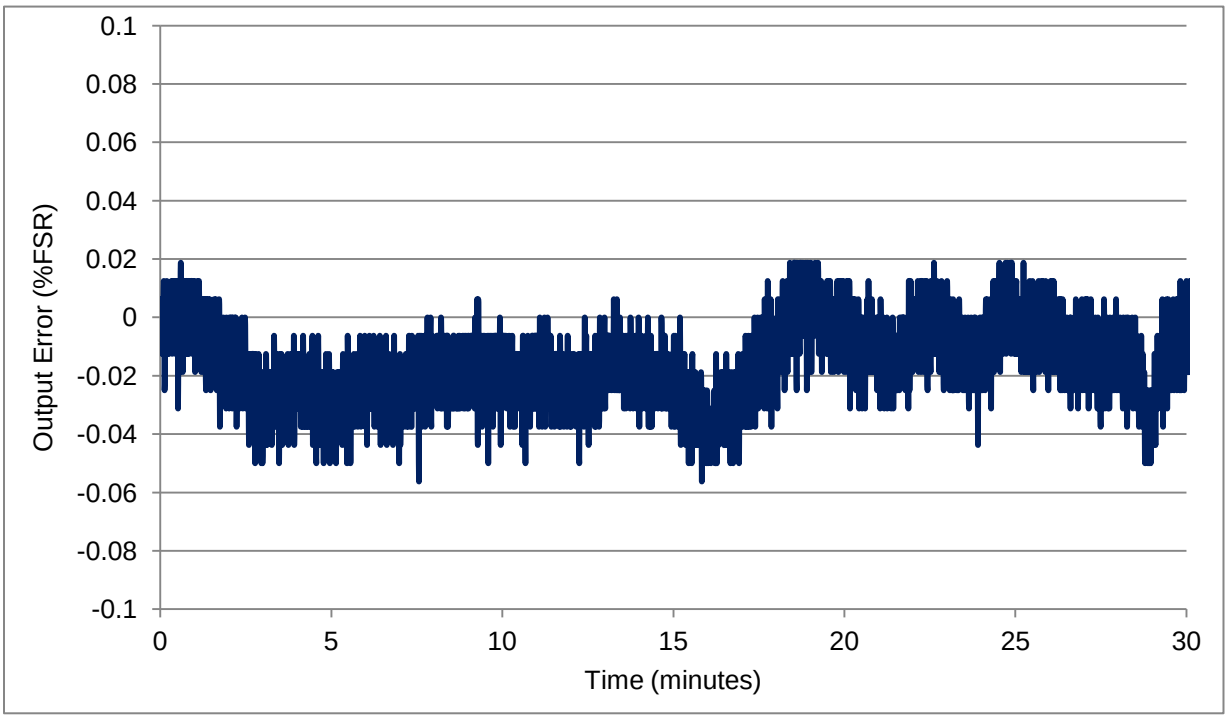


Figure 22: Module Output Error during Conducted EMI Immunity Tests

7.6 FCC Title 47, Section 15.109: Radiated EMI Emissions

This reference design module is primarily a dc system and does not radiate significant amounts of EMI. It easily passed all radiated EMI emissions tests against the FCC Class B standard.

Table 12. Radiated EMI Emissions Test Result

Test	Result	Class
Emissions – Vertical	Pass	FCC Class B
Emissions – Horizontal	Pass	FCC Class B

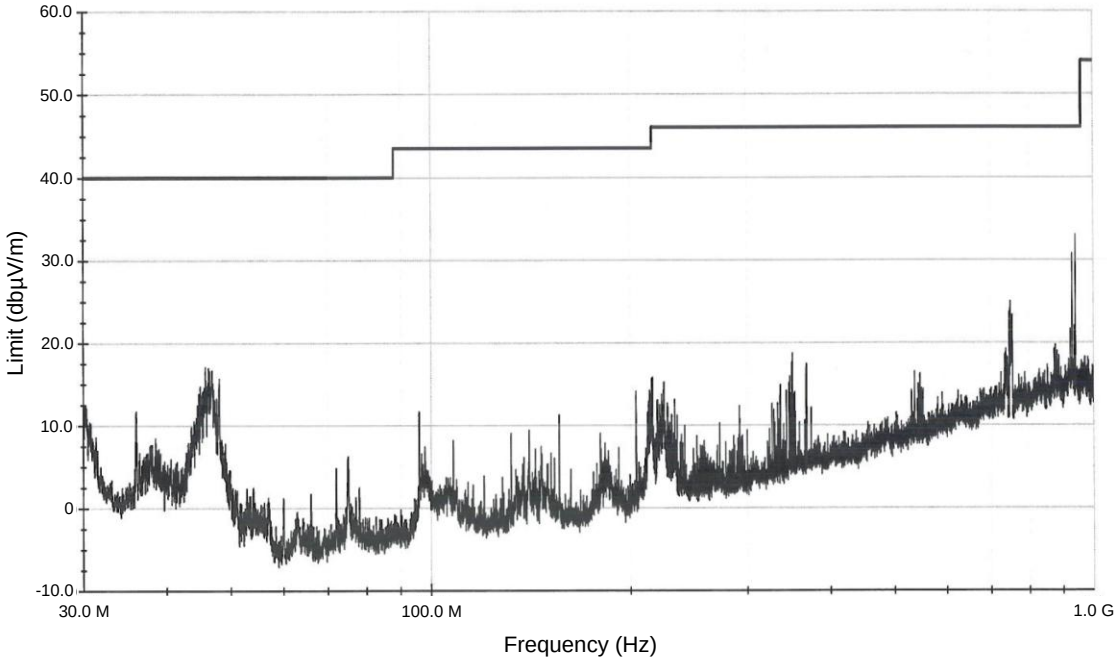


Figure 23: Radiated EMI Emissions Test - Vertical

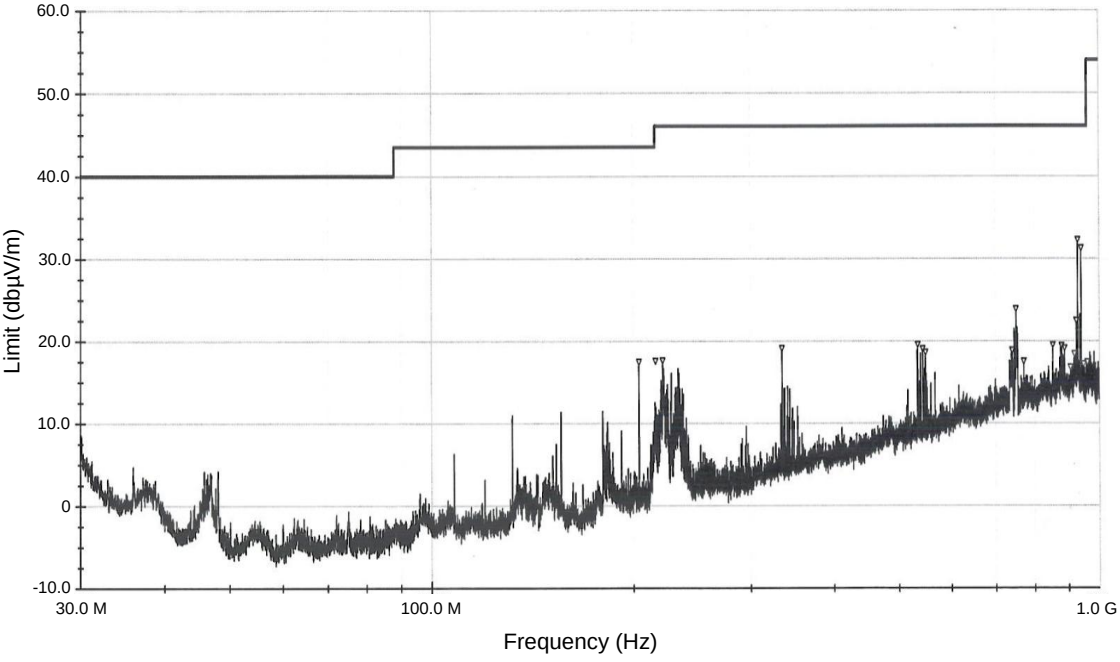


Figure 24: Radiated EMI Emissions Test - Horizontal

8 Modifications

The components selected for this design were based on the design goals outlined at the beginning of the design process.

Selecting a digitally calibrated signal conditioning device such as the PGA309 removes the dc errors normally attributed to the amplifier in this design. Although the zero-drift features of the PGA309 will allow for little change in its performance over temperature, the other resistors in the design may drift substantially over the full range of -40°C to 125°C. Therefore, if the design is meant to operate over a wide temperature range, it is recommended to choose low temperature coefficient and low tolerance components for the V-to-I conversion and filter resistors.

Cost may be a critical factor in some applications. It is also possible that the sensor is installed in a very stable thermal environment. For such an application, the PGA308 is a suitable choice. It is similar to the PGA309 in core function, but the linearization and temperature compensation circuitry is removed. It also includes seven banks of OTP (one-time programmable) non-volatile memory so there is no need for an external EEPROM – this helps reduce the size of the overall solution and decrease the total component cost.

Table 13 compares the PGA308 to the PGA309 as a potential signal conditioner for this design.

Table 13. Brief Comparison of Bridge Sensor Signal Conditioners

Signal Conditioner	Max Supply Voltage (V)	Sensor Linearization	Sensor Drift Compensation	Onboard Memory
PGA309	5.5	Yes	Yes	No (external EEPROM)
PGA308	5.5	No	No	Yes (7-bank OTP)

Table 14 summarizes the other potential current transmitters for this design as compared to the XTR117. The XTR115 and XTR116 are suitable choices for this system, with the differences being slightly higher dc precision, an additional internal voltage reference and higher cost. However, the higher precision of these devices is unnecessary since the entire system is calibrated, and the voltage reference is redundant as the PGA309 already includes a more precise reference.

Table 14. Brief Comparison of Current Transmitters

Current Transmitter	Max Supply Voltage (V)	V_{REF} Voltage (V)	Quiescent Current (µA)	Span Error Drift (ppm/°C)	Offset Voltage Drift (µV/°C)
XTR117	40	n/a	130	±3	±0.7
XTR116	36	4.096	200	±3	±0.7
XTR115	36	2.5	200	±3	±0.7

9 About the Authors

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10 Acknowledgements & References

10.1 Acknowledgements

The authors wish to acknowledge NTS (National Technical Systems) in Plano, TX for their assistance performing the electromagnetic compatibility tests.

10.2 References

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3. *IEC Publication 61000-4-3 "Electromagnetic Compatibility (EMC) – Part 4-3: Testing and Measurement Techniques – Radiated, Radio-Frequency, Electromagnetic Field Immunity Test," International Electrotechnical Commission, 2006.*

4. *IEC Publication 61000-4-4 "Electromagnetic Compatibility (EMC) – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test," International Electrotechnical Commission, 2012.*

5. *IEC Publication 61000-4-5 "Electromagnetic Compatibility (EMC) – Part 4-5: Testing and Measurement Techniques – Surge Immunity Test," International Electrotechnical Commission, 2009.*

6. *IEC Publication 61000-4-6 "Electromagnetic Compatibility (EMC) – Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields," International Electrotechnical Commission, 2008.*

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Appendix A.

A.1 Electrical Schematic

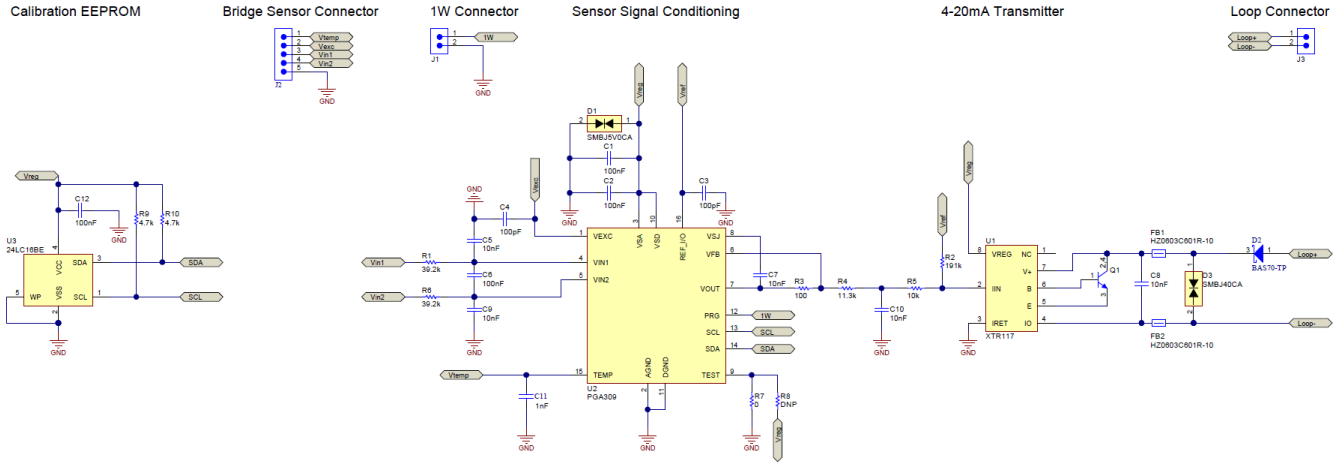

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item #	Quantity	Value	Designator	Description	Manufacturer	Part Number	Supplier Part Number
1	4	100nF	C1, C2, C6, C12	CAP CER 0.1UF 10V 10% X7R 0402	TDK Corporation	C1005X7R1A104K050BB	445-4958-1-ND
2	2	100pF	C3, C4,	CAP CER 100PF 50V 10% X7R 0402	Yageo	CC0402KRX7R9BB101	311-1419-1-ND
3	4	10nF	C5, C7, C9, C10	CAP CER 10000PF 10V 10% X7R 0402	Kemet	C0402C103K8RACTU	399-7759-1-ND
4	1	10nF	C8	CAP CER 10000PF 50V 10% X7R 0603	TDK Corporation	C1608X7R1H103K080AA	445-1311-1-ND
5	1	1nF	C11	CAP CER 1000PF 6.3V 10% X7R 0402	Kemet	C0402C102K9RACTU	399-8941-1-ND
6	2	39.2K	R1, R6	RES 39.2K OHM 1/10W 1% 0402 SMD	Panasonic Electronic Components	ERJ-2RKF3922X	P39.2KLCT-ND
7	1	191K	R2	RES 191K OHM 1/10W 1% 0402 SMD	Panasonic Electronic Components	ERJ-2RKF1913X	P191KLCT-ND
8	1	100	R3	RES 100 OHM 1/10W 1% 0402 SMD	Panasonic Electronic Components	ERJ-2RKF1000X	P100LCT-ND
9	1	11.3K	R4	RES 11.3K OHM 1/16W 0.1% 0402	TE Connectivity	4-1879215-1	A102592CT-ND
10	1	10K	R5	RES 10.0K OHM 1/16W 0.1% 0402	TE Connectivity	7-1879208-3	A102579CT-ND
11	1	0	R7	RES 0.0 OHM 1/10W 0402 SMD	Panasonic Electronic Components	ERJ-2GE0R00X	P0.0JCT-ND
12	1	N/A	R8	DNP, 0402	N/A	N/A	N/A
13	2	4.7K	R9, R10	RES 4.70K OHM 1/10W 1% 0402 SMD	Panasonic Electronic Components	ERJ-2RKF4701X	P4.70KLCT-ND
14	2	FERRITE BEAD	FB1, FB2	FERRITE 300MA 600 OHM 0603 SMD	Laird-Signal Integrity Products	HZ0603C601R-10	240-2380-1-ND
15	1	TVS	D1	TVS BIDIRECT 600W 5V SMB	Fairchild Semiconductor	SMBJ5V0CA	SMBJ5V0CACT-ND
16	1	SCHOTTKY	D2	DIODE SCHOTTKY 70V 70MA SOT23	Micro Commercial Co	BAS70-TP	BAS70TPMSCT-ND
17	1	TVS	D3	TVS BIDIRECT 600W 40V SMB	Fairchild Semiconductor	SMBJ40CA	SMBJ40CAFSCT-ND
18	1	NPN	Q1	TRANSISTOR NPN 45V 2000MA SOT-89	Diodes Inc	FCX690BTA	FCX690BCT-ND
19	1	XTR117	U1	XTR117	Texas Instruments	XTR117AIDGKT	296-18744-1-ND
20	1	PGA309	U2	PGA309	Texas Instruments	PGA309AIPWR	296-16726-1-ND
21	1	EEPROM	U3	IC EEPROM 16KBIT 400KHZ SOT23-5	Microchip Technology	24LC16BHT-I/OT	24LC16BHT-I/OTCT-ND
22	2		J1, J3	CONN HEADER 2POS .100" T/H GOLD	Samtec Inc	HTSW-102-07-G-S	HTSW-102-07-G-S-ND
23	1		J2	CONN HEADER 5POS .100" T/H GLD	Samtec Inc	HTSW-105-07-G-S	HTSW-105-07-G-S-ND

Figure A-2: Bill of Materials

Appendix B.

B.1 Certification Testing General Information

The EMC certification testing performed on this reference design follows the standards set by two entities: the IEC (International Electrotechnical Commission) and the FCC (Federal Communications Commission).

The IEC is a worldwide organization which promotes international cooperation on issues of standardization in electrical and electronic systems. They have developed a set of transient and EMI immunity standards which have become the minimum requirements for manufacturers wanting to do business in the European Community and around the world. The standards which are applicable to this reference design are known as IEC 61000-4.

The FCC is the authority on communications technology in the United States that creates and enforces the use of airwaves throughout the entire radio frequency spectrum. They have defined a set of limits for the amount of radiated emissions which may be transmitted from an electronic device, which are given in the Code of Federal Regulations.

In general, a device may achieve one of four classes of performance for each test.

Table B-1: EMC Test Performance Classes

Class	Description
A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance without operator intervention.
C	Temporary loss of function or degradation of performance, the correction of which requires operation intervention.
D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

B.2 IEC 61000-4-2: ESD (Electrostatic Discharge)

ESD (Electrostatic discharge) is one of the most common forms of transients in electronic systems. ESD results from conditions which allow the buildup of electrical charge from contact and separation of two non-conductive materials. When the charged body is brought in proximity of another object of lower potential, energy is released in the form of ESD.

IEC 61000-4-2 defines four threat levels which depend on material type, ambient humidity, and expected amount of handling. Level 1 is the least severe while level 4 is the most severe. IEC 61000-4-2 also specifies the parameters of the current waveform associated with the ESD.

Table B-2: IEC 61000-4-2 Severity Levels and Test Voltages

Threat Level	Relative Humidity As Low As (%)	Material Type	Maximum Charge Voltage (kV)	Test Voltage – Contact Discharge (kV)	Test Voltage – Air Discharge (kV)
1	35	Antistatic	2	2	2
2	10	Antistatic	4	4	4
3	50	Synthetic	8	6	8
4	10	Synthetic	15	8	15

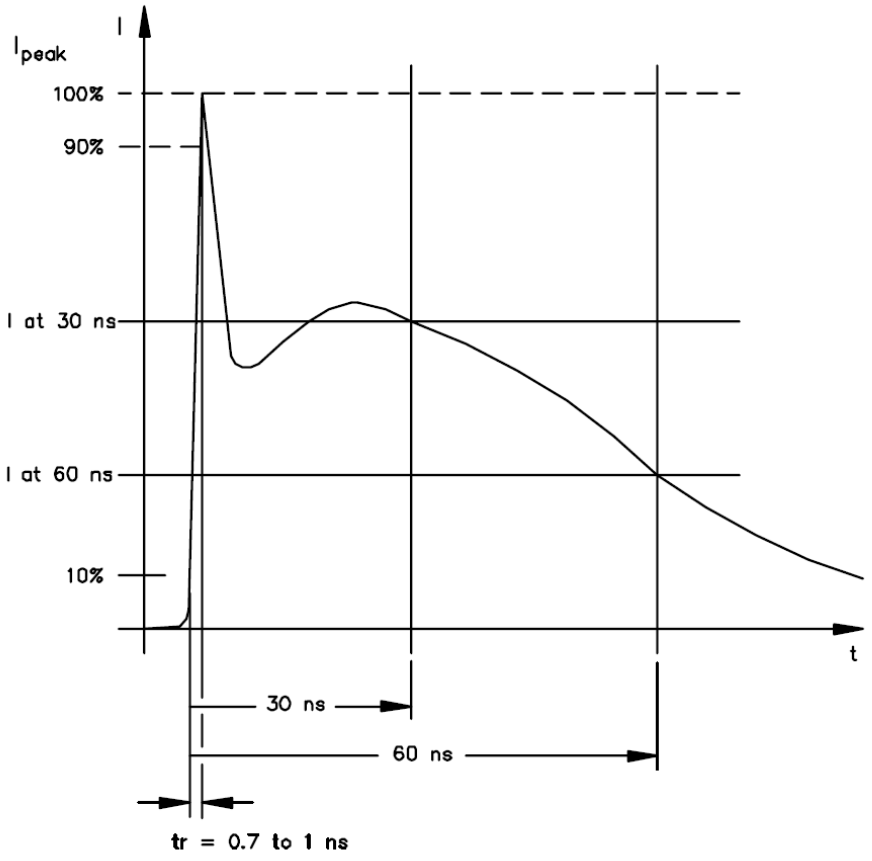

Figure B-1: IEC 61000-4-2 ESD Current Waveform [7]

Table B-3: IEC 61000-4-2 Waveform Parameters

Threat Level	Indicated Voltage (kV)	First Peak Current of Discharge ±10% (A)	Rise Time with Discharge Switch (ns)	Current (±30%) at 30 ns (A)	Current (±30%) at 60 ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Figure B-2 illustrates the test hardware setup for the different ESD tests. Typically four tests are performed:

1. Indirect discharge to VCP (Vertical Coupling Plane): The device under test is placed 10 cm away from a vertically-oriented metal plane. ESD is discharged ten times to the side of the plane.
2. Indirect discharge to HCP (Horizontal Coupling Plane): The device under test is placed on an insulating mat, which is on a table with a horizontal metal plane. ESD is discharged ten times on the side of the plane.
3. Air discharge: ESD is discharged ten times approximately 1 cm from the device under test.
4. Contact discharge: The tip of the ESD generator is placed in contact with the device under test. ESD is discharged ten times.

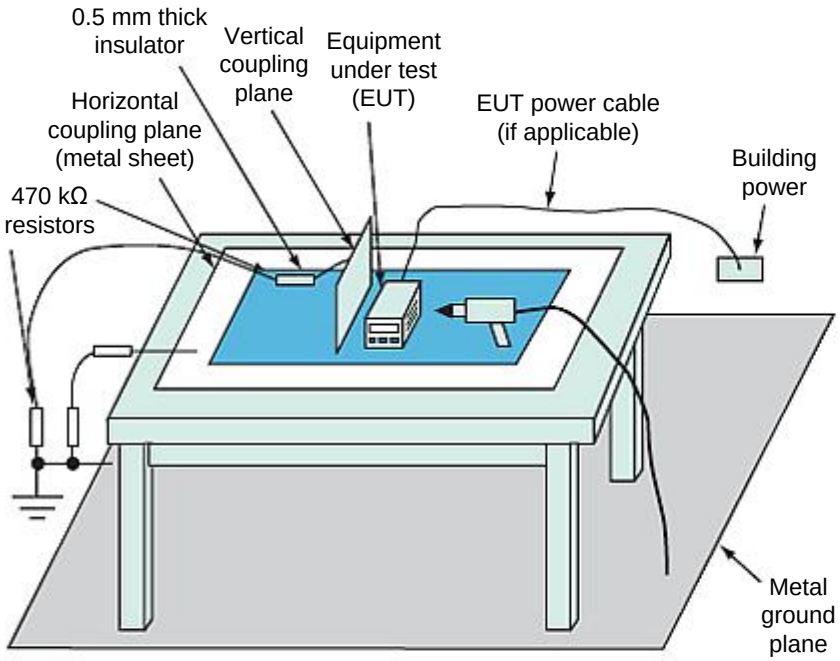

Figure B-2: IEC 61000-4-2 ESD Test Hardware Setup [2]

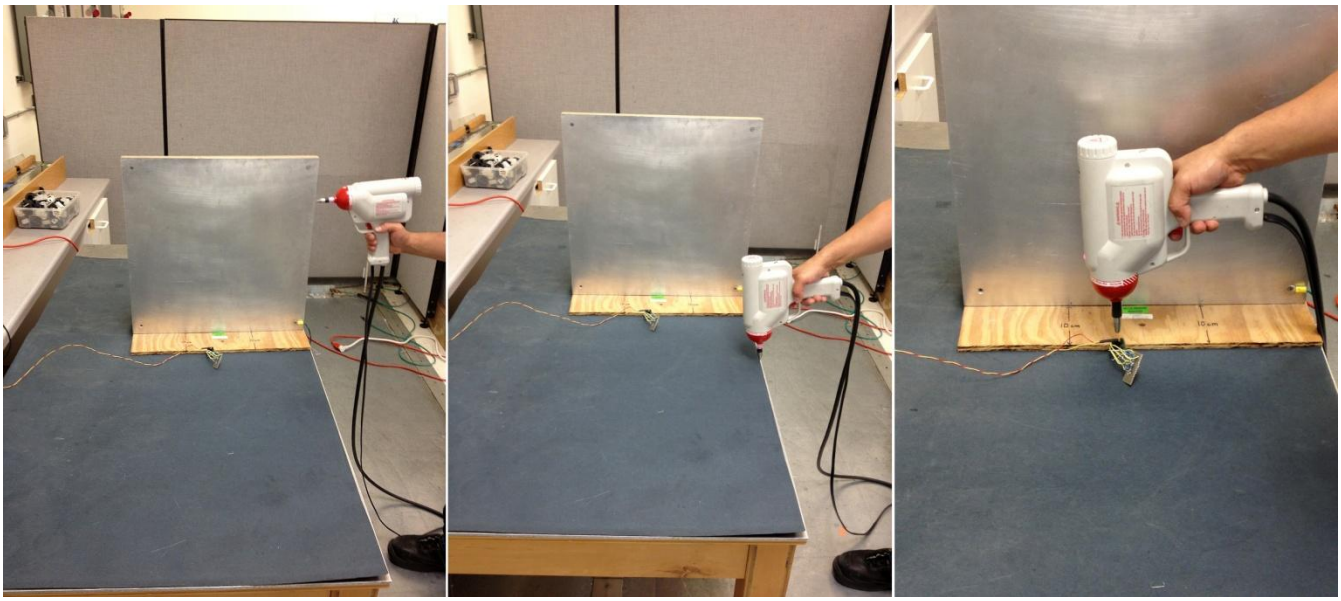

Figure B-3: IEC 61000-4-2 ESD Tests – VCP, HCP, Air Discharge

B.3 IEC 61000-4-3: Radiated EMI (Electromagnetic Interference) Immunity

Electronic products are often installed in locations near RF (radio frequency) transmitters. These transmitters create electromagnetic fields which can have a significant impact on the functionality of other electronics. The IEC 61000-4-3 standard relates to the radiated immunity requirements of electrical and electronic equipment to disturbances coming from RF transmitters in the frequency range of 80 MHz to 1 GHz.

Table B-4: IEC 61000-4-3 Test Levels

Level	Test Field Strength (V/m)
1	1
2	3
3	10
4	30
x	Special
Note: x is an open test level and the associated field strength may be any value.	

The test is performed inside a shielded, anechoic chamber which must be large enough to maintain a uniform field with respect to the device under test. RF absorbers are used to damp reflections in the chamber. An RF signal generator, often controlled by software, creates the test signals which are amplified by a power amplifier and transmitted by a field generating antenna. The antenna can be set to vertical and horizontal orientations.

The device under test is placed on an insulated wooden table a fixed distance away from the antenna. The table sits on a motorized turntable which allows the device under test to be rotated. A field sensor is placed adjacent to the device under test in order to calibrate and monitor the intensity of the electromagnetic field.

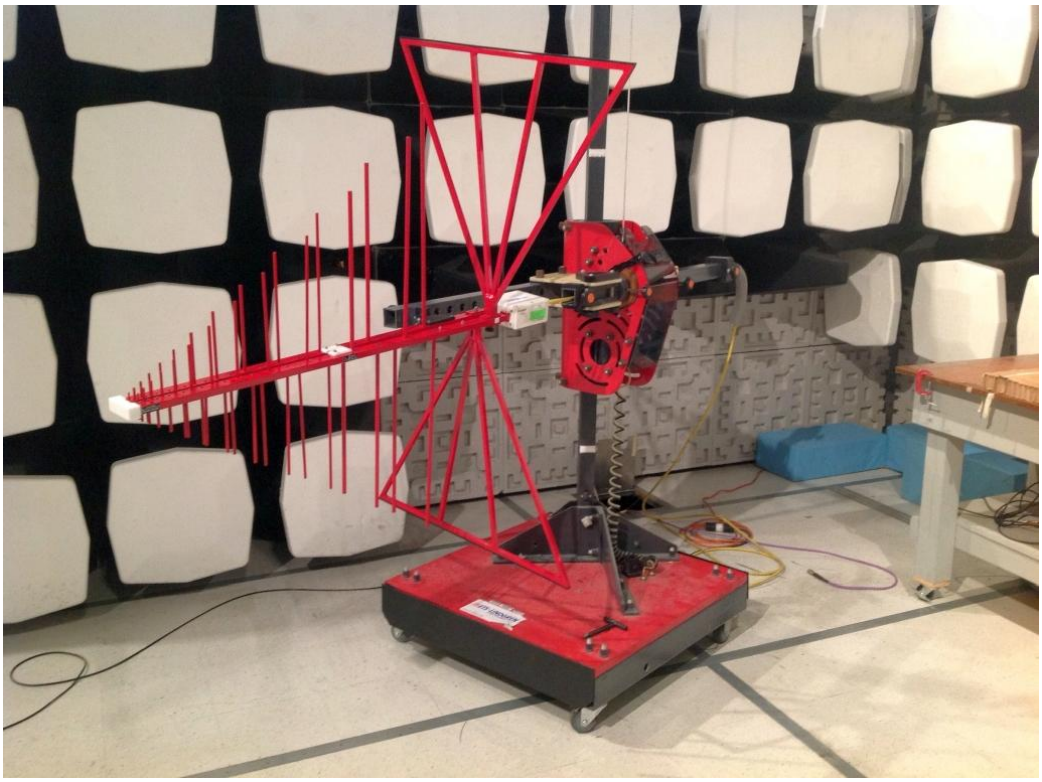

Figure B-4: Log-Periodic Dipole Antenna – Vertical Orientation

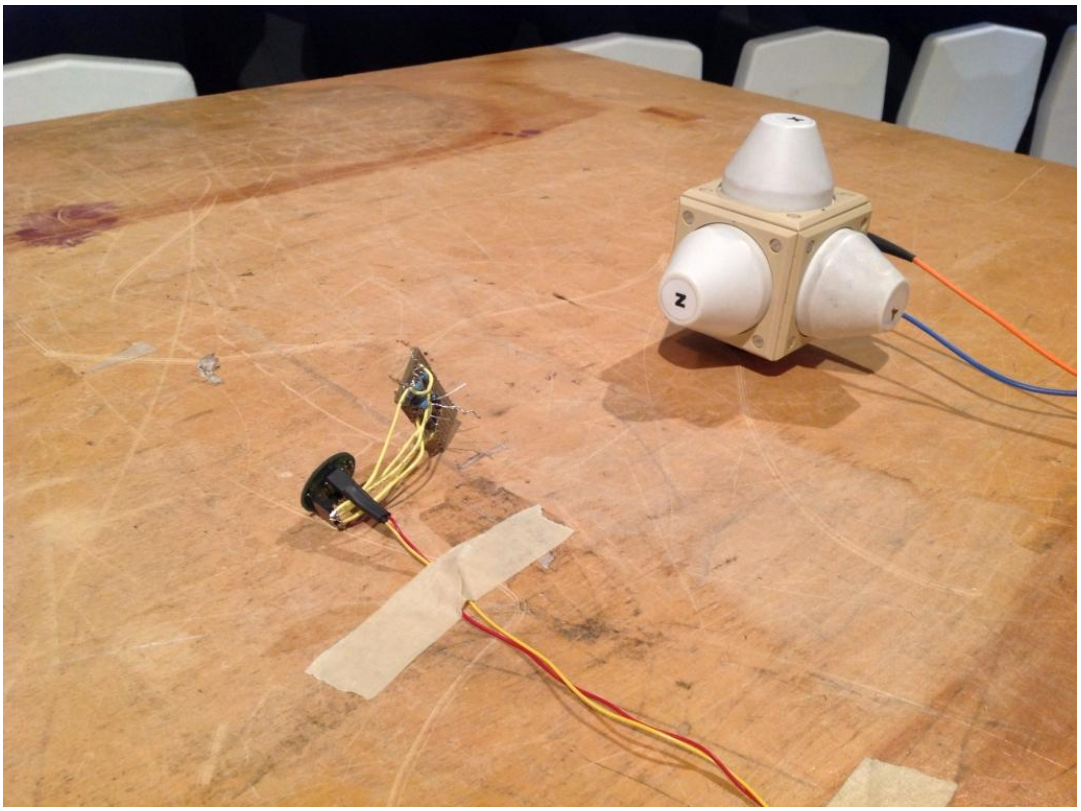

Figure B-5: Device under Test (with Sensor Test Board) and Field Sensor

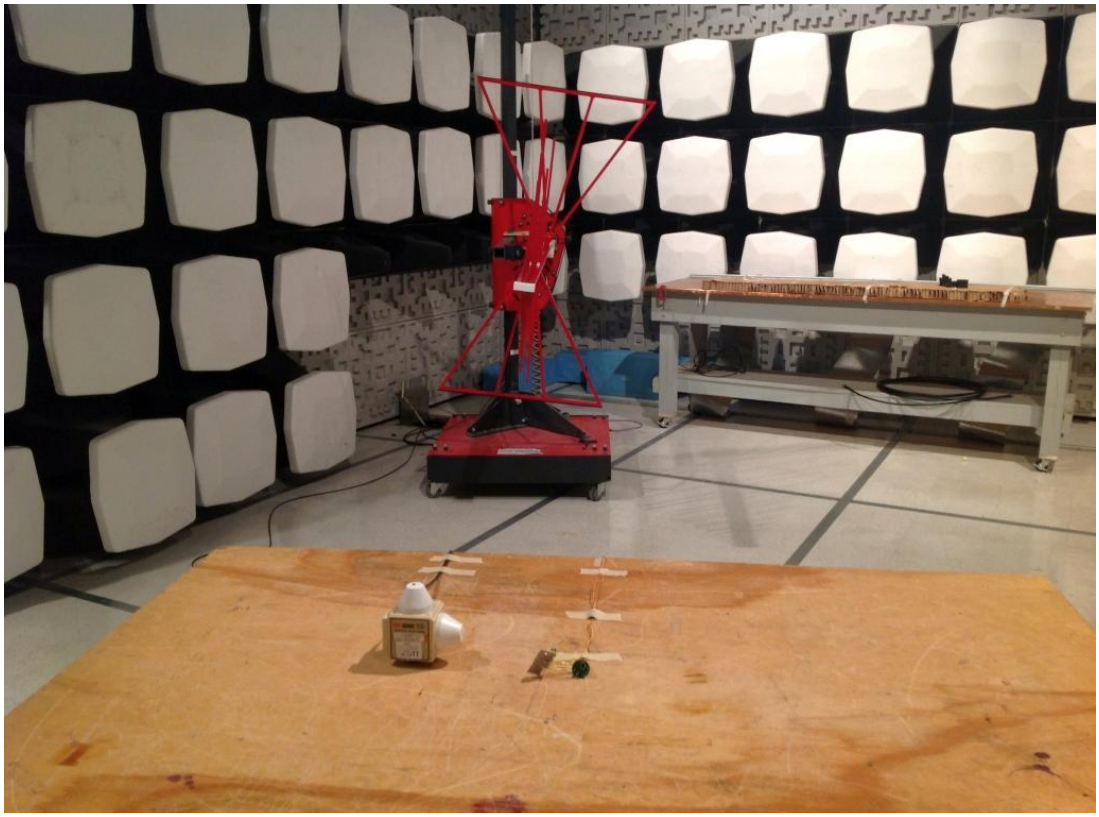

Figure B-6: IEC 61000-4-3 Full Test Chamber Setup

B.4 IEC 61000-4-4: EFT (Electrical Fast Transients)

EFT (electrical fast transients) occur as a result of arcing contacts in switches and relays, and are very common in industrial environments using electromechanical switches to connect and disconnect inductive loads. IEC 61000-4-4 specifies the EFT threat in both power and data lines.

Table B-5: IEC 61000-4-4 Severity Levels and Test Voltages

	Power Supply Port		I/O, Signal, Data and Control Lines	
Threat Level	Open-Circuit Voltage (kV)	Short-Circuit Current (A)	Open-Circuit Voltage (kV)	Short-Circuit Current (A)
1	0.5	10	0.25	5
2	1	20	0.5	10
3	2	40	1	20
4	4	80	2	40

The EFT waveform is described in terms of a voltage across a 50 Ω load from a generator having a nominal dynamic source impedance of 50 Ω. The output occurs as a burst of high voltage spikes at a repetition rate ranging from 2 kHz to 5 kHz. The burst length is defined as 15 ms with bursts repeated every 300 ms. Each individual burst pulse has a rise time of 5 ns and a total duration of 50 ns.

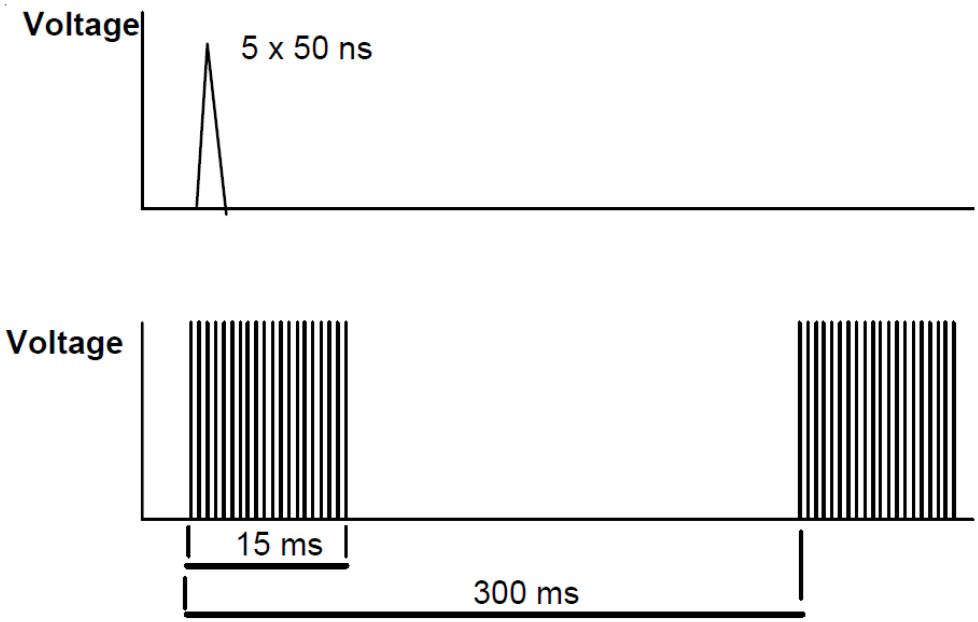

Figure B-7: IEC 61000-4-4 EFT Voltage Waveform [7]

During the EFT test, the device under test is connected to its power supply with 3m of cable and placed on a small wooden platform. Part of the cable passes through a special trough with wooden side panels and a triangular metallic inner chamber. The EFT generator is connected to the metallic chamber of the trough and the test waveform is applied. The EFT waveform can then couple to the device under test's power supply cable.

Figure B-8: IEC 61000-4-4 EFT Test Hardware Setup

B.5 IEC 61000-4-5: Surge

The most severe transient conditions on power and data lines are surges caused by lightning strikes and switching. Switching transients include power system switching, load changes, and short circuit faults. Lightning transients may result from a direct strike or induced voltages and currents due to an indirect strike.

The IEC 61000-4-5 standard defines a transient entry point and a set of installation conditions. The transient is defined in terms of a generator producing a given waveform and having a specified open circuit voltage and source impedance. Two surge waveforms are specified: the 1.2 x 50 µs open-circuit voltage waveform and the 8 x 20 µs short-circuit current waveform.

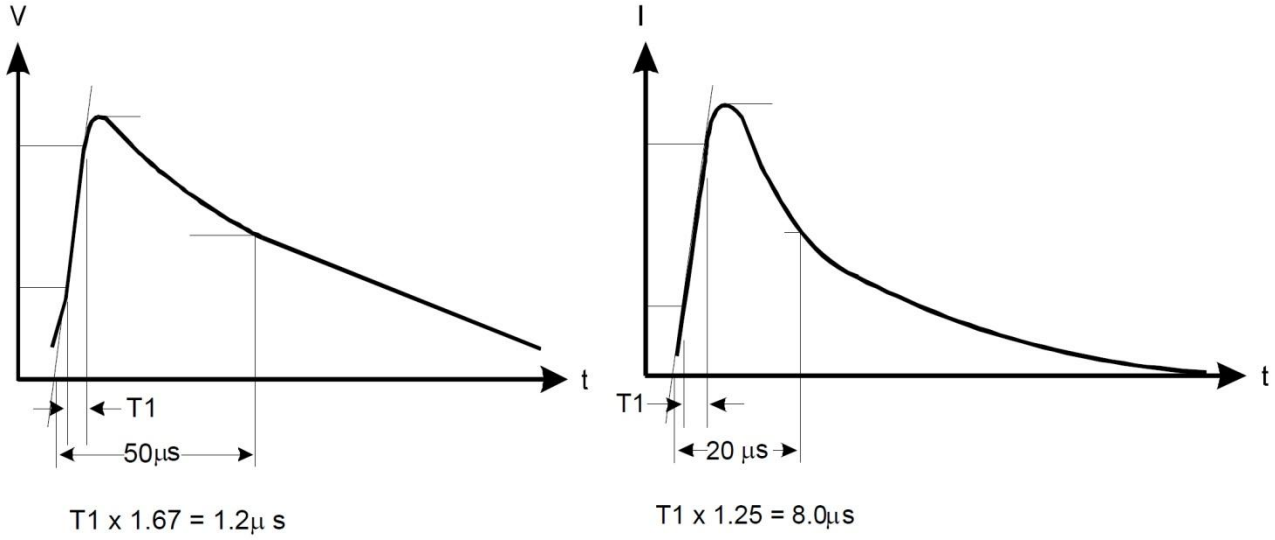

Figure B-9: IEC 61000-4-5 Surge Waveforms [7]

Table B-6: IEC 61000-4-4 Severity Levels and Test Voltages

Threat Level		Power Supply		Unsym Lines (Long Distance Bus)		Sym Lines	Data Bus (Short Distance)
		Coupling Mode		Coupling Mode		Coupling Mode	Coupling Mode
		Line-Line Z_S = 2Ω	Line-GND Z_S = 12Ω	Line-Line Z_S = 42Ω	Line-GND Z_S = 42Ω	Line-GND Z_S = 42Ω	Line-GND Z_S = 42Ω
1	Voltage	n/a	0.5 kV	n/a	0.5 kV	1 kV	n/a
	Current	n/a	42 A	n/a	12 A	24 A	n/a
2	Voltage	0.5 kV	1 kV	0.5 kV	1 kV	1 kV	0.5 kV
	Current	250 A	83 A	12 A	24 A	24 A	12 A
3	Voltage	1 kV	2 kV	1 kV	2 kV	2 kV	n/a
	Current	500 A	167 A	24 A	48 A	48 A	n/a
4	Voltage	2 kV	4 kV	2 kV	4 kV	n/a	n/a
	Current	1 kA	333 A	48 A	95 A	n/a	n/a
5	Voltage	Varies	Varies	2 kV	4 kV	4 kV	n/a
	Current	Varies	Varies	48 A	95 A	95 A	n/a
Waveforms	Voltage	1.2 x 50 µs	1.2 x 50 µs	1.2 x 50 µs	1.2 x 50 µs	1.2 x 50 µs	1.2 x 50 µs
	Current	8 x 20 µs	8 x 20 µs	8 x 20 µs	8 x 20 µs	8 x 20 µs	8 x 20 µs

For the surge test, the device under test is placed on a small wooden platform and connected to its power supply through a robust LC filter network. The surge generator is connected to the capacitors of the LC filter, allowing the device under test to be exposed to surge conditions while protecting the power supply.

The surge voltage is tested at both positive and negative polarities. Connections are made using all possible combinations across the device under test's power supply terminals, both differentially and common-mode.

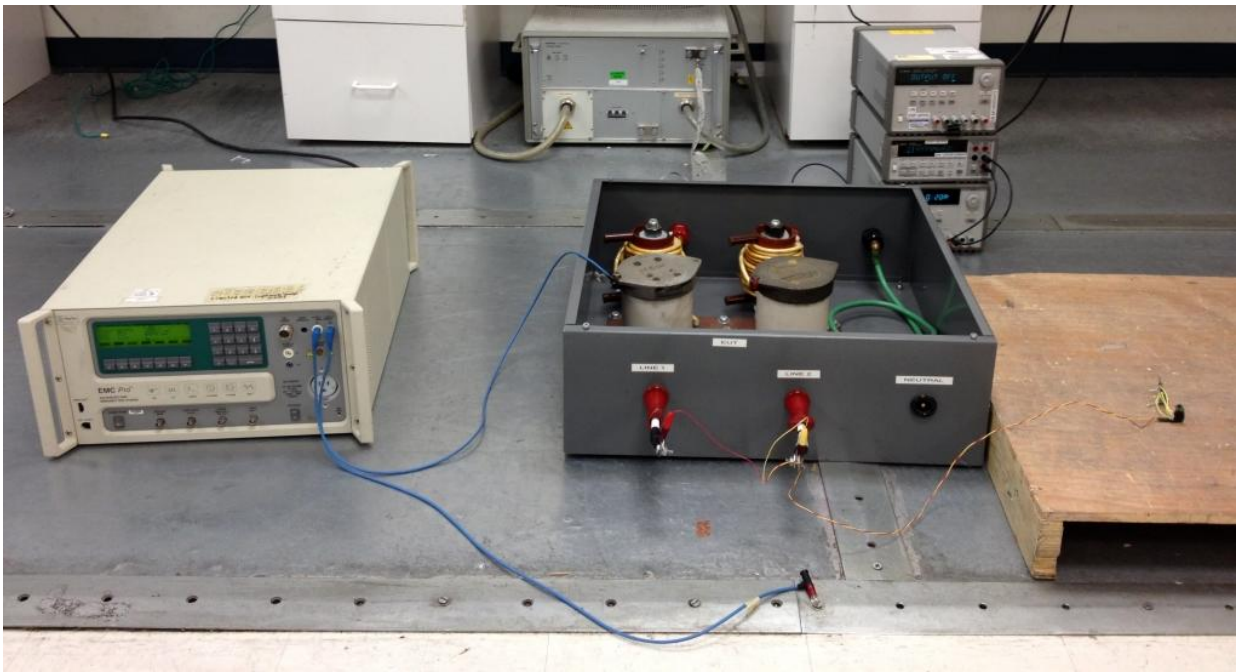

Figure B-10: IEC 61000-4-5 Surge Test Hardware Setup

B.6 IEC 61000-4-6: Conducted EMI Immunity

Electronic products are often installed in locations near RF (radio frequency) transmitters. These transmitters create electromagnetic fields which can have a significant impact on the functionality of other electronics. The IEC 61000-4-6 standard relates to the conducted immunity requirements of electrical and electronic equipment to disturbances coming from RF transmitters in the frequency range of 15 kHz to 80 MHz.

The principle of the test is to excite an electromagnetic disturbance field within the device under test by applying the RF stress to certain cables entering it. The device's cables are run through a circular injection probe which applies the test field, and another probe monitors the intensity of the field.

Table B-7: IEC 61000-4-6 Test Levels

Product Type	Electric Field (V/m)	Frequency Range (MHz)	Amplitude Modulation Depth (%)	Amplitude Modulation Frequency (kHz)
Residential, Commercial, Light Industrial	3	0.15 – 80	80	1
Industrial	10	0.15 – 80	80	1

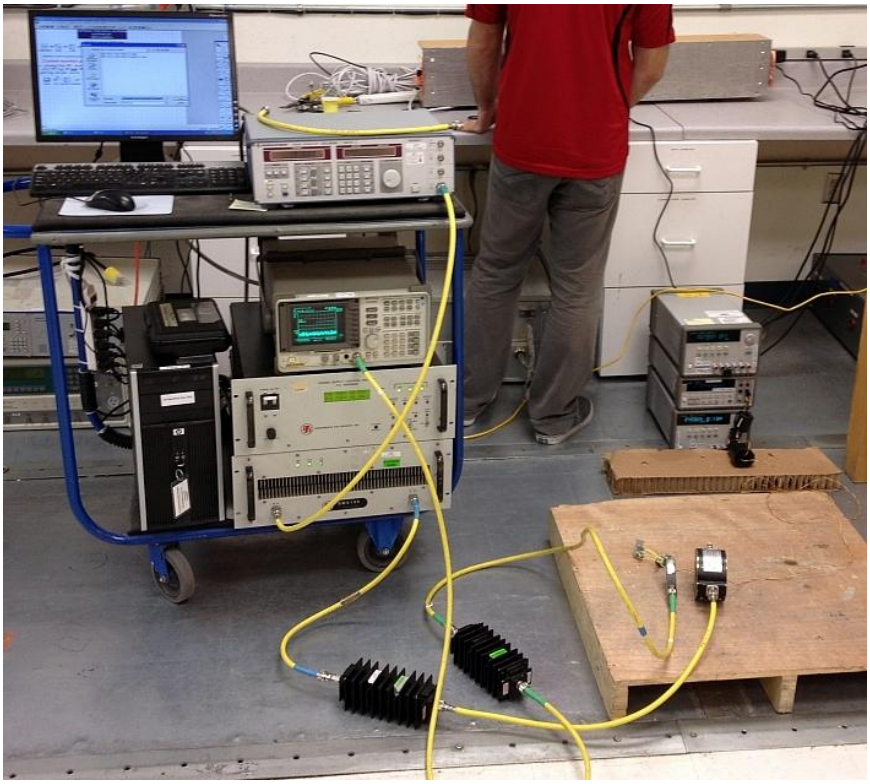

Figure B-11: IEC 61000-4-6 Conducted EMI Immunity Test Hardware Setup

B.7 FCC Title 47, Section 15.109: Radiated Emission Limit

The FCC (Federal Communications Commission) has specified a limit to the amount of EMI which can be radiated by an electronic device. This standard is intended to help maintain lower levels of radiated interference in order to reduce problems caused by radiative coupling.

This test is performed in the same type of anechoic chamber as the radiated EMI immunity test described in Section 9.2.2. However, for this test the device under test acts as the EMI transmitter and the test chamber's antenna is configured as a receiver. The antenna measures the intensity of the electric field at a specified distance away from the device under test.

Table B-8: FCC Radiated Emissions Limits

Frequency Range	Class A Devices at 10m (dBµV/m)	Class B Devices at 3m (dBµV/m)
30 – 88 MHz	39.1	40.0
88 – 216 MHz	43.5	43.5
216 – 960 MHz	46.4	46.0
> 960 MHz	49.5	54.0

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