Application Report

Long-Term Drift in Voltage References

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Long-Term Drift in Voltage References

Multiple industrial applications, such as grid monitoring and remote field sensors, require instrumentation that operates with high precision over a long period of time. For such use cases with long life times, the Long-Term Drift (LTD) parameter of voltage references, becomes critically important. This application note describes the Long-Term Drift parameter, factors which affect it, how it is measured and gives sample profiles of some of the TI precision voltage references.

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1 Long-Term Drift

The reference voltage is a critical component in a signal chain and can impact the performance if careful consideration not provided to various the error sources. The output of the voltage reference varies depending on the temperature, input voltage, load current, and time. This application note focuses on deviations of the output voltage over time due to aging known as Long-Term Drift (LTD) or long-term stability. LTD is a key parameter in industrial and automotive applications where a system will not experience regular calibration over its lifetime. The error from LTD can dominate all other errors over time. Therefore, it is important to understand how the parameter is tested and specified for the data sheet.

2 Long-Term Drift Data Sheet Measurement

Long term drift (LTD) for voltage references give insight of its output behavior over long period of time in a quantitative manner. Long-Term Drift Equation shows how Long-Term Drift is typically defined in a data sheet electrical characteristics table.

$$\mathrm{LTD}_{tn}(\mathrm{ppm}) = \frac{(\mathrm{VOUT}_{t0} - \mathrm{VOUT}_{tn})}{\mathrm{VOUT}_{t0}} \times 10^{6} \qquad (1)$$

Where:

- VOUT_{t0} = Output voltage at the start of measurement. This is done right after soldering.
- VOUT_{tn} = Output voltage at n^{th} hour

During this measurement the reference was powered up for n hours.

The resulting value is then captured in the data sheet in Figure 2-1 based on the amount of time tested and measured. LTD is not production tested; therefore the value specified is a typical value that will have variation across devices. Examples of variations can be found in the typical characteristic graphs in the data sheet. This table shows two LTD values based on two time subdivisions from the same continuous test for the DBV package, the first 1000 hours and the subsequent 1000 hours for a total of 2000 hours.

Long-term stability	DBV package	0 – 1000 hours at 35°C	25	ppm
		1000 – 2000 hours at 35°C	10	
	DGK package	0 – 1000 hours at 35°C	25	

Figure 2-1. Long-Term Drift Data Sheet Table Example for REF34-Q1

The LTD specification in the electrical characteristics table can be used for generic error calculations but the graphs in the data sheet show the actual trend over time. The graphs illustrate that the drift is not consistent in value or direction from unit to unit but generally the drift slows over time. The LTD primarily comes from the mechanical stress and aging, so as the packaging, bonding and die materials settle over time, the drift will slow down.

3 Long-Term Drift Error

Multiple applications demand that the systems will operate without periodic calibration for long periods of time. In these situations then LTD can be one of the dominant contributors in the error budget. REF34-Q1 Gain Error Breakdown illustrates a comparison between errors of the REF34-Q1. For more details on all error sources of a voltage reference, see the *Voltage Reference Design Tips For Data Converters Application Note*.

Table 3-1. REF34-Q1 SOT23-3 Error Breakdown

Parameter	Error (ppm)	Source	Notes	Error Reduction Method	% of Total (No Calibration)	% of Total (With Initial Calibration)
Initial accuracy	500	Data sheet maximum value		Calibration at 25°C	27.4%	0%
Solder shift	100	Data sheet typical value		Calibration at 25°C	5.49%	0%
Temperature drift	990	Data sheet maximum value	6ppm/C × (125 – (-40))°C = 990 ppm	Calibration across temperature	54.3%	80.9%
Long-Term Drift	234	Data sheet typical value	Conservative estimate based on 10 yr value	LTD shift = 25 × sqrt(hr/1000)	12.8%	19.1%

In this example the LTD is the third highest error at 234 ppm without calibration in situations where the life cycle of the system is very long due to the low LTD of the REF34 in SOT23-3. Initial calibration can be implemented in the signal chain which reduces the error of the voltage reference at the temperature it was calibrated at. In REF34-Q1 Gain Error Breakdown the initial calibration reduces the error that exists at 25°C and post solder shift. LTD becomes the second highest error if there is initial calibration. The 10 year LTD value was calculated using the typical value using an equation which results with a conservative value.

The primary reason for change in output voltage over time for the same temperature and electrical conditions (supply voltage, load) is change in the stress on the voltage reference die. The Piezo junction effect explains that mechanical stress on band gap changes base to emitter voltage (VBE) of transistor and resistors which results in drift in the output voltage of the reference. Package, mold compound, PCB design and moisture in the environment are key contributing factors for this stress change.

4 Package and Mold Compound Stress

In plastic package assembly, the die is mounted on the die pad using an epoxy and the pins are bonded out to the leadframe as shown in Figure 4-1. Afterwards, a liquid mold compound material fills the package mold to create the package. The mold compound cools down to from a liquid to a solid state and then packaged device is cut down from the base. Due to the curing process, the mold compound settles over time and hence total stress on the die also changes over the time which causes drift in output voltage. The package compound, assembly, and any component that can cause stress on the die will affect the Long-Term Drift.

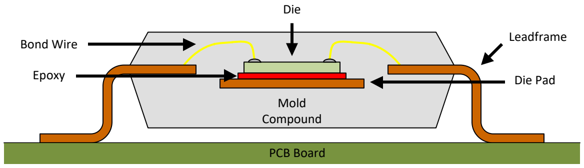

Figure 4-1. Leadframe Cross Section

A lower LTD is observed when a larger package is used for the same die. The stress on the device changes in lesser proportion in larger die package compare to small die resulting in lower LTD. For this example, the REF34 in VSSOP is a larger package and it has better LTD than the REF34 in SOT23-6 due to the VSSOP adding less stress to the REF34 die.

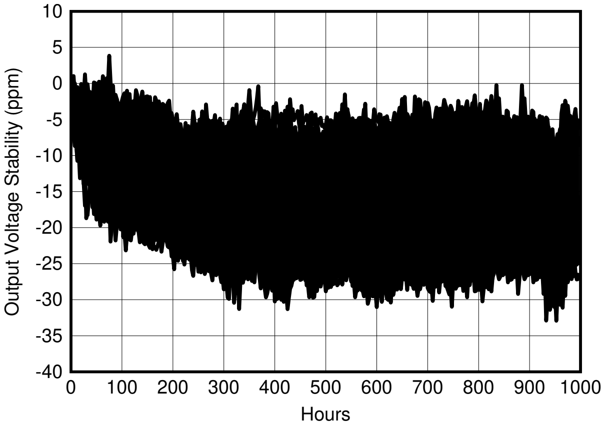

Figure 4-2. REF34 - VSSOP Package LTD

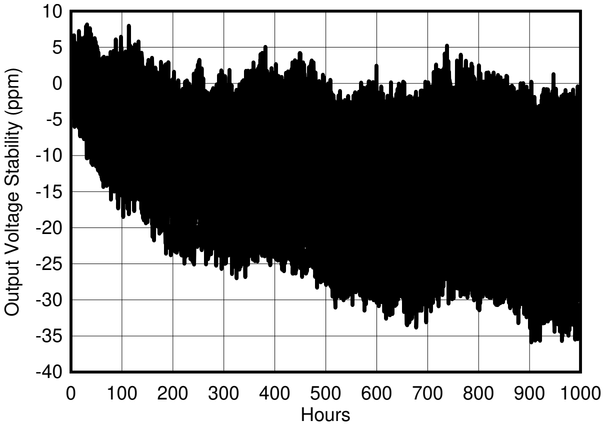

Figure 4-3. REF34 - SOT23-3 Package LTD

Ceramic packages have different compounds and assembly than plastic package. In a ceramic packaged device, the die is hermetically sealed (airtight) between two ceramic shields. The ceramic shield packaging does not need to cure and the filler material has a minimal effect on stress. So the ceramic (hermetically shielded) packages usually have the best LTD performance. Figure 4-4 shows the effect of LTD on the REF70 package.

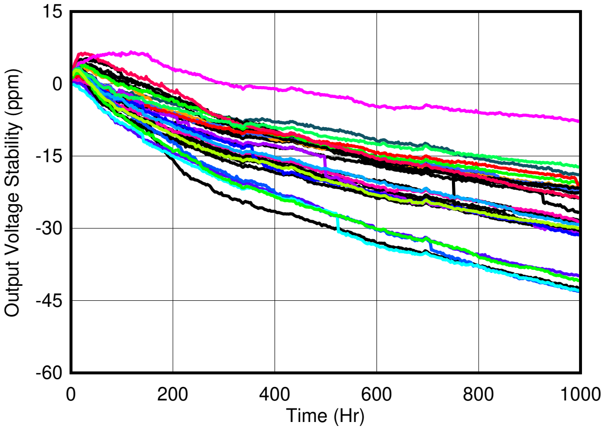

Figure 4-4. REF7025 - FHK Package LTD

5 Test Setup

At TI, LTD test is done on fully automated multisite bench setups. An example of one setup is shown in Figure 5-1. The PCB assembly is done with solder reflow to mimic exact application board condition and get uniform solder stress profile across all the devices. The PCB board and devices are fresh and not pre-baked. Oil bath is used to provide very stable temperature (±0.01°C variation) environment. All the devices are always powered on. Output of all the references are measured by 8.5 digits DMM after every half an hour. DMM is calibrated before each measurement cycle. All the error sources on the bench setup are calibrated with respect to Fluke732B voltage standard. LTD oil bath is above the room temperature (35°C) to avoid variations in room temperature causing any issues.

Figure 5-1. LTD Oil Bath Setup

6 Temperature Effect

The LTD curve of a typical device has the majority of the deviation within the first 100 hr. During the first 100 hr the device experiences the largest shift due to the mold curing. As time passes, the mold cures and the effect of the mold compound reduces. The LTD of the device will "settle" but it can keep increasing due to other stresses the die might experience such as PCB stress. Figure 6-1 shows the REF50 LTD deviation for 1year. After 1yr (8760 hr), the deviation of the REF50 is 60 ppm with the majority of the deviation before the first initial 1000 hr.

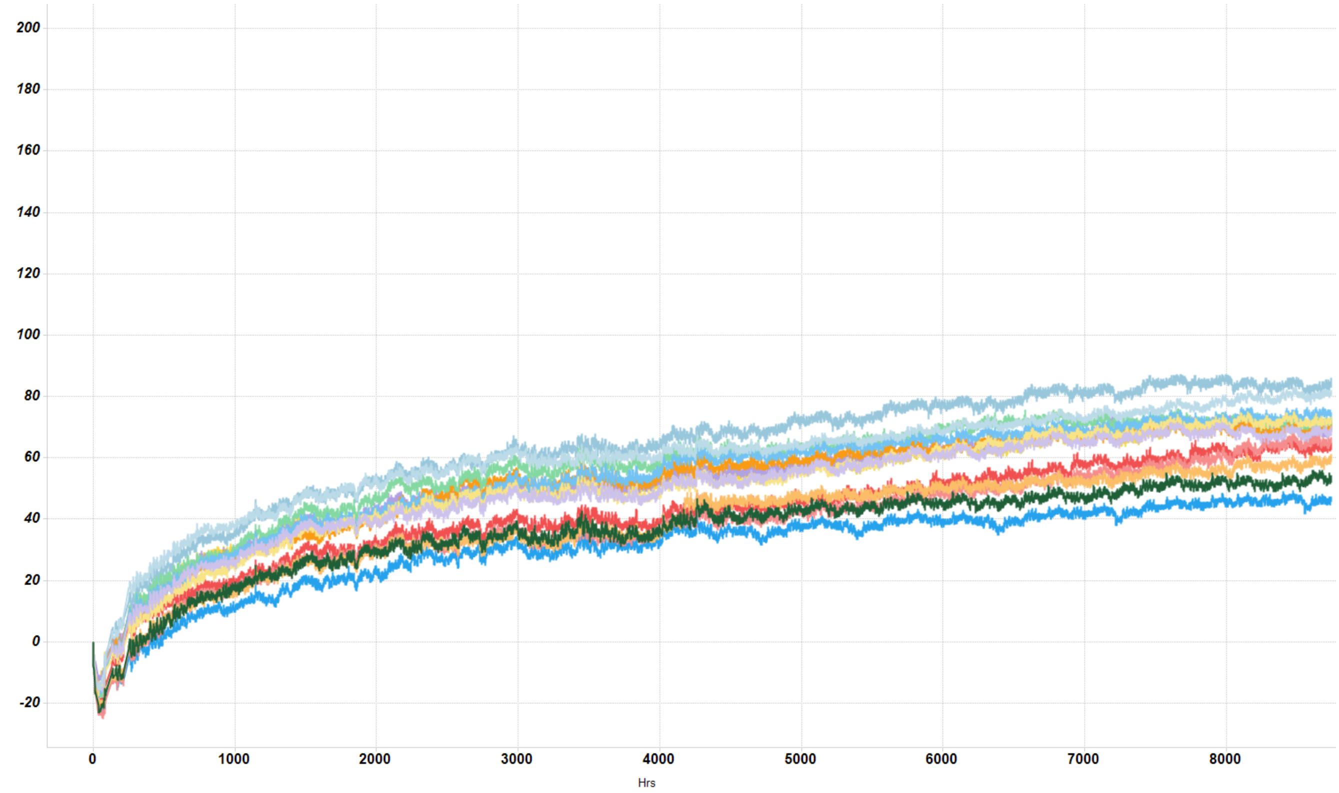

Figure 6-1. REF50 - VSSOP Package LTD 35°C

Temperature accelerates the stress settling factor and hence the LTD profile settles within a low drift coefficient earlier at higher temperature. In Figure 6-2, the LTD profile is settling after 100 hours at 85°C temperature. After 400 hr, the REF50 has a flat settled behavior with minimal deviation. There is device to device variation in how long it takes to reach a settled behavior.

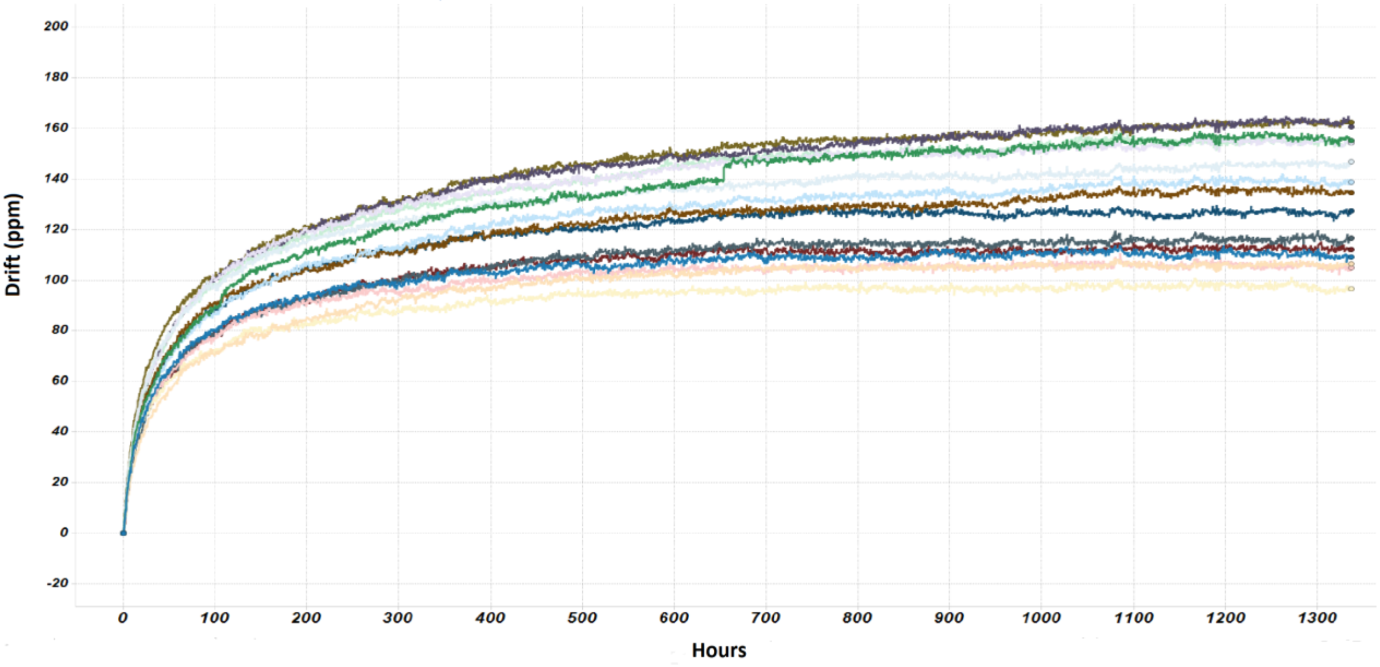

Figure 6-2. REF50 - VSSOP Package LTD 85°C

7 Long-Term Drift Estimation

A Long-Term Drift test can range from 1000 hr to much longer. The test is time consuming and can have issues in testing due to equipment calibration, equipment failures, and environmental reasons. Due to this, it is important to be able to estimate the behavior of the device over the entire lifetime of the system that can span 10 years. The difficulty comes from the nonlinear behavior of the device that is not consistent between device to device nor between products.

One common method to estimate LTD over a large period of time is from IC long term stability: The only constant is change by Marek Lis. In this article there is a Long-Term Estimation, that can be used to estimate LTD over a long period of time. Figure 7-1 shows the accuracy of the equation near 1000 hr. The main drawback of the equation is that from 4000 hr to 8760 hr the equation goes from having a typical value to a over estimation that will be growing over 10 years (87600 hr). This is due to the REF50 settling behavior that cannot be characterized. Different voltage references will have different behavior that might not match the equation due to their settling behavior. The equation is useful to get a conservative estimate of LTD but it does have its limitations.

$$\mathrm{LTD(hr)} = \mathrm{LTD(1k\,hr)} * \sqrt{\frac{\mathrm{hr}}{1000}} \tag{2}$$

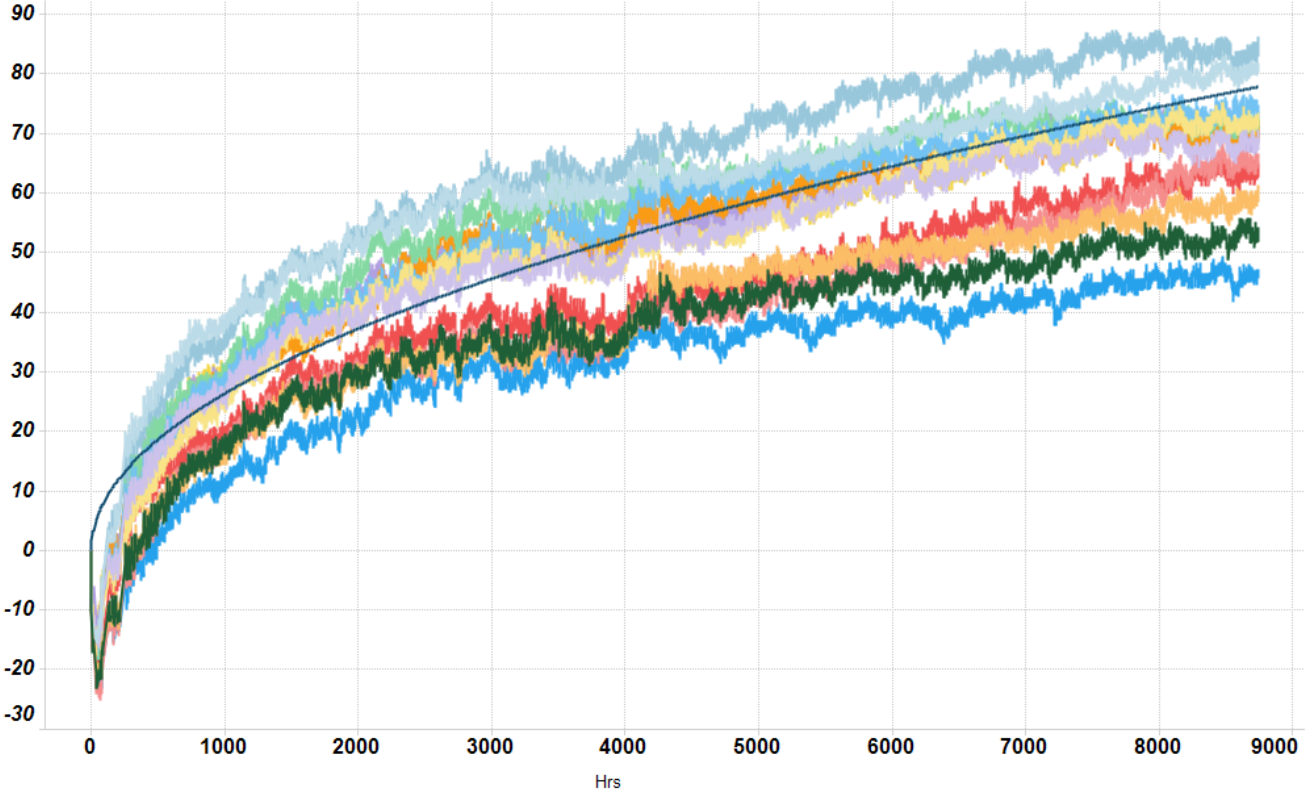

Figure 7-1. REF50 - VSSOP With Estimation

8 Methods to Minimize LTD Impact

The impact of LTD on a system can be minimized by the following:

- Bake the device in power on condition before calibrating to remove the large deviation that occurs in the initial hours.
- If high precision is required, it is recommended to have routine calibration.
- If routine calibration is not possible, delay the 1st time calibration as late as possible to let the device age. Preferably just before installation or commissioning in the field.

9 Reference

- *IC long term stability: The only constant is change – TI E2E*
- *Low-drift bandgap voltage reference* – Fabiano Fruett , Gerard C.M. Meijer , Anton Bakker
- *Long term characterization of voltage references* - Hubert Halloin , Peirre Prat, Julien Brossard

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