Application Report
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Hercules Family Frequency Slewing to Reduce Voltage and Current Transients

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ABSTRACT

This application report describes a method to dynamically increase device frequency in a way that minimizes voltage dips on the board power supply. The PLL's multiplier can be stepped in 8% steps every 50 reference clocks.

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1 Overview of Slewing Considerations

The Hercules™ family of devices has a phase-locked loop (PLL) for synthesizing device frequencies. The simplified block diagram of the PLL is shown in Figure 1 .

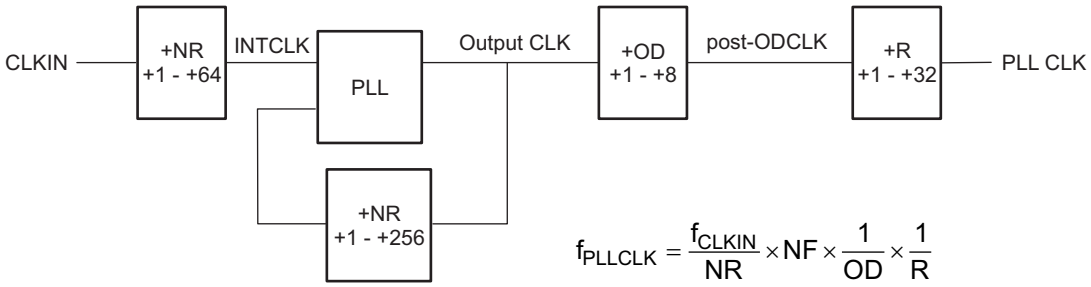

Figure 1. PLL Block Diagram

The oscillator provides CLKIN to the PLL. It is divided by NR before multiplication by NF. After the PLL frequency synthesis, there are two cascaded dividers that allow the PLL CLK frequency to be reduced *digitally*. For more detailed information on the PLL operation, see the *Oscillator and PLL* section of the *TMS570LS31x/21x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU499). As discussed in the TRM and the device-specific data sheet, the PLL has frequency limits on *INTCLK*, *Output CLK*, and *post-OD CLK*. Obviously, the device maximum frequency governs the upper end of the PLL CLK range. For these limits, see the device-specific TRM and data sheet.

The PLL CLK frequency can be changed through the OD-divider and R-divider in order to implement digital steps to the frequency. Additionally, this PLL is capable of re-locking on-the-fly without generating a slip signal if:

- The step size is small enough
- The update rate for the stepping is slow enough

The on-the-fly change to the multiplier (NF) produces a smaller frequency-step than can be achieved with the digital divider; the on-the-fly multiplier change results in a more gradual frequency (and current) increase that is easier for an external regulator to supply.

This document is intended to define the pattern of steps that can be used to smooth the current steps for an external voltage regulator.

From an application perspective, a smooth increase in frequency (no large digital steps) reduces the current jumps to which the power supply circuitry must respond. If the PLL frequency is stepped on-the-fly in order to reduce the current transients seen by the power control circuitry, the stepping of the PLL must be slow compared to the rate of change of the power control circuitry.

This application report recommends a PLL maximum step size for the multiply factor of 8%.

The PLL requires time to lock to the new value before an additional step can occur. This settling time is defined in terms of INTCLK cycles: $f_{INTCLK} = \frac{f_{CLKIN}}{NR} \left(and\ T_{INTCLK} = NR \times T_{OSCIN}\right)$. The required settling time for a small perturbation to the PLL multiplier is 50 INTCLK periods (reference periods).

2 System Considerations Affecting the Power Supply

Although the PLL stabilizes within 50 reference cycles, the PLL's rate of change must be slower than the response of the board-level power supply system. That is, the response of the board-level voltage regulator must be known in order to choose an update rate.

For switching regulators, the first limitation on the update rate is the external stabilization circuitry. If the regulator requires a 10 µH inductor and 10 µF capacitor to filter the switching voltage, then the breakpoint of the filter occurs at $f_B = \frac{1}{2\pi\sqrt{LC}}$, which in this example falls at 16 kHz. If the DC operating point changes faster than 16 kHz (62.5 µs), the filter output shows an accumulating voltage droop. In order to minimize this droop, small frequency steps are programmed with a sufficient delay for the DC operating point to be re-established prior to the next step. Frequency steps smaller than 8% make each current/voltage step response smaller.

The frequency jump due to a fixed percentage step is much bigger when the PLL is at the top end of its range than when it is at the first frequency step of the ramp. Said another way, adding a constant percentage to the divider produces an exponential increase in frequency and current. If this exponential ramp is not acceptable, add a constant value (starting from the initial 8% step) and generate a linear ramp.

3 Procedure for Changing Frequency

The procedure for slewing the device to its final frequency depends upon whether the final PLL CLK frequency exceeds 250 MHz. If the final PLL CLK frequency exceeds 250 MHz, then the *PLL* should be used with all output dividers equal to 1. If the final PLL CLK frequency is less than 250 MHz, the final divider may be maintained as 2. The procedure is as shown in Table 1.

Table 1. Procedure for Changing Frequency

PLL CLK < 250 MHz	PLLCLK ≥ 250 MHz
1) Determine maximal frequency step [Δf_{max} in terms of MHz]; this step is seen when the PLL changes its R-divider from /3 to /2. The maximal step determines the initial Output CLK frequency. $\Delta f_{max} = \frac{(f_{VCO})_{init}}{2} - \frac{(f_{VCO})_{init}}{3}$ $(f_{VCO})_{init} = 6 \times \Delta f_{max}$	1) Determine maximal frequency step [Δf_{max} in terms of MHz]; this step is seen when the PLL changes its R-divider from /2 to /1. The maximal step determines the initial Output CLK frequency (typically close to VCO*min*). $\Delta f_{max} = \frac{(f_{VCO})_{init}}{1} - \frac{(f_{VCO})_{init}}{2}$ $(f_{VCO})_{init} = 2 \times \Delta f_{max}$
Note: The initial Output CLK frequency must be greater than the minimum VCO frequency. This constraint effectively ties the maximal frequency step to the minimum VCO frequency.	**Note:** The initial Output CLK frequency must be greater than the minimum VCO frequency. This constraint effectively ties the maximal frequency step to the minimum VCO frequency.
Increase PLL CLK frequency through R-divider changes (/6 → /3 → /2)	Increase PLL CLK frequency through R-divider changes (/6 → /2 → /1)
2) Set the initial PLL CLK frequency as a frequency step above the crystal frequency with the OD-divider set to /1; the R-divider is set to /6. The initial frequency step from the crystal to the first PLL frequency is not be larger than Δf_{max}. Lock the PLL to this divided initial Output CLK frequency. When the PLL is valid, enable the GCLK and HCLK to run on the PLL output.	
3) Delay changing the frequency based upon the response time of the power supply. The Dual Clock Comparator (DCC) can be used to count oscillator cycles in order to set this delay **Note:** When the DCC is configured to count oscillator cycles, the crystal frequency [in MHz] defines the number of cycles in 1 µs. Therefore, a 50 µs delay is achieved with a 20 MHz crystal by counting = 1250 oscillator cycles. For more detailed information on the DCC operation, see the *Dual-Clock Comparator (DCC) Module* section of the *TMS570LS31x/21x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU499) .	
4) Set the next PLL CLK frequency as a frequency step above the initial frequency; maintain OD-divider at /1 and set the R-divider to /3 (1). There is no change to the PLL loop so immediately begin the delay.	4) Set the next PLL CLK frequency as a frequency step above the initial frequency; maintain OD-divider at /1 and set the R-divider to /2 (1) There is no change to the PLL loop so immediately begin the delay.
5) Delay changing the frequency based upon the response time of the power supply. The DCC can be used to count oscillator cycles in order to set this delay	
6) Set the next PLL CLK frequency as a frequency step above the previous frequency; maintain the OD-divider at /1 and step the R-divider to /2. There is no change to the PLL loop so immediately begin the delay.	6) Set the next PLL CLK frequency as a frequency step above the previous frequency; maintain the OD-divider at /1 and step the R-divider to /1. There is no change to the PLL loop so immediately begin the delay.
7) Delay changing the frequency based upon the response time of the power supply. The DCC can be used to count oscillator cycles in order to set this delay Increase Output CLK frequency through multiplier changes (maximum change is NF + 8%)	
8) Increase the NF multiplier by no more than 8%. The PLL loop is changed, locking to the new Output CLK frequency following a response similar to what is shown in Figure 2.	

(1) This procedure assumes that the ramp should be carried out in as few steps as possible (with appropriate delays between each step). If the regulator can supply a consistent jump of ΔI, then it makes sense to step in the largest divider steps possible (for example, /6 → /3 → /2 or /6 → /2 → /1). However, regulators are sensitive to not only ΔI but also ΔI/I (or the step as a fraction of the current bias point). Therefore, choose the largest jump that does not violate ΔI *at the current bias condition*.

Table 1. Procedure for Changing Frequency (continued)

PLL CLK < 250 MHz	PLLCLK ≥ 250 MHz

20MHz/5 Reference Frequency -- multiplier step

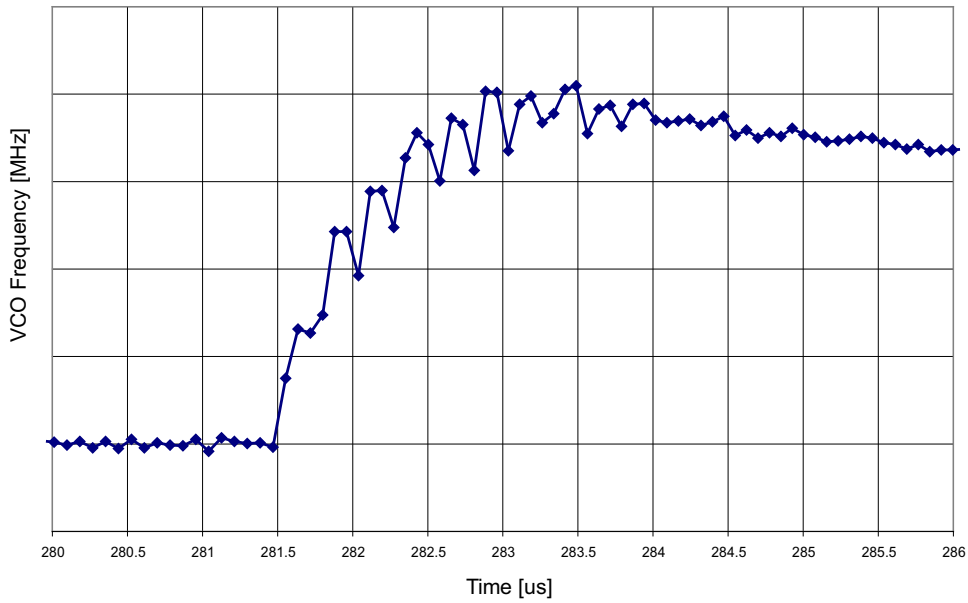

Figure 2. PLL CLK Frequency Step With a Multiplier Change

9) Delay changing the frequency *based upon the response time of the power supply*; because these frequency and current steps are typically smaller than the digital stepping, the delay might be reduced based upon the response of the *power supply*. The DCC can be used to count oscillator cycles in order to set this delay.
Continue to increase the frequency by increasing the multiplier and then waiting for the power supply to settle (steps 8 and 9). The frequency ramp can be exponential (by continuing to increase the multiplier NF by a fixed *percentage*) or linear (by continuing to increase the multiplier NF by a fixed *amount*).

NOTE: The PLL parameters must continue to be obeyed. That is:

- The Output CLK frequency cannot exceed VCO_{max}
- The PLL multiplier cannot exceed the maximum multiplier
- The *post-ODCLK* frequency cannot exceed the maximum *post-ODCLK* frequency

NOTE: When changing the PLL multiplier (NF), the change must be the smaller of {8%, Δf_{max}}. For an exponential frequency ramp, it is likely that the last steps will be governed by limiting Δf_{max} rather than maintaining a fixed percentage increase in the multiplier.

4 Examples

Examples assume that the regulator can step 150 mA with a 100 µs recovery time for a digital step and 40 µs recovery from a smaller (analog) step. These delay times should be verified against the particular regulator topology used in the final system. Estimate is active (dynamic) current.

4.1 16 MHz crystal, 180 MHz GCLK and HCLK, 90 MHz VCLK (TMS570LSxx and TMS570RM4xx)

Table 2. 16 MHz crystal, 180 MHz GCLK and HCLK, 90 MHz VCLK (TMS570LSxx and TMS570RM4xx)

Frequency [MHz]	Current [mA]	Current Step [mA and %]	Configuration	Delay [µs]
16	41.2		Crystal	
60	91.3	50.1 and 121.5%	16/ 4 * 90/(1*6) = 60	100
120	159.5	68.3 and 74.8%	16/ 4 * 90/(1*3) = 120	100
180	227.8	68.3 and 42.8%	16/ 4 * 90/(1*2) = 180	100

5 References

- *TMS570LS31x/21x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU499)

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