

# ***AN-1217 How to Validate BLVDS SER/DES Signal Integrity Using an Eye Mask***

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## **ABSTRACT**

The following application report contains information that will help you validate signal quality on a BLVDS SER/DES link. How to capture an eye pattern, how to generate an eye mask, and how to validate signal quality are all explained in detail in this document.

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## 1 Introduction

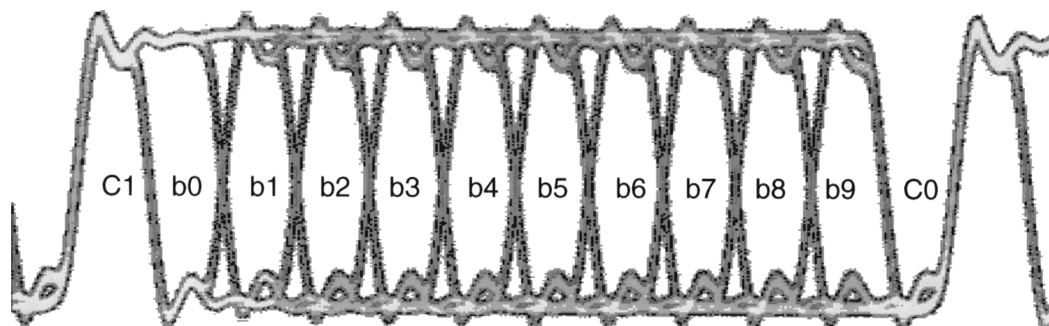
The TI DS92LV1023 and DS92LV1224 are used as examples, but this procedure can be used with other BLVDS SER/DES devices. The 1023/1224 chipset operates between 40 and 66 MHz and serializes a 10-bit data bus. Data sheets for the DS92LV1023 and DS92LV1224, as well as information on other LVDS and Bus LVDS devices, can be found on TI's website at <http://www.LVDS.ti.com>.

## 2 How to Capture a Serialized BLVDS Eye Pattern

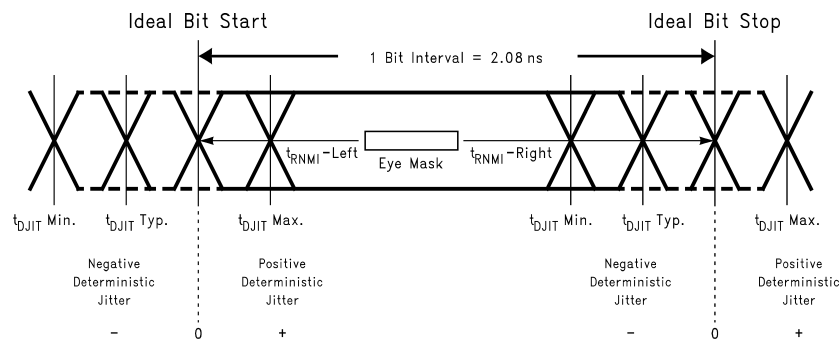
Capturing a low voltage differential signal (LVDS) is simple as long as you follow a few general guidelines. First, make sure you are operating within the specifications for the DS92LV1023 and DS92LV1224. In order to see the full twelve bits (10 data bits and 2 embedded clock bits), you must trigger on an external clock source. In this scenario, use the same source as the TCLK input for the DS92LV1023. Pseudo random data should be applied to the transmitter data input pins along with clock from a data generator or other source. The display on the oscilloscope should also be set to variable persistence mode. In order to accurately probe the LVDS signal, a high bandwidth (>1 GHz) and high impedance (>100k $\Omega$ ) differential probe should be used. In the example shown below, a Tektronix TEKP6248 differential probe was used.

## 3 The Ideal Start and Stop Bit Position

After using the recommendations above, you should be able to capture an eye pattern that looks like [Figure 1](#). The bits have been labeled for clarity.



**Figure 1. BLVDS Serialized Payload Eye Pattern With PRBS Data**



**Figure 2. Single BLVDS Data Bit Drawing**

[Figure 2](#) shows all parameters involved when isolating a single bit from the data stream. Not all parameters will apply, and in order to determine which parameters will apply, the ideal start and stop bit positions need to be calculated. By determining the ideal bit positions, you can determine if the start and stop positions for the captured signal are early, late, or ideal. For this example, you will use a 40 MHz clock with a period (T) of 25.0 ns. There are a few guidelines to remember when making start and stop bit calculations. For one, all calculations should be made from the first clock (C1) edge. This should be considered time zero for the period. Ideally, each bit is T/12 wide, or in this case, 25.0 ns/12 = 2.083 ns wide per bit. The bits start and stop in increments of 2.083 ns from the C1 rising edge. Applying this, you will arrive at [Table 1](#).

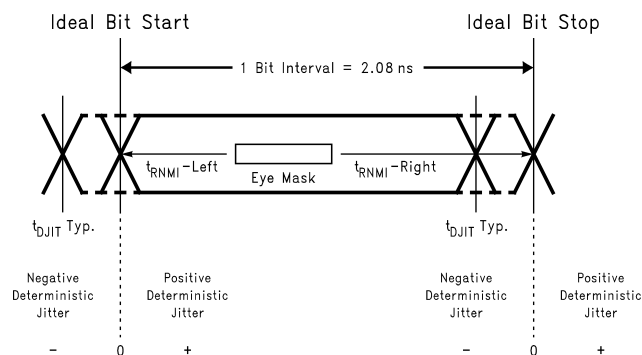
**Table 1. Ideal Start and Stop Bit Positions**

Bit No.	Bit Description	Ideal Bit Start (ns)	Ideal Bit Center (ns)	Ideal Bit Stop (ns)
1	C1	0.000	1.040	2.083
2	0	2.083	3.123	4.166
3	1	4.166	5.206	6.249
4	2	6.249	7.289	8.332
5	3	8.332	9.372	10.415
6	4	10.415	11.455	12.498
7	5	12.498	13.538	14.581
8	6	14.581	15.621	16.664
9	7	16.664	17.704	18.747
10	8	18.747	19.787	20.830
11	9	20.830	21.870	22.913
12	C0	22.913	23.953	24.996
<b>Conditions: Frequency = 40 MHz; Period (T) = 25.0 ns</b>				

It is easiest to tell if a bit's start or stop position is early or late by using the vertical cursor function on the oscilloscope. One vertical cursor should be placed on the C1 rising edge (time zero) and another should be placed at the crossing point of the isolated bit. Use the 0V (differential) crossing and the center of the distribution to set the first cursor on the clock transition center (C0 to C1 rising edge). Move the second cursor to the ideal location (a delta of 2.083 ns in this example) for the ideal start location of the first data bit. If the waveform on the oscilloscope transitions before the cursor, the bit is early. If aligned, it is at the ideal location, and if after, it is late. Minor offsets are expected due to PLL constraints, clock purity, and external noise.

#### 4 Adjusting to Ideal Bit Positions and Placing the Eye Mask

In placing the leading edge of an eye mask, the three important parameters are the ideal bit start position,  $t_{RNMI-LEFT}$ , and  $t_{DJIT}$  typical. Because the eye mask may not be perfectly centered within the ideal bit (it may actually be on the early side of the bit, for example), only the worst-case (leading edge)  $t_{RNMI-LEFT}$  min. is specified. The noise margin on the trailing side of the measured bit is larger. Looking at the  $t_{DJIT}$  specification from the DS92LV1023 data sheet, you will see that, typically, the start and stop bit positions are 80ps early (designated by a negative sign). This is depicted in Figure 3.


**Figure 3. Parameter Relationships to Generate the Eye Mask**

Looking at the DS92LV1224 data sheet at 40 MHz, the worst-case noise margin ( $t_{\text{RNMI}}$  min.) is 450 ps. The trailing edge of the eye mask has a larger noise margin, and you can use the typical noise margin value of 730 ps for this measurement. This information is all that is required to set the eye mask. However, because the noise margin specification is measured to the ideal start and stop bit positions, it needs to be budgeted against transmitter deterministic jitter ( $t_{\text{DJIT}}$  max.), intersymbol interference (ISI), and available margin. To ensure error free operation, no hits should be observed in the eye mask.

Leading edge:  $t_{\text{RNMI-LEFT}}$  Min. -  $t_{\text{DJIT}}$  typ. = 450 ps - (-80 ps) = 530 ps

Trailing edge:  $t_{\text{RNMI-RIGHT}}$  Typ. +  $t_{\text{DJIT}}$  typ. = 730 ps + (-80 ps) = 650 ps

Figure 4 shows a single scope captured bit with a properly placed eye mask. The captured signal has been outlined for clarity.

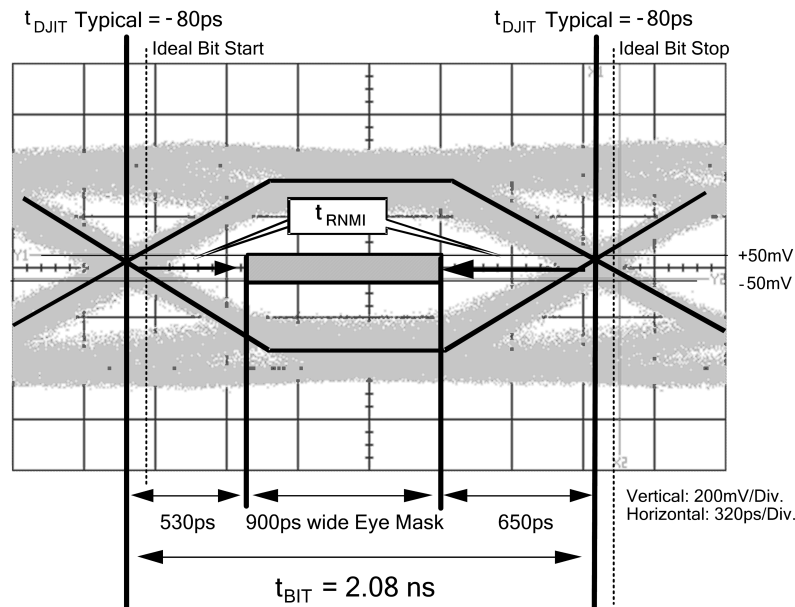


Figure 4. Captured Eye Pattern With Properly Placed Eye Mask

So on the scope, the leading edge of the mask should be placed 530 ps after the middle of the observed crossing. And the trailing edge of the mask should be placed 650 ps before the next observed crossing. Therefore, in this example, the eye mask is about 900 ps wide. Typically, the strobe window for the DS92LV1224 is about 100 ps wide. However, the position of this window shifts due to bit order, process, temperature, and frequency. Therefore, the 900 ps eye mask is a conservative mask that includes a four-sigma margin.

The minimum and maximum specifications for  $t_{\text{DJIT}}$  are not necessary to place the eye pattern mask but can be used to determine interoperability between serializers and deserializers. For example, it would not be advisable to use a serializer with a typical deterministic jitter of 0 ps and a maximum deterministic jitter of +300 ps with a deserializer with a noise margin of 300 ps; the deterministic jitter from the serializer would use up all of the receiver's noise margin, leaving no margin for inevitable interconnect loading (ISI).

## 5 Validating Signal Quality

For reliable link operation, the opening of the eye pattern should be outside of the eye mask. You have already determined where to place the leading and trailing edge of the eye mask, so now you need to draw the actual height (amplitude) for the eye mask. The amplitude of the eye mask is simply the differential receiver's input threshold voltages ( $V_{\text{TH}}$  and  $V_{\text{TL}}$ ), which are typically  $\pm 50$  mV. In some cases, a  $\pm 100$  mV level is used to make the verification measurement more conservative. As long as the captured eye opening stays out of the eye mask, the chipset should be able to operate error free. Note that this validation is done at the receive end of the link, after the interconnect loading effects have occurred.

## 6 Applicable Devices

Current and future data sheet noise margin specifications will not account for transmitter deterministic jitter. All current and future parts will measure eye mask corners to ideal bit positions. [Table 2](#) lists all current (Q1 CY2002) devices where this application report applies. In addition, all future product data sheets will separate the left ( $t_{\text{RNMI-LEFT}}$ ) and right ( $t_{\text{RNMI-RIGHT}}$ ) noise margin specifications and use this methodology to validate signal quality.

**Table 2. Current (Q1 CY2002) Applicable Parts**

Part Number	Description
DS92LV1212A	10-Bit Deserializer
DS92LV1224	10-Bit Deserializer
DS92LV1260	Six Channel 10-Bit Deserializer
DS92LV16 <sup>(1)</sup>	16-Bit Transceiver
SCAN921226	10-Bit Deserializer with SCAN
SCAN921260	Six Channel 10-Bit Deserializer with SCAN

<sup>(1)</sup> The DS92LV16 is a 16-bit transceiver; calculations used must be adjusted accordingly.

First generation devices measured noise margin to the maximum  $t_{\text{DJIT}}$  limit. These parts are listed in [Table 3](#). Therefore, for these devices, noise margin is a chipset specification and is allocated solely to the interconnect. The measurement location of  $t_{\text{RNM}}$  was changed to allow inter-operation calculations between different devices within the family (10-bit payload).

**Table 3. Past Non-Applicable Parts**

Part Number	Description
DS92LV1210	10-Bit Deserializer
DS92LV1212	10-Bit Deserializer

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