

SCANSTA101



Literature Number: SNLA198

SCANSTA101 Quick Reference

Registers

| Address | Register | Active Bits | Reset Value |
|---------|----------------------|-------------|-------------|
| 0x00 | Start | 5 | 0x0000 |
| 0x01 | Status | 10 | 0x0000 |
| 0x02 | Interrupt Control | 8 | 0x0000 |
| 0x03 | Interrupt Status | 8 | 0x0000 |
| 0x04 | Setup | 8 | 0x0043 |
| 0x05 | Clock Divider | 6 | 0x0000 |
| 0x07 | LFSR Exponent | 3 | 0x0000 |
| 0x08 | LFSR LSB Seed | 16 | 0x0000 |
| 0x09 | LFSR MSB Seed | 16 | 0x0000 |
| 0x0A | LFSR LSB Result | 16 | 0x0000 |
| 0x0B | LFSR MSB Result | 16 | 0x0000 |
| 0x0C | Index | 16 | 0x0000 |
| 0x11 | Vector Index | 16 | 0x0000 |
| 0x13 | Header/Trailer Index | 16 | 0x0000 |
| 0x15 | Macro Index | 16 | 0x0000 |
| 0x17 | Sequencer Index | 16 | 0x0000 |
| 0x19 | Bridge Support | 16 | 0x0000 |

Memory Map

| R/W Address | Function | Base Address (Long Words) | Long Word Index | Index Register |
|-------------|---------------------|---------------------------|-----------------|----------------|
| 0x0D | TDO_SM | 0x00 | 0x000 to 0x1BF | 0x0C |
| 0x0E | TDI_SM | 0x1C0 | 0x000 to 0x1BF | 0x0C |
| 0x0F | Expected | 0x380 | 0x000 to 0x1BF | 0x0C |
| 0x10 | Mask | 0x540 | 0x000 to 0x1BF | 0x0C |
| 0x12 | Vector 1 | 0x700 | 0x0 to 0x1 | 0x11 |
| | Vector 2 | 0x700 | 0x2 to 0x3 | |
| | Vector 3 | 0x700 | 0x4 to 0x5 | |
| | Vector 4 | 0x700 | 0x6 to 0x7 | |
| 0x14 | Data header | 0x708 | 0x00 to 1x1F | 0x13 |
| | Data trailer | 0x728 | 0x20 to 0x3F | |
| | Instruction header | 0x748 | 0x40 to 0x5F | |
| | Instruction trailer | 0x768 | 0x60 to 0x7F | |
| 0x16 | Macro 1 to Macro 16 | 0x788 to 0x797 | 0x0 to 0xF | 0x15 |
| 0x18 | Sequencer | 0x798 | 0x00 to 0x1F | 0x17 |
| 0x1A | Scan Bridge support | 0x7B8 | 0x00 to 0x3F | 0x19 |

Vector Structure

The vector is two long words (64 bits) long.

| Bits | Function | Comment |
|--------------|----------------------------------|--|
| 0x00 to 0x1F | Data length (long words) | Maximum of 2 ¹⁷ long words or 4 Gbits |
| 0x20 to 0x27 | Macro number | 0 to 255 (only macros 0 to 15 are valid) |
| 0x28 to 0x2E | Reserved | Reserved |
| 0x2F | Preloaded data / load on the fly | Preloaded – 1 load on the fly – 0 |
| 0x30 to 0x3F | Reserved | Reserved |

Macro Structure

Macro controls the TMS_SM line. The macro is 1 long word (32 bits) long.

| Bits | Function | Comment |
|--------------|------------------------------|--|
| 0x00 to 0x06 | First 7 TMS_SM bits | Most significant bits are shifted out |
| 0x07 | TMS_SM loop bit | Loop bit for SHIFT or BIST macro |
| 0x08 | TMS_SM bit at terminal count | Output at terminal count for SHIFT macro |
| 0x09 to 0x0F | Last 7 TMS_SM bits | Least significant bits are shifted out |
| 0x10 to 0x11 | Macro type bits | See macro type table |
| 0x12 to 0x14 | Header/trailer usage | See header/trailer usage table |
| 0x15 | Macro structure bit 7 enable | Ignored for SHIFT macros |
| 0x16 | Macro structure bit 8 enable | Ignored for SHIFT macros |
| 0x17 | Sync bit support enable | Sync bit length in setup register |
| 0x18 to 0x1A | Pre-shift TCK_SM count | Count of bits 0x00 to 0x06 to be used |
| 0x1B to 0x1D | Post-shift TCK_SM count | Count of bits 0x09 to 0x0F to be used |
| 0x1E | Use mask | Use mask – 1 Compare all bits – 0 |
| 0x1F | Compare | Compare TDI_SM to expected |

Macro Type

Macro type is set by bits 0x11:0x10 in the macro structure.

| Bit 0x11 | Bit 0x10 | Macro Type | Comment |
|----------|----------|------------------|---|
| 0 | 0 | BIST | Loop-on-loop bit for vector count – no data |
| 0 | 1 | SHIFT | Loop-on-loop bit for vector count – data from TDO_SM memory |
| 1 | 0 | SHIFT w/ capture | Loop-on-loop bit for vector count – data from TDO_SM memory – data to TDI_SM memory |
| 1 | 1 | STATE | No loop – no data |

Header/Trailer Usage

A macro can call out an instruction shift or a data shift, but not both.

| Bit 2 | Bit 1 | Bit 0 | Function |
|-------|-------|-------|------------------------------------|
| 0 | 0 | 0 | Ignore headers and trailers |
| 0 | 0 | 1 | Use instruction header |
| 0 | 1 | 0 | Use instruction trailer |
| 0 | 1 | 1 | Use instruction header and trailer |
| 1 | 0 | 0 | Use data header |
| 1 | 0 | 1 | Use data trailer |
| 1 | 1 | 0 | Use data header and trailer |
| 1 | 1 | 1 | Reserved |

Header/Trailer Structure

The headers and trailers are 32 long words (1024 bits) long

| Bits | Function | Comment |
|---------------|---------------------|---|
| 0x00 to 0x1F | Data length (bits) | Must be > 0 if use header/trailer bits are set in macro |
| 0x20 to 0x3FF | Header/trailer data | Max 922 bits |

SCANSTA101 Quick Reference

Sequencer Structure

| Bits | Function | Comment |
|----------------|---------------------------------------|---|
| 0x00 to 0x1F | Sequence repeat count | Max of 255 |
| 0x20 to 0x2F | Vector repeat count | First vector |
| 0x30 to 0x3F | Vector number | First vector |
| ..x.. - ..x.. | Vector repeat count and vector number | Repeat for each vector to be used in sequence |
| 0x3E0 to 0x3EF | Vector repeat count | Vector 255 (if used) |
| 0x3F0 to 0x3FF | Vector number | Vector 255 (if used) |

Scan Bridge Support Structure

Only Mode Register 0 in the Scan Bridge is used.

| Bits | Function | Comment |
|----------------|------------------------------|--------------------------------|
| 0x00 to 0x0F | Number levels | Levels of Scan Bridge support |
| 0x10 to 0x17 | Scan Bridge address | Level 0 |
| 0x18 to 0x1F | Scan Bridge LSPs | Level 0 |
| 0x20 to 0x27 | Scan Bridge address | Level 1 |
| 0x28 to 0x2F | Scan Bridge LSPs | Level 1 |
| ..x.. - ..x.. | Scan Bridge address and LSPs | Additional hierarchical levels |
| 0x7F0 to 0x7F7 | Scan Bridge address | Level 125 (if used) |
| 0x7F8 to 0x7FF | Scan Bridge LSPs | Level 125 (if used) |

Use Mask/Compare

Use mask/compare is set by bits 0x1F:0x1E in the macro structure.

| Bit 0x1F | Bit 0x1E | Description |
|----------|----------|----------------------|
| 0 | 0 | Do not compare |
| X | 1 | Compare with mask |
| 1 | 0 | Compare without mask |

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Start Register

To begin scan operations, write the start register with a valid vector number.

| Bits | Type | Field |
|-------|------|--|
| 2:0 | RW | Use vector <2:0> - only vectors 1 to 4 are valid |
| 7:3 | RO | Reserved for future vector expansion |
| 8 | RW | Use sequencer (preloaded data) |
| 12:9 | RO | Reserved |
| 13 | RW | Onboard memory BIST |
| 15:14 | RO | Reserved |

Setup Register

| Bits | Type | Field |
|-------|------|---|
| 1:0 | RW | Test loop back |
| 2 | RW | Reset – synchronous processor-commanded reset |
| 3 | RW | TRST – Scan Master test reset |
| 4 | RW | Scan Bridge support initiate/release |
| 5 | RW | Debug mode |
| 6 | RW | Default TDO value on BIST or STATE macro |
| 9:7 | RW | Sync-bit length <9:7> |
| 11:10 | RW | TDO_SM control (use bit 6) |
| 14:11 | RO | Reserved |
| 15 | RW | 16/32-bit mode |

Status Register

Write to status register only for test and debug. Disable writes to register during normal operation.

| Bits | Type | Field |
|------|------|--------------------------------|
| 2:0 | RW | Using vector <2:0> |
| 7:3 | RO | Reserved for vector expansion |
| 8 | RW | Using sequencer |
| 9 | RW | TDI status half-full |
| 10 | RW | TDI status full |
| 11 | RW | TDO status empty |
| 12 | RW | TDO status half-empty |
| 13 | RW | Memory BIST result |
| 14 | RO | BIST running |
| 15 | RW | Results of compare (1 = match) |

Interrupt Control/Status Registers

Control register enables interrupts. Status register reports interrupt status.

| Bits | Type | Field |
|-------|------|-------------------------------|
| 2:0 | RW | Vector <2:0> interrupt |
| 7:3 | RO | Reserved for vector expansion |
| 8 | RW | Sequencer interrupt |
| 9 | RW | TDI half-full interrupt |
| 10 | RW | TDO full interrupt |
| 11 | RW | TDO empty interrupt |
| 12 | RW | TDO half-empty interrupt |
| 15:13 | RO | Reserved |

Pin Descriptions

| Pin Name | I/O | Description |
|----------|-----|-------------------------------------|
| D(15:0) | I/O | Bidirectional data bus |
| A(4:0) | I | Address bus |
| SCK | I | System clock |
| INT | O | Interrupt output |
| OE | I | Output enable |
| DTACK | O | Data transfer handshake |
| R/W | I | Processor read/write |
| STB | I | Data transfer handshake |
| CE | I | Chip-enable data transfer handshake |
| RST | I | Asynchronous reset |
| TDO | O | TDO for SCANSTA101 TAP |
| TDI | I | TDI for SCANSTA101 TAP |
| TMS | I | TMS for SCANSTA101 TAP |
| TCK | I | TCK for SCANSTA101 TAP |
| TRST | I | TRST for SCANSTA101 TAP |
| TDI_SM | I | Scan Master test data input |
| TDO_SM | O | Scan Master test data output |
| TMS_SM | O | Scan Master test mode select |
| TCK_SM | O | Scan Master test clock output |
| TRST0_SM | O | Scan Master test reset output |
| TRIST_SM | O | Indicates TDO_SM is TRI-STATE® |

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