SCANSTA112

Literature Number: SNLA199

SCANSTA112 Quick Reference

Operating Modes

Scan Bridge – SCANSTA112 addressed by Level 1 protocol. Set up by register settings.

Stitcher – no Level 1 protocol; always addressed. Set up by pins or register settings.

Normal (not transparent) – instruction register in scan chain. Responds to most JTAG instructions. Pad bit between TDI and TDO on each local scan port.

Full Transparent – instruction register not accessible. No response to JTAG instructions. No pad bits between TDI and TDO.

Transparent Local Scan Port (LSP) – instruction register in scan chain. Responds to most JTAG instructions. Pad bit between TDI and TDO on last LSP.

Mode Availability

- Normal and full transparent modes are available in both Scan Bridge and Stitcher modes.
- Transparent LSP mode in Scan Bridge mode only.
- Full transparent mode can be exited only by reset.

Reset Sequence

Reset	IgnoreReset	Normal	Transparent
$\overline{\text{RESET}}$	0	Full reset	Full reset
$\overline{\text{RESET}}$	1	Full reset	Full reset
$\overline{\text{TRST}}$	0	Full reset	Full reset
$\overline{\text{TRST}}$	1	Ignored	Ignored
5-High TMS	0	Full reset	Ignored
5-High TMS	1	Ignored	Ignored

Addressing After Reset

Scan Bridge mode – Scan instruction register; data = slot address

Stitcher mode – always active; no addressing

Address Space

Address Type	Hex Address	TDO_B State
Direct address	0x00 to 0x39 0x40 to 0xFF	Normal per 1149.1 std.
Interrogation	0x3A	Address out (see AN-1259)
Broadcast	0x3B	TRI-STATE®
Multi-Cast 0	0x3C	TRI-STATE
Multi-Cast 1	0x3D	TRI-STATE
Multi-Cast 2	0x3E	TRI-STATE
Multi-Cast 3	0x3F	TRI-STATE

Registers

Name	Bits
Instruction register	8
Boundary register	22
Bypass register	1
Device ID register	32
Multi-Cast Group register	2
Mode Register 0	8
Mode Register 1	8
Mode Register 2	8
Linear Feedback Shift Register (LFSR)	16
TCK Counter register	32
Shared $GPIO_{(0-6)}$ registers	8
Control register	8
Local Scan Port (LSP) Select register	8

Register Access

Instruction register – transition IEEE-1149.1 TAP controller to Capture-IR/Shift-IR state

Boundary register – EXTEST or SAMPLE/PRELOAD

Bypass register – BYPASS

Device ID register – IDCODE, UNPARK, PARKTLR, PARKRTI, PARKPAUSE, GOTOWAIT, LFSRON, LFSROFF, CNTRON, CNTROFF

Multi-Cast Group register – MCGRSEL

Mode Register 0 – MODESEL

Mode Register 1 – MODESEL1

Mode Register 2 – MODESEL2

LFSR - LFSRSEL

TCK Counter register – CNTRSEL

Shared $GPIO_{(0-6)}$ registers – $SGPIO_n$

Control register – CONTROLSEL

LSP Select register – LSPSEL

Op-Codes

Instruction	Op-Code	Description
BYPASS	0xFF	Bypass register
EXTEST	0x00	Boundary register
SAMPLE/PRE-LOAD	0x81	Boundary register
IDCODE	0xAA	Device ID register
UNPARK	0xE7	Unparks LSPs
PARKTLR	0xC5	Parks LSPs in TLR
PARKRTI	0x84	Parks LSPs in RTI
PARKPAUSE	0xC6	Parks LSPs in Pause-IR or Pause-DR; Unparks parked LSPs
GOTOWAIT	0xC3	Sends all SCANSTA112s to wait for address
MODESEL	0x8E	Mode Register 0
MODESEL1	0x82	Mode Register 1
MODESEL2	0x83	Mode Register 2
MCGRSEL	0x03	Multi-Cast Group register
SOFTRESET	0x88	Parks all LSPs in TLR
LFSRSEL	0xC9	LFSR
LFSRON	0x0C	Accumulates signature
LFSROFF	0x8D	Stops signature accumulation
CNTRSEL	0xCE	TCK Counter register
CNTRON	0x0F	Enables TCK counter
CNTROFF	0x90	Disables TCK counter
DEFAULT_ BYPASS	0x07	Sets bypass register as default data register

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Op-Codes (continued)

Instruction	Op-Code	Description
TRANSPARENT0 to TRANSPARENT6	0xA0 to 0xA6	Sets single LSP and transparent mode
$SGPIO_0$ to $SGPIO_6$	0xB8 to 0xBE	Shared $GPIO_n$ register
CONTROLSEL	0x87	Control register
LSPSEL	0x86	LSP Select register
TRANSPARENTEN	0xA8	Sets transparent mode

General Sequence for Register Writes

1) Set TAP controller to RTI
2) Sequence to Shift-IR (TMS 1-1-0-0)
3) Shift in op-code to select register (TMS 0)
   Example – MODESEL = 0x8E on TDI
4) Sequence to Exit1-IR (TMS 1)
5) Sequence to Update-IR (TMS 1)
6) Return to RTI (TMS 0)
7) Sequence to Shift-DR (TMS 1-0-0)
8) Shift register contents in (TMS 0) example – Shift 0x01 on TDI into Mode Register 0 to select LSP 0
9) Sequence to Exit1-DR (TMS 1)
10) Sequence to Update-DR (TMS 1)
11) Return to RTI (TMS 0)

Register Functions

Instruction register – receives op-codes in Shift-IR TAP controller state

Boundary register – all boundary cells connected as a 22-bit shift register

Bypass register – one-bit bypass data register required by 1149.1

Device ID register – 32-bit read-only register containing device ID code

Multi-Cast Group register – Binary multi-cast group selection (00 = 0, 01 = 1, etc.)

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Mode Registers

Bit	Mode Reg 0	Mode Reg 1	Mode Reg 2
0	LSP0	LSP5	LSP0/GPIO0
1	LSP1	LSP6	LSP1/GPIO1
2	LSP2	Reserved	LSP2/GPIO2
3	TCK Free Run	Reserved	LSP3/GPIO3
4	TDIB-TDOB Loopback	Reserved	LSP4/GPIO4
5	LSP3	Reserved	LSP5/GPIO5
6	LSP4	Reserved	LSP6/GPIO6
7	TCK Counter status	Transparent LSP mode	LSP7/GPIO7

LFSR register – signature compactor; LFSRSEL allows scanning in a seed or scanning out a signature

TCK counter – when counter is enabled and LSP is parked, TCK_{LSP} drives clock pulses while TCK counter counts down to 0

Shared $GPIO_{(0-6)}$ – in GPIO mode (see Mode Register 2):

Bit	I/O	Function
0	O	TMS
1	O	TDO
2	I	TDI
3 to 7	N/A	Reserved

Control Registers

Bit	Function	Default
0	IgnoreReset	0
1	Transparent	TRANS pin
2	Scan Bridge/Stitcher	SB/$\overline{S}$ pin
3	$MPSel_{B1/\overline{B0}}$	$MPSEL_{B1/\overline{B0}}$ pin
4	TLR-TRST	TLR_TRST pin
5	$TLR\text{-}TRST_6$	TLR_TRST_6 pin
6	Reserved	0
7	Reserved	0

LSP Select register – Stitcher only; selects LSPs to be inserted in the scan chain

Pin Descriptions

Pin Name	I/O	Description
$\overline{RESET}$	I	Resets device regardless of state
ADDMASK	I	Masks 6 lower-slot address bits
$MPSEL_{B1/\overline{B0}}$	I	Selects master backplane port
SB/$\overline{S}$	I	Selects Scan Bridge or Stitcher mode
$LSPsel_{(0-6)}$	I	Selects LSPs in Stitcher mode
TRANS	I	Enables transparent mode at startup or reset – Stitcher only
TLR_TRST	I	Value of $\overline{TRST}_{(0-5)}$ when $LSP_{(0-5)}$ is in TLR
TLR_TRST_6	I	As above for LSP6
$TRIST_{B0}$, $TRIST_{B1}$, $TRIST_{(01-03)}$	O	Indicates associated TDO output is TRI-STATE
$A0_{B0}$, $A1_{B0}$, $A0_{B1}$, $A1_{B1}$	I	Backplane pass-through inputs
$Y0_{B0}$, $Y1_{B0}$, $Y1_{B1}$, $Y1_{B1}$	O	Backplane pass-through outputs
$S_{(0-7)}$	I	Slot identification
$\overline{OE}$	I	Output enable for LSPs
$A0_{01}$, $A1_{01}$	I	Local pass-through inputs
$Y0_{01}$, $Y1_{01}$	O	Local pass-through outputs
$TCK_{B0,B1}$, $TMS_{B0,B1}$, $TDI_{B0,B1}$, $TDO_{B0,B1}$, $\overline{TRST}_{B0,B1}$	I/O	Backplane JTAG TAPs
$TCK_{(01-06)}$, $TMS_{(01-06)}$, $TDI_{(01-06)}$, $TDO_{(01-06)}$, $TRST_{(01-06)}$	I/O	LSP JTAG TAPs

Miscellaneous

- Always reset SCANSTA112 if $MPSEL_{B1/\overline{B0}}$ pin changes
- Transparent mode can be set by TRANSPARENTN or TRANSPARENTEN instruction – must reset SCANSTA112 multiplexer to cancel transparent mode
- LSP Select register defaults to pin setting after reset

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