Application Report
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Using the SM28VLT32-HT With Power Saving Features

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ABSTRACT

Some applications will require or desire usage of low power features to increase battery life while down hole. This application note discusses the features, usage and implications of the SM28VLT32-HT Flash memory power savings modes.

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1 INTRODUCTION

The SM28LVT32 is a 32Mbits flash memory intended for use in extreme temp environments. It consists of 8 Flash banks, a Flash controller, Flash Pump, and SPI controller. The Flash array is configured as 16bits by 2M words. Each bank represents 16bits by 256K words (4Mbits). Each bank is further divided down into 8 sectors. See Figure 1 for block diagram.

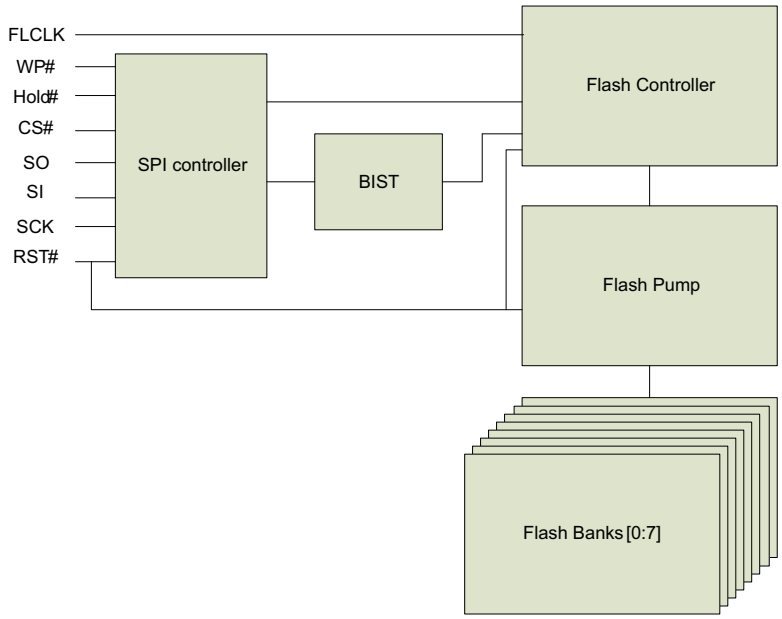

Figure 1. Block Diagram

By default, the SM28VLT32-HT powers up with all banks and flash pump active. This represents a nominal current demand of 120mA on Vcore, and 16mA on VIO. This static current load can be excessive for some applications. Applying reset will also return the device to default settings with banks and pump active.

2 FEATURES

The Flash controller has three power settings for the banks and flash pump. These are active, standby, and sleep. In order to set the power mode for a bank or pump, one must set the bank/pump fallback modes. This mode is set to active for all banks and pump on reset and power up.

The fallback power mode is defined as the power mode that is set after the banks (or pump) has expired the bank access grace period (BAGP) or pump active grace period (PAGP). The BAGP and PAGP must be programmed by user. If a bank is set to have a fallback mode of sleep, then after bank becomes inactive (no commands being executed affecting that bank) and the grace period has elapsed, the bank will automatically enter sleep. The converse is true as well. When a sleeping bank is accessed, then the bank will automatically transition to active mode. This automatic transition uses wait state registers to count the appropriate delay from sleep to standby, and from standby to active. It is useful to note, that if any BANK is active then the pump will be active. It cannot enter standby or sleep unless all banks are in standby or sleep.

Typical power numbers for all banks and pump in sleep and/or standby mode can be referenced in Table 1.

Table 1. Typical Power Numbers for Various States

DEVICE STATE				TYPICAL I_{CORE}	TYPICAL I_{IO}	UNITS
NUMBER OF BANKS IN STATE			PUMP STATE			
ACTIVE	SLEEPING	STANDBY				
1[(1)]	7	0	Active	18	15	mA
2	6	0	Active	33	15	mA
8	0	0	Active	125	15	mA
0	8	0	Sleep	2.5	<0.1	mA
0	8	0	Active	2.5	15	mA
0	0	8	Standby	5	<0.1	mA

(1) Each additional active bank adds 15mA to typical I_{CORE}.

3 REGISTER DEFINITIONS

Table 2. Per Bank Registers

Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAC1	X0000h	BAGP								WTBSTDBY						BNKPWR	
BAC2	X0001h	OTP	WTBSLEEP							WTPAGE				WTREAD			

Table 3. Bank Identifiers

Bank0	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7
000	004	008	00C	010	014	018	01C

3.1 Bank Access Register 1 (BAC1)

BAGP— Bank access grace period

These 8 bits represent the count values of FCLK to delay reverting from the active mode to the bank fallback mode defined by the BNKPWR bits.

WTBSTDBY— Standby mode wait state generation

The 6 bits represent the delay count of FCLK before going to active mode from standby when an access demands transition to active mode. This count value should represent a time value of greater than 120ns. This represents a value of 2 or greater for WTBSTDBY at 12MHz FCLK.

BNKPWR— Bank's fallback power mode

00 = Sleep, 01 = Standby, 10 = Reserved, 11 = active.

3.2 Bank Access Register 2 (BAC2)

OTP— Protection bit for reserved flash area

0 is protected, 1 is unprotected. Usage of OTP is outside the scope of this document, and can be set to 0 or 1 without issue.

WTBSLEEP— Sleep mode wait state generation for the bank

The 7 bits represents the delay count of FCLK before going from SLEEP to STANDBY mode when an access demands transition to active mode. This value should represent a time value of greater than 1.5µs. At 12MHz FCLK, this value should be set to a minimum of 0x12.

WTPAGE and WTREAD —Wait states for read modes

The necessity to change the wait states in this application is not required. These values must be left at default value of 1 for each counter. Increasing the wait states to larger values can cause the read command to fail due to data not being available when necessary.

Table 4. Global (Pump) Registers

Name	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC1	XF000	PRT	WTBSLEEP														
MAC2	XF001	WTPSTDBY											PMPPWR		BANK		
PAGP	XF002	PAGP															

3.3 Module Access Register 1 (MAC1)

PRT— Protection bit for a software protection scheme

Usage of this bit is outside the scope of this document. This bit should be left logic low.

WTBSLEEP— Count value for the pump sleep mode down counter

When counter expires, it indicates that the bank has transitioned from sleep to active. This value should represent a time value of greater than 2µs. At 12MHz FCLK, WTBSLEEP should be programmed to 0x0018 or larger.

WTPSTDBY— Pump standby wait state counter and represents the time for transitioning from active from standby

The minimum value for wake up from standby is 500ns, and represents a minimum count value of 0x06 at 12MHz.

PMPPWR— Pump's fallback power mode

Where 00 = sleep, 01 = Standby, 10 = reserved, and 11 = Active. These bits will set the pumps power mode after the pump active grace period counter times out.

BANK— Reserved control for internal testability functions

These bits must be left at 000.

PAGP— Pump active grace period counter

This represents the amount of time (in flash clocks) that the Pump will remain active after last command before entering the fallback setting for PMPPWR.

3.3.1 Psuedo Code to Set All Banks and Pump Fallback Mode to Standby Mode

The following pseudo code is in the following format: Command_Address_Data. This format is the same format that is used for the SM28VLT32 GUI. The below code issues the command 0x1D, to various BANKS accessing the BAC1 register, followed by the value to be written. In each case for setting bank power mode, only value changing is the bank identifier. The value written to BAC1 is FF09. This is setting the BAGP to max value with WTBSTDBY to 2. The value written to BAC2 is 1211. This is setting the WTBSLEEP to 0x12 and each of WTPAGE and WTREAD to 0x1. The last command is setting the pump fallback mode to standby by accessing MAC2 register.

1D_0000000_FF09 // set bank 0 pwr dn fallback mode to standby

1D_0000001_1811 // set bank 0 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_0040000_FF09 // set bank 1 pwr dn fallback mode to standby

1D_0040001_1211 // set bank 1 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_0080000_FF09 // set bank 2 pwr dn fallback mode to standby

1D_0080001_1211 // set bank 2 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_00C0000_FF09 // set bank 3 pwr dn fallback mode to standby

1D_00C0001_1211 // set bank 3 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_0100000_FF09 // set bank 4 pwr dn fallback mode to standby

1D_0100001_1211 // set bank 4 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_0140000_FF09 // set bank 5 pwr dn fallback mode to standby

1D_0140001_1211 // set bank 5 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_0180000_FF09 // set bank 6 pwr dn fallback mode to standby

1D_0180001_1211 // set bank 6 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_01C0000_FF09 // set bank 7 pwr dn fallback mode to standby

1D_01C0001_1211 // set bank 7 Wait times WTBSLEEP,WTPAGE,WTREAD

1D_000F000_0018 // set pump MAC1 Register for Pump WTBSLEEP

1D_000F002_FFFF // set PAGP to max

1D_000F001_00C1 // set pump pwr dn fallback mode to standby

3.3.2 Power Up Behavior

During the power up sequence, the flash pump module will hold a “SAFE” signal in a low state. This signal will indicate to all the flash banks that it is not yet safe to power up. This feature can be used to inhibit the SM28LVT32 from consuming standby current if it is not needed at power up. The SAFE signal cannot propagate to the flash bank unless there is a FCLK, and reset is de-asserted. If it is desired to keep the device from consuming current prior to changing to the current fallback mode , the device can simply be held in reset, or inhibit the clock after power-up. Note that after device is operational after powerup, re-asserting reset or inhibiting clocks will not cause SAFE signal to be de-asserted and lower power consumption. This condition can only be achieved after power up.

3.3.3 Implications of Using Power Saving Features

Using the low power features of the SM28VLT32 introduces some additional burden to the host to make sure that the device is operating as expected. Both writing to the array and reading from a sleeping bank will be impacted.

3.3.4 Write Protocol Implications

Writing to the arrays is not significantly impacted from a protocol standpoint. If a bank/pump is sleeping and a program command is initiated, the SM28VLT will automatically begin the wake up process and complete programming without further need for host to be involved. The process will take longer, as the device will be busy during the wake and actual programming process. The polling of quick status can occur exactly the same as if the device was not sleeping. The only real impact is that it will take longer to complete the write.

3.3.5 Read Protocol Implications

Reading from the array when the array is in a lower power mode is impossible. The read command returns the result in the same command. The action is not queued up as in a write. The flash pump and/or the bank being accessed cannot wake up and process this within the time for a read command. In this case, the read error will be set and the actual data that is returned from the read command needs to be discarded.

There are two ways this can be handled. If the host is capable of accessing the array fast enough to be within the active grace period, then the read error can be ascertained and immediately re-issue the same read. The bank and pump will be awake at this time, and the read will complete as expected. However, if the host is not quick enough to evaluate the read error and re-issue the read command before the active grace period expires then the device will be back to sleep before command is processed properly. The active grace period can be set to a max value of 256 for a bank. This will represent 256 fclks. At 12MHz, this is 21.3µs.

If the host cannot handle this case, or if it cannot handle it under all cases, it would be recommended to place the bank being accessed to active mode prior to the read operation. This is accomplished by setting the bank fallback mode to active. As the read process completes, or if address transitions to a new bank, the old bank can be put back to fallback mode of sleep while the new bank is set to active fallback.

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