Power-Up Behavior of Clocked Devices

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ABSTRACT

Some logic devices, such as flip-flops and shift registers, require the use of a clock input, typically designated CLK or CP. The state of the outputs of these devices change once an appropriate clock edge has occurred. Device datasheets specify whether the action occurs on a positive or negative edge of the clock. However, the behavior of a device upon power-up is not always specified **before** a valid clock edge has occurred.

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The CD74HC4094 is an example of a device that does not have guaranteed output levels upon power-up. Before a valid clock edge, thresholds within the device can cause the internal logic chains to product high or low signals. This effect can vary with voltage, temperature, manufacturing lot, and more. As a result, the outputs Q_n will be determined by unpredictable power-up states determined by these internal thresholds and should **not** be considered valid logic signals. However, once a valid clock edge has occurred, the outputs behave normally according to the truth table in the datasheet. For this particular device, 8 clock edges are required to shift the unknown data out of the device and ensure that all Q_n outputs are valid.

Another important consideration is the rise of the CLK signal simultaneously with V_{CC}. Although the clock signal will be seen as an appropriate edge on an oscilloscope, the device may not consider it a valid clock. As V_{CC} rises, the V_{IH} threshold of the clock signal also rises. If the two rise simultaneously, the clock signal may or may not cross the appropriate thresholds required to be considered valid. Capacitance within the circuit will also cause subtle and unpredictable differences in the timing of CLK and V_{CC}. Therefore, it is not recommended to produce a clock edge until V_{CC} has risen to a recommended level as specified in the device datasheet.

2   Solutions to Unknown States at Power-Up

There are several methods that designers can use to prevent unwanted signals at power-up from affecting their systems.

Use a Device with Clear or Preset Pins

Some devices come with input pins designed to ensure a specific state upon power up. For example, an alternative to the CD74HC4094 is the CD74HC299, which contains a Master Reset ($\overline{MR}$) pin, which sets all outputs low when the pin is pulled low. The outputs will be set low regardless of the state of the clock pulse (see the truth table in the datasheet). Other devices, such as the SN74HC74, have clear ($\overline{CLR}$ or CLR) and preset ($\overline{PRE}$ or PRE) pins. When active, the clear pins set the outputs low, and the preset pins set the outputs high, regardless of CLK. The polarities of the clear and preset pins vary among different parts, and it is typically not recommended to activate both of them at the same time (nonstable configuration). The truth table in the device datasheet specifies which configurations are not recommended.

The example in Figure 1 shows a configuration where the user wants an initial high output at Q. According to the truth table, this requires a high $\overline{CLR}$ and a low $\overline{PRE}$. Use pullup resistors to connect the inputs to the appropriate levels. After power-up, the truth table says that $\overline{PRE}$ must then be pulled high to allow Data and CLK to control the output. The pullup resistor must be sized such that the device driving $\overline{PRE}$ can overdrive the pullup resistor while keeping $\overline{PRE}$ above its V_{IH} level.
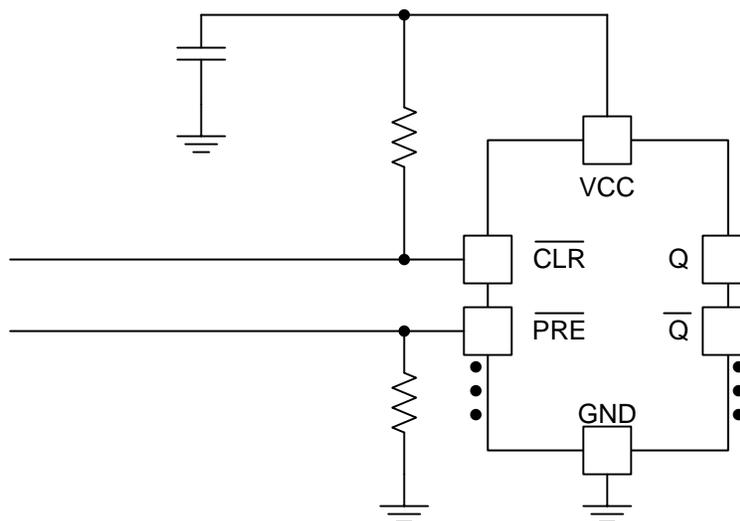

Figure 1. SN74HC74 Partial Schematic for High Power-Up Output at Q

Wait Until V$_{CC}$ Has Ramped

Another method for ensuring outputs is to wait until V$_{CC}$ has ramped to an appropriate level before a clock edge occurs. If the application requires that CLK rise with V$_{CC}$, the user should wait one extra clock cycle to ensure valid outputs. For example, this means waiting for 9 clock pulses for the CD74HC4094 instead of the 8 mentioned earlier.

Delay the Clock Edge with an RC Circuit and Schmitt Trigger Buffer

An alternative to waiting for V$_{CC}$ to ramp is to add an RC circuit and Schmitt Trigger (Figure 2) buffer to delay the clock pulse. Design the RC for an appropriate time constant, which will depend on the signal frequency and desired CLK delay. The CLK signal behind the Schmitt Trigger will rise slowly, and the Schmitt Trigger will convert the slower edge to a fast edge. The resulting CLK signal coming out of the Schmitt Trigger will be delayed by a small amount. A weak pulldown on the output of the Schmitt Trigger may be necessary to avoid floating the CLK input. The pulldown resistor is not necessary if the device has Bus Hold.
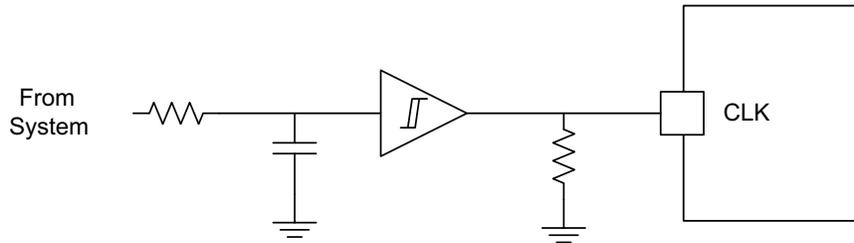
Figure 2. Schmitt-Trigger Clock Delay Circuit

Revision History

Changes from Original (January 2015) to A Revision	Page

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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