Advanced High-Speed CMOS (AHC) Logic Family

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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Introduction

The Texas Instruments (TI™) advanced high-speed CMOS (AHC) logic family provides a natural migration for high-speed CMOS (HCMOS) users who need more speed for low-power, and low-drive applications. Unlike many other advanced logic families, AHC does not have the drawbacks that come with higher speed, e.g., higher signal noise and power consumption. The AHC logic family consists of gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC™ process that features higher performance than the HCMOS HC product family at comparable cost.

This application report introduces the AHC logic family characterization information to supplement the AHC/AHCT Logic Advanced High-Speed CMOS Data Book, literature number SCLD003A. The additional information is to aid design engineers in more accurately designing their digital logic systems. The focus is on the family's features and benefits, product characteristics, and design guidelines. This application report is divided into sections, each dealing with a specific characteristic of the AHC logic family. This application report focuses on the AHC logic family and compares it to the HC family.

The main topics discussed are:

- High-Speed CMOS (HC)
- Advanced High-Speed CMOS (AHC)
- Protection Circuitry
- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- AHC Versus HC
- Advanced Packaging
- Microgate Logic

For more information on TI's AHC logic products, please contact your local TI field sales office or an authorized distributor, or call TI at 1-800-336-5236.

High-Speed CMOS (HC)

HC has the following characteristics:

- The HC family covers a wide range of applications: low power drain for low-speed systems, and a slightly higher drain for higher-speed systems.
- The HC family has ac parameters ensured at supply voltages of 2 V, 4.5 V, and 6 V over the full operating temperature range into a 50-pF load. The TTL compatible version, HCT, is specified for a 4.5-V to 5.5-V V_{CC} range.
- In HC, only the gates that are switching contribute to the dynamic system power. This reduces the size of the power supply required, thus providing lower system cost and higher reliability through lower heat dissipation.
- HC devices are ideal for battery-operated systems, or systems requiring battery backup because there is virtually no static power dissipation.
- Improved noise immunity is due to the rail-to-rail (V_{CC}-to-ground) output voltage swings.
- HC devices are warranted for operation over an extended temperature range of –40°C to 85°C.

Advanced High-Speed CMOS (AHC)

AHC can be used for higher-speed applications. Some advantages of using AHC over HC are:

- The AHC logic family is almost three times faster than the HC family. The AHC logic family has a typical propagation delay of about 5.2 ns.
- The AHC logic family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices.
- The AHC family has lower power consumption than the HC family.
- The output drive is ±8 mA at 5-V V_{CC} and ±4 mA at 3.3-V V_{CC}.
- AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), PW (TSSOP), and DGV (TVSOP) packages. Selected AHC devices are available in military versions (SN54AHCxx).
- Microgate Logic (single-gate) versions that simplify routing are also available.

Protection Circuitry

Electrostatic discharge (ESD) and latchup are two traditional causes of CMOS device failure. To protect AHC devices from ESD and latchup, additional circuitry has been implemented at the inputs and outputs of each device.

Electrostatic Discharge

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. The end effect is the ESD causes a short between the two surfaces. These damaged devices might pass normal data sheet tests, but eventually fail. The input and output protection circuitry designed by TI provides immunity to over 2000 V in the human-body-model test, over 200 V in the machine-model test, and over 1000 V in the charged-device model test.

Figure 1 shows the circuitry implemented to provide protection for the input gates against ESD. The primary protection device is a low-voltage-triggered silicon-controlled rectifier (LVTSCR). During an ESD event, most of the current is diverted through the LVTSCR. Additional protection is provided by the resistor and secondary clamp transistors, which break down during an ESD event and protect the gate oxides.

Figure 2 shows how the LVTSCR protects an output.

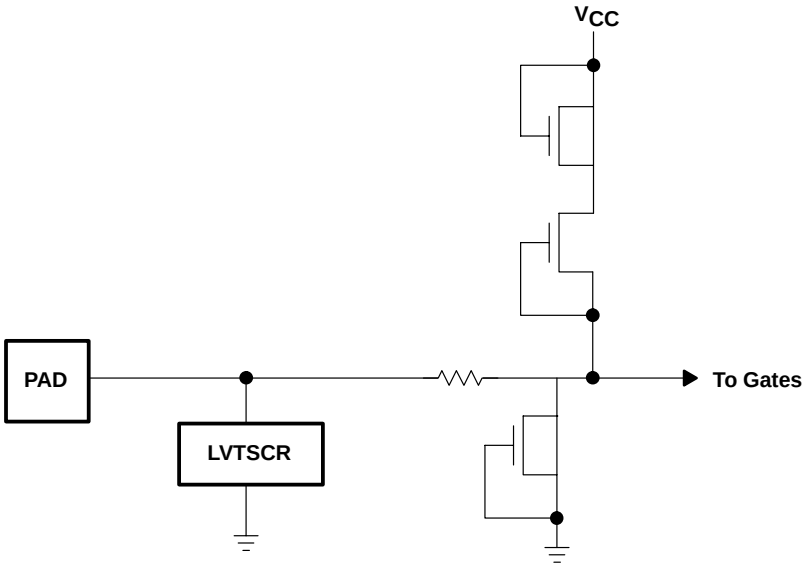

Figure 1. ESD Input Protection Circuitry

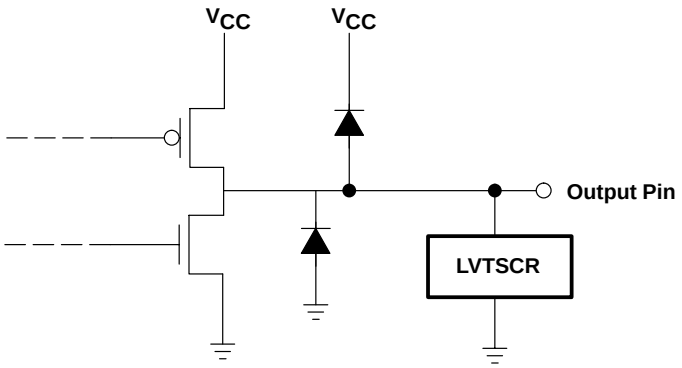

Figure 2. ESD Output Protection Circuitry

Latchup Protection

Internal to almost all CMOS devices are two parasitic bipolar transistors; one p-n-p and one n-p-n. Figure 3 shows the cross section of a typical CMOS inverter with the parasitic bipolar transistors. As shown in Figure 4, these parasitic bipolar transistors are naturally configured as a thyristor or a silicon-controlled rectifier (SCR). These transistors conduct when one or more of the p-n junctions become forward biased. When this happens, each parasitic transistor supplies the necessary base current for the other to remain in saturation. This is known as the latchup condition and could destroy the device if the supply current is not limited.

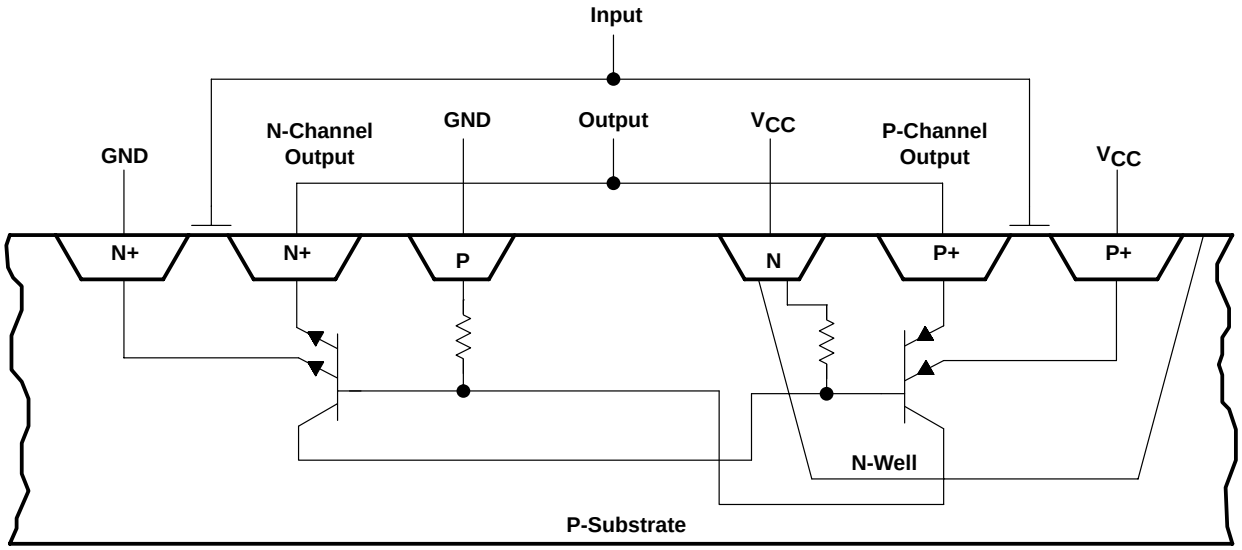

Figure 3. Parasitic Bipolar Transistors in CMOS

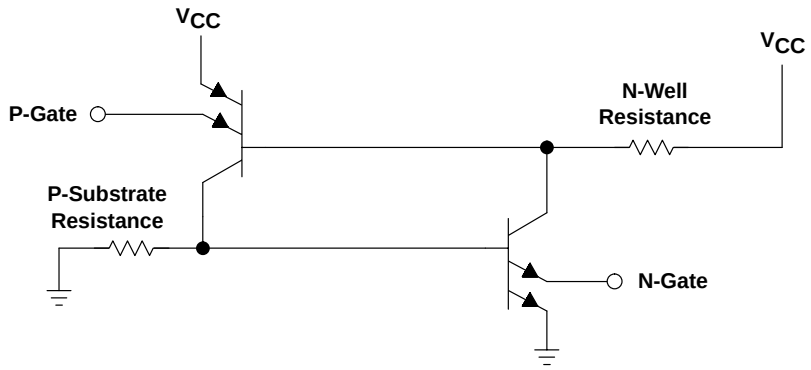

Figure 4. Schematic of Parasitic SCR Showing P-Gate and N-Gate Electrodes Connected

A conventional thyristor is fired (turned on) by applying a voltage to the base of the n-p-n transistor, but the parasitic CMOS thyristor is fired by applying a voltage to the emitter of either transistor. One emitter of the p-n-p transistor is connected to an emitter of the n-p-n transistor, which is also the output of the CMOS gate. The other two emitters of the p-n-p and the n-p-n transistors are connected to V_{CC} and ground, respectively. Therefore, to trigger the thyristor there must be a voltage greater than V_{CC} + 0.5 V or less than –0.5 V and there has to be sufficient current to cause the latchup condition.

Latchup cannot be completely eliminated. The alternative is to prevent the thyristor from triggering. TI has improved the circuit design by adding an additional diffusion or guard ring. The guard ring provides isolation between the device pins and any p-n junction that is not isolated by any transistor gate.

Switching Characteristics

The switching characteristics of the AHC are similar to those of the AHCT in terms of the operating conditions and limits, except for the AHCT input TTL compatibility. Table 1 gives the performance figures for the HC/HCT and the AHC/AHCT logic parts. Individual data sheets provide parameter values for the AHC and the AHCT devices for different values of operating free-air temperature, number of outputs switching, and load capacitance.

Table 1. HC and AHC Performance Comparison (Typical Values)

DEVICE	SN74HC	SN74HCT	SN74AHC	SN74AHCT
244 buffer	13 ns	15 ns	5.8 ns	5.4 ns
245 transceiver	15 ns	14 ns	5.8 ns	4.5 ns
373 latch	15 ns	20 ns	5 ns	5 ns
374 flip-flop	17 ns	25 ns	5.4 ns	5 ns

AHC is almost three times faster than HC.

Power Considerations

The power dissipation of CMOS devices can be divided into three components:

- Quiescent power dissipation, P_q
- Transient power dissipation, P_t
- Capacitive power dissipation, P_c

The quiescent power is the product of V_{CC} and the quiescent current, I_{CC}. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current is generally very small (a few nA), which makes the quiescent power insignificant. However, for circuits that are in static condition for long periods, the quiescent power must be considered.

The transient power is due to the current that flows only when the transistors are switching from one logic level to the other. During this time, both of the transistors are partially on, which produces a low-impedance path between V_{CC} and ground that results in a current spike. The rise (or fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal passes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise and fall times of the input signal. The component can be calculated using the following equation:

$$P_t = C_{pd} \times V_{CC}^2 \times f_I \quad \textbf{(1)}$$

Where:

V_{CC} = Supply voltage (V)
f_I = Input frequency (Hz)
C_{pd} = Power dissipation capacitance (F)

Additional capacitive power dissipation is caused by the charging and discharging of external load capacitance and is dependent on the switching frequency. To calculate the power, the following equation can be used:

$$P_C = C_L \times V_{CC}^2 \times f_O \quad \textbf{(2)}$$

Where:

V_{CC} = Supply voltage (V)
f_O = Output frequency (Hz)
C_L = External load capacitance (F)

Power Dissipation

AHCT devices are used primarily to interface TTL output signals to CMOS inputs. To make the inputs of the AHCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption, as compared to the equivalent AHC device, if the input is kept at a level other than GND or V_{CC}. The increase in power consumption occurs because TTL input levels cause both transistors in the transistor pair to be partially turned on. Included in the tables for the AHCT devices is the parameter ΔI_{CC}, which enables the designer to compute how much additional current the AHCT device draws per input when at a TTL-voltage level.

Figure 5 shows the relation between the supply current and the frequency of operation for the AHC245 and the AHCT245. The increase in power consumption for the AHCT is relatively insignificant.

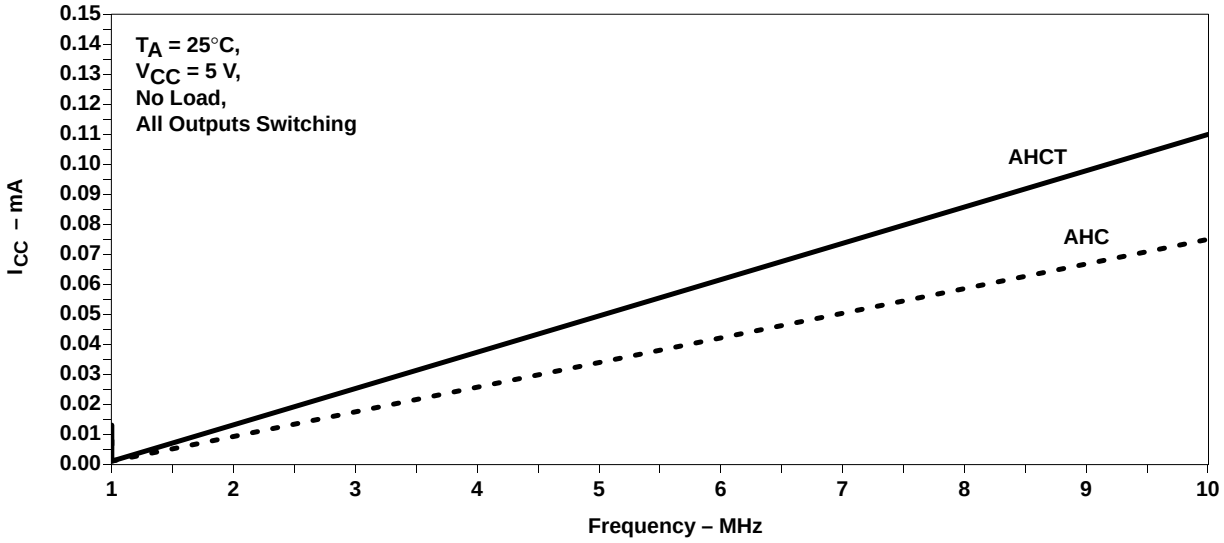

Figure 5. I_{CC} Versus Frequency

Input Characteristics

The AHC logic family input structure is such that the 5-V CMOS dc V_{IL} and V_{IH} fixed levels of 1.5 V and 3.5 V are ensured, meaning that, while the threshold voltage of 2.5 V is typically where the transition from a recognized low input to a recognized high input occurs, it is at 1.5 V and 3.5 V that the corresponding output levels are specified. For AHCT, V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V are ensured, and the threshold voltage is 1.5 V. Figure 6 shows the characteristics for the AHC245 and the AHCT245.

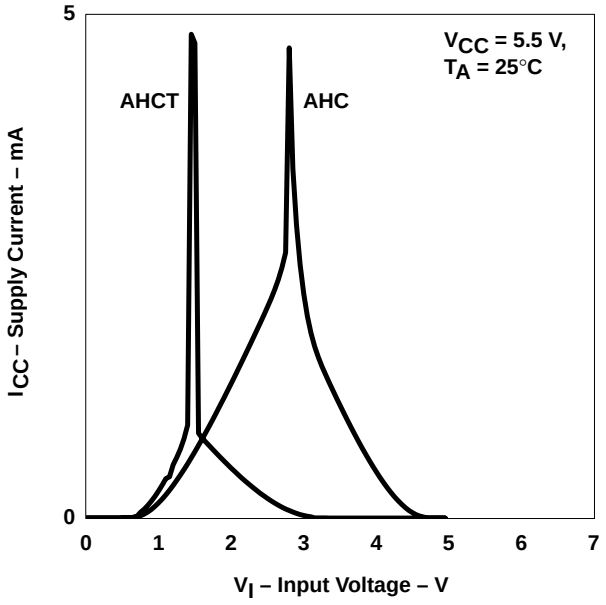

Figure 6. Supply Current Versus Input Voltage

AHC Input Circuitry

The simplified AHC input circuit shown in Figure 7 consists of two transistors, sized to achieve a threshold voltage of 2.5 V. Since V_{CC} is 5 V and the threshold voltage is commonly set to be centered around one-half of V_{CC} in a pure CMOS input, additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage V_I is low, the PMOS transistor (Q_p) turns on and the NMOS transistor (Q_n) turns off, causing current to flow through Q_p, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when V_I is high, Q_n turns on and Q_p turns off, causing current to flow through Q_n, resulting in the output voltage (on the input stage) to be pulled low.

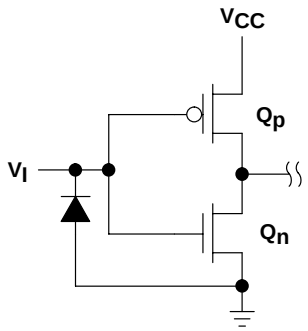

Figure 7. Simplified Input Stage of an AHC Circuit

Figures 8 and 9 show the graphs of V_O versus V_I for the AHC04 and the AHCT04. The recommended operating range for the AHC family is from 2 V to 5.5 V. For the AHCT the recommended range is from 4.5 V to 5.5 V. Input hysteresis of typically 150 mV is included in AHC devices (300 mV in AHCT devices), which ensures the devices are free from oscillations by increasing the noise margin around the threshold voltage during low-input transitions.

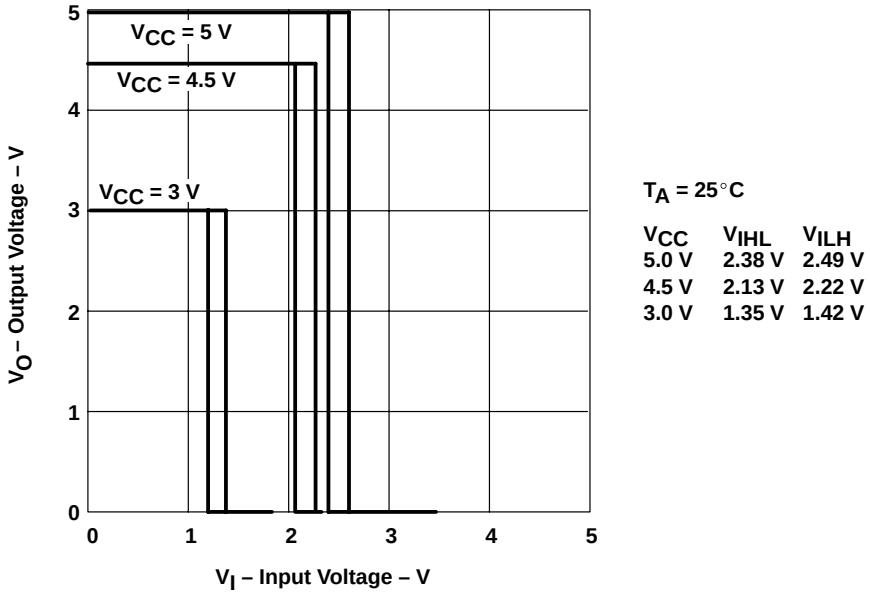

Figure 8. Output Voltage Versus Input Voltage (AHC04)

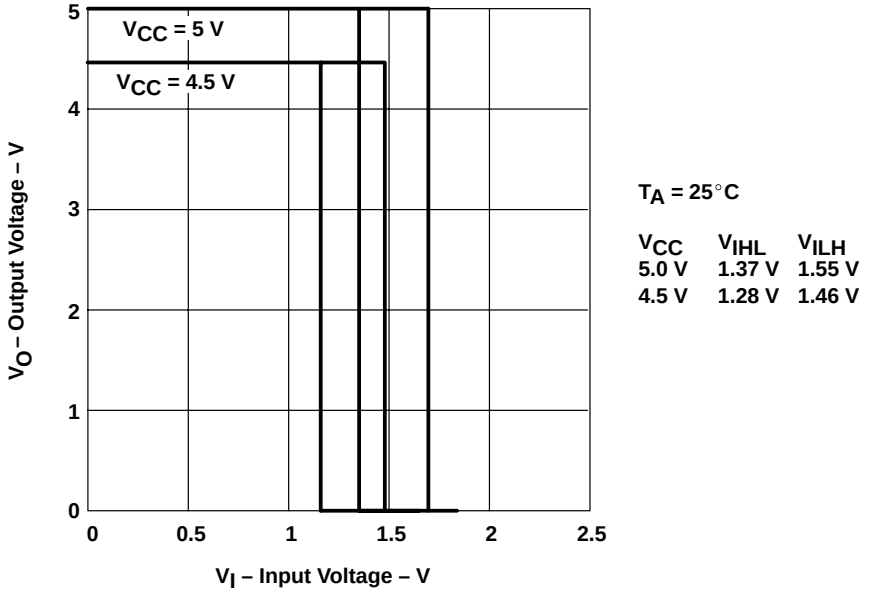

Figure 9. Output Voltage Versus Input Voltage (AHCT04)

Input Current Loading

Minimal loading of the system bus occurs when using the AHC family due to the EPIC process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 1 μA (see Table 2). Capacitance for transceivers can be as low as 2.5 pF for C_i and 4 pF for C_{io}. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using AHC devices is minimal and, depending on the logic family being used, bus loading can decrease as a result of using AHC parts.

Table 2. Input-Current Specification

PARAMETER	TEST CONDITIONS		SN74AHC245		UNIT
			MIN	MAX	
I_I	$V_I = V_{CC}$ or GND			±1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND,	$V_I = (\overline{OE}) = V_{IL}$ or V_{IH}		±2.5	μA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

Supply Current Change (ΔI_{CC})

Because the input circuitry for AHC is CMOS, an additional specification, ΔI_{CC}, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting (see *Power Dissipation* in the application report). Although this situation exists when a low-to-high or high-to-low transition occurs, the transition usually occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the AHC part. Here, a dc voltage that is not at the rail is applied to the input of the AHC device. This results in both the n-channel transistor and the p-channel transistor conducting, and a path from V_{CC} to GND is established. This current is specified as ΔI_{CC} in the data sheet for each device and is measured one input at a time, with the input voltage set at $V_{CC} - 0.6$ V, while all other inputs are at V_{CC} or GND. Table 3 provides the ΔI_{CC} specification, which is contained in the data sheet for the SN74AHCT245.

Table 3. ΔI_{CC}-Current Specification

PARAMETER	TEST CONDITIONS	SN74AHCT245		UNIT
		MIN	MAX	
ΔI_{CC}	One input at 3.4 V, Other inputs at V_{CC} or GND, V_{CC} = 5.5 V		1.5	mA

Figure 10 is a graph of I_I versus V_I for the AHC245. An operating range from 0 V to 5.5 V is recommended.

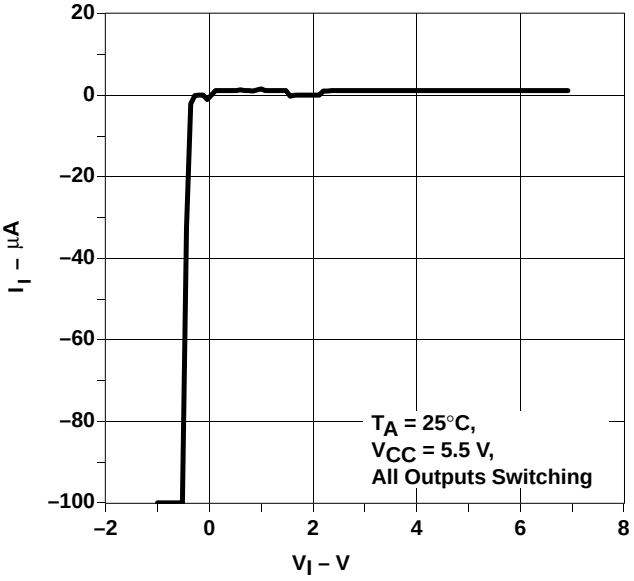

Figure 10. Input Current Versus Input Voltage (AHC245)

DC Characteristics

The AHC family uses a pure CMOS output structure. The AHC family has the dc characteristics shown in Table 4. The values are measured at T_A = 25°C.

Table 4. AHC DC Specifications

PARAMETER	TEST CONDITIONS		V_{CC}	SN74AHC245 T_A = 25°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA		2 V	1.9	2		V
			3 V	2.9	3		
			4.5 V	4.4	4.5		
	I_{OH} = –4 mA		3 V	2.58			
	I_{OH} = –8 mA		4.5 V	3.94			
V_{OL}	I_{OL} = 50 μA		2 V			0.1	V
			3 V			0.1	
			4.5 V			0.1	
	I_{OL} = 4 mA,		3 V			0.36	
	I_{OL} = 8 mA,		4.5 V			0.36	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND,	V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2.5		pF
C_{io}	$V_I = V_{CC}$ or GND		5 V		4		pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

AHC/AHCT Output Circuitry

Figure 11 shows a simplified output stage of an AHC/AHCT circuit. When the NMOS transistor (Q_n) turns off and the PMOS transistor (Q_p) turns on and begins to conduct, the output voltage (V_O) is pulled high. Conversely, when Q_p turns off, Q_n begins to conduct and V_O is pulled low. The AHC/AHCT devices have a rail-to-rail output swing to make them compatible with the HC/HCT families.

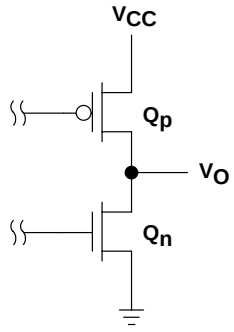

Figure 11. Simplified Output Stage of an AHC Circuit

Output Drive

Figure 12 shows values for V_{OL} vs I_{OL}, and I_{OH} vs V_{OH} for the AHC/AHCT245.

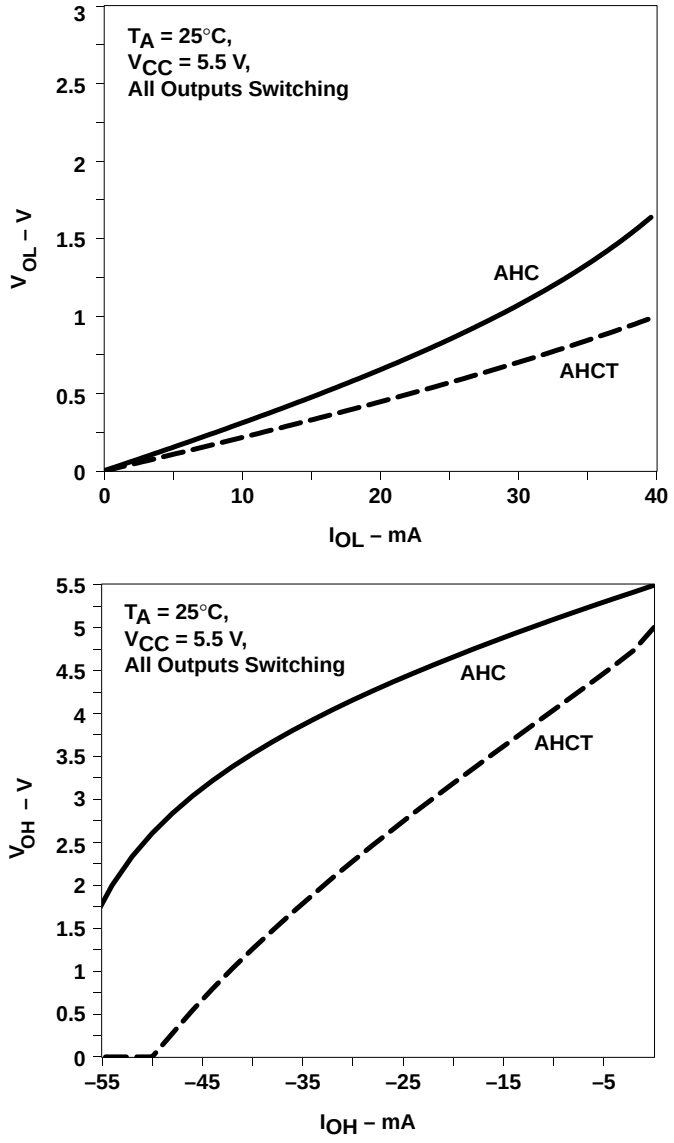

Figure 12. AHC Output Characteristics

Partial Power Down

All AHC devices are 5-V input tolerant when operated at 3.3 V. To partially power down a device, no paths from the input or output pins to V_{CC} exist. With the AHC family, there are no paths from the input pins to V_{CC}. The AHC/AHCT devices have rail-to-rail output swings to make them compatible with the HC/HCT family. The AHC/AHCT devices do not have a path from the output pins to V_{CC} and can be partially powered down.

Proper Termination of Outputs

Depending on the trace length, special consideration might need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system might appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

Common Termination Techniques

Most transmission-line termination techniques rely on impedance matching at either the source or receiver to reduce reflections and line noise (see Figure 13). Series, thevenin, and ac techniques commonly are used and are effective methods of line termination for high-speed logic. Shunt termination is educational, but has implementation problems. Diodes can be used as a solution, but, generally, this is not a good termination technique by itself.

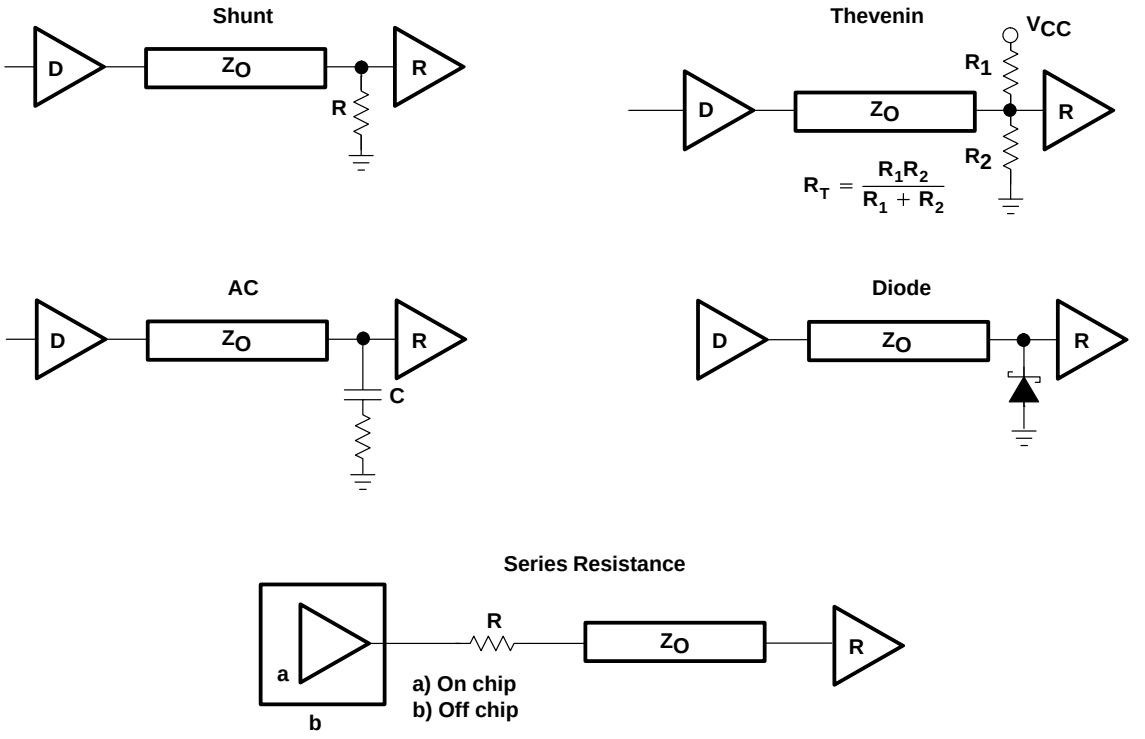

Figure 13. Termination Techniques

Shunt

Shunt termination (see Figure 13) is one of the simplest termination techniques to implement. The value of the termination resistor should match the line impedance for best performance. As the transmitted signal reaches the receiver, the shunt termination drains off the current with an impedance matching the transmission line. There is no reflection, thus, no noise is retransmitted down the transmission line.

There are several disadvantages to shunt termination. Usually the line impedance is fairly low (50 Ω to 70 Ω), which requires a resistor of similar value. This causes a heavy dc current drain on the source when in the logic high state and requires a strong line driver to source the current. With the low-impedance resistor pulling to GND, the V_{OH} of the transmission line is lower, reducing the noise immunity at the receiver. Additionally, having a strong pull down on the transmission line might unbalance the rising and falling edges of the signal, causing the falling edge to be faster than the rising edge, resulting in duty-cycle distortion of the signal.

AC

AC termination utilizes the same line-impedance-matching resistor as shunt termination, except it is ac coupled with a capacitor, making a simple high-pass filter. The capacitor appears to be a short circuit during signal transitions when termination is needed, but eliminates the dc component of the current drain.

AC termination (see Figure 13) has the precise termination advantages of shunt termination, but reduces the disadvantages of dc current drain and waveform distortion. At each transition of the signal, the capacitor charges up to the voltage level necessary to maintain zero volts across the resistor. During the arrival of the next input transition, the signal drives the full value of the resistor until the capacitor can again recharge.

It is recommended that the resistor value be equivalent to the line impedance. The ideal capacitor value varies with line impedance, edge rate, and desired signal quality. The values are not critical, but tests have shown that with TI logic, a value of 50 pF for the capacitor is a good compromise. Increasing the capacitance value to 200 pF improves signal quality, but sacrifices power dissipation. Reducing the value to 47 pF lowers the power dissipation, but sacrifices signal quality. Values below 47 pF give a very high frequency response to the filter and tend to be ineffective for line termination. Values above 200 pF add power dissipation without additional signal quality improvement. AC termination is excellent for use with clock drivers, cables, backplanes, distributed loads, and many other applications. The combined cost of the capacitor, resistor, and real estate for each line frequently precludes general use for on-board bus termination.

Thevenin

Thevenin termination (see Figure 13) attempts to correct the dc problems of shunt termination by reducing the dc load of the termination and pulling the signal closer to the center of the transition. For high-speed logic, it is best to center the dc level at a logic high (>2.0 V) to avoid holding the input at the input threshold (toggle point »1.5 V). Under this condition, if the driver shuts off (high Z), the input pulls up rather than causing oscillations from logic uncertainties.

A disadvantage of thevenin termination is the dc leakage from V_{CC} to GND through the terminator. Using thevenin termination to match a 50- or 70-Ω line requires a parallel resistance that is low enough to pass considerable current. Thevenin is commonly used on backplanes, cables, and other long transmission lines. Some applications, such as backplanes, might require termination at both ends of the transmission line.

Diode

Diode termination (see Figure 13) simply clips the undershoot of a high-to-low transitioning signal and thereby reduces the line reflection. Diode termination can be effective if the cause of the problem is undershoot and the frequency response of the diode is considerably higher than the transition frequency of the signal.

With very-high-speed logic families, such as TI's, the frequency response of the output-signal transition can reach 400 MHz and beyond. At these frequencies, the effectiveness of diode termination is limited due to the frequency response of the terminator. While some benefit might be realized with diode termination, the inductances, capacitances, and frequency response of the diode and diode connections probably make the termination scheme less effective when used at high frequencies.

The internal parasitic clamp diode to ground, found on the inputs and outputs of all CMOS logic, bleed off some of the overshoot current, but this parasitic clamp does not have the necessary frequency response to perform effective diode termination in high-speed applications. Diode termination frequently is used on backplanes and long cables, possibly in conjunction with another form of line termination.

Series (Source Terminated)

Series termination reduces the output edge rate of the driver, the switching amplitude of the signal, and the charge injected into the transmission line. This has significant benefits by reducing signal line noise and electromagnetic interference (EMI). Series termination adds a series resistor at the output of the line driver, effectively increasing the source impedance of the driver (see Figure 13). When using series termination with distributed loads, care must be taken that the combined output impedance of the driver and series resistor is small enough to allow first incident-wave switching. If the output impedance becomes too high, the step that is seen in the output transition does not toggle the components at the near end of the transmission line until the signal passes down the line and returns to the source, causing an unnecessary propagation delay. Series termination is the most commonly used form of termination and is found on circuit boards, cables, and in most other applications.

Table 5 provides a comparison of the five termination techniques.

Table 5. Termination Techniques Summary

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	DELAY	HOLDS DEFINED LEVEL	IDEAL VALUE†	COMMENTS
Shunt	1	Significant	No	Yes	$R = Z_O$	Low dc noise margin
Thevenin	2	Yes	No	Yes	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
AC	2	Yes	No	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series resistor on device	0	No	Small	No	$25 = < R = < 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

† Symbols are defined in Figure 13.

Signal Integrity

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

Simultaneous Switching

In a digital circuit, when multiple outputs switch, the current through the ground or V_{CC} terminals changes rapidly. As this current flows through the ground (or V_{CC}) return path, it develops a voltage across the parasitic inductance of the bond wire and the package pin. The phenomenon is called simultaneous switching noise. Figure 14 shows the equivalent circuit of a typical CMOS output buffer stage with the package parasitics and the external load. The parasitic components that affect the ground bounce are inductance and resistance of the ground bond wire and pin, inductance and resistance of the output bond wire and pin, and load impedance. For the first-order analysis, the parasitics associated with the V_{CC} terminal can be ignored. Also, the external ground plane is assumed to be ideal.

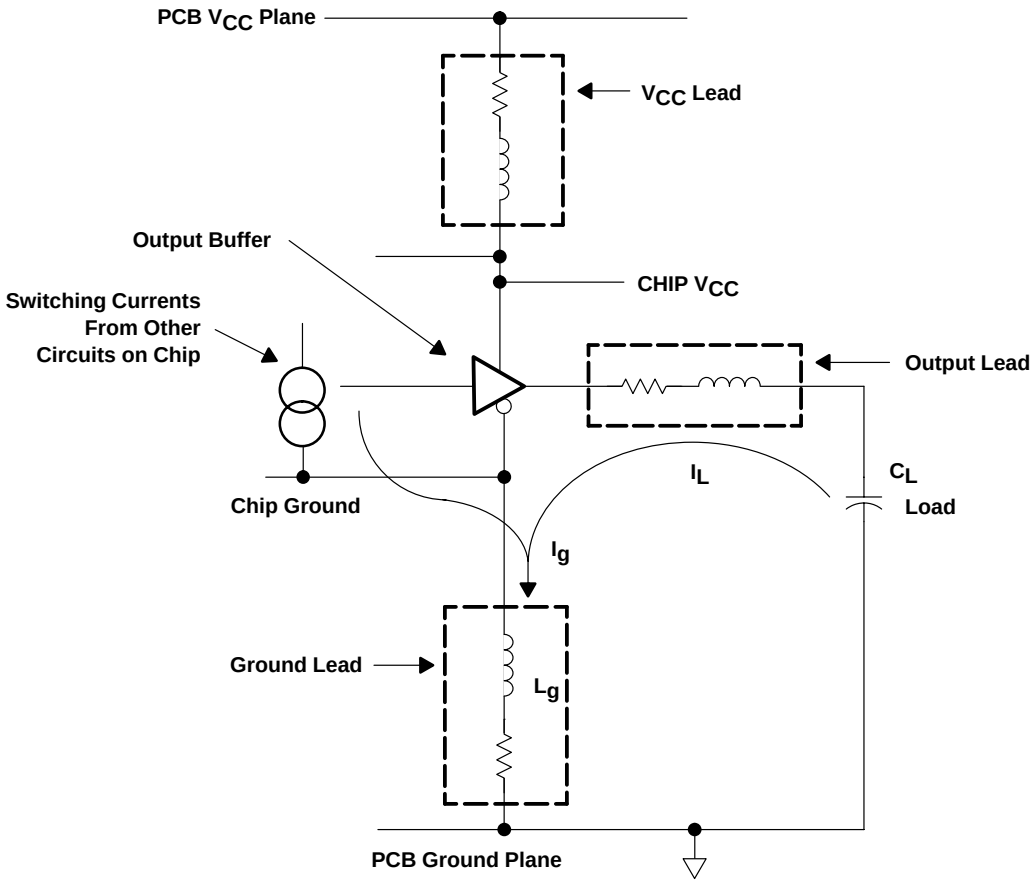

Figure 14. Output Buffer With External Parasitics

During the output high-to-low transition, the sum of the output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance and causes a positive ground bounce or an overshoot in an otherwise quiet ground. This positive ground bounce is normally followed by an undershoot coincident with the voltage waveform on the output terminal. The amplitudes of both the positive and the negative ground bounce are a function of $L_g * di/dt$ and of the number of outputs switching simultaneously (SS noise). The ground-bounce phenomenon can be clearly observed at an unswitched low output of a device by switching several other outputs simultaneously from logic high to low. Figure 15 shows the typical output voltage transition and the corresponding ground bounce, as observed at the unswitched low output. Positive ground bounce is primarily the result of the rate of change of current (di/dt) through the ground lead inductance. The rate is determined by the rate at which the gate-to-source voltage (V_{gs}) of the sink transistor changes. During the early part of the fall time, the ground voltage rises while the output voltage falls, forcing the sink transistor into the linear region. The transistor then behaves like a resistor R_{on} (the on-state resistance of the transistor in the linear region). For the remainder of the output voltage excursion, the equivalent circuit at the output can be treated like a resonant L-C-R circuit formed by the ground and the output lead inductance, load capacitance, and the total resistance in the loop, which includes R_{on}. The oscillation frequency is determined by the net values of L and C, while damping is determined by L and the total resistance in the loop. Ground bounce also is generated during the output low-to-high transition. However, the magnitude of this ground bounce is much smaller because of the absence of load current in the ground lead.

Ground and V_{CC} bounce cannot be eliminated, but they can be minimized by controlling edge rates and reducing output swing. Ground bounce depends on many factors, with device speed being one of the more important influences. As device speed goes up, the rate of change of current in the parasitic inductances increases and the related switching noise goes up. Due to this correlation between speed and ground bounce, high-speed logic families arouse increased concern over noise due to simultaneous switching of outputs.

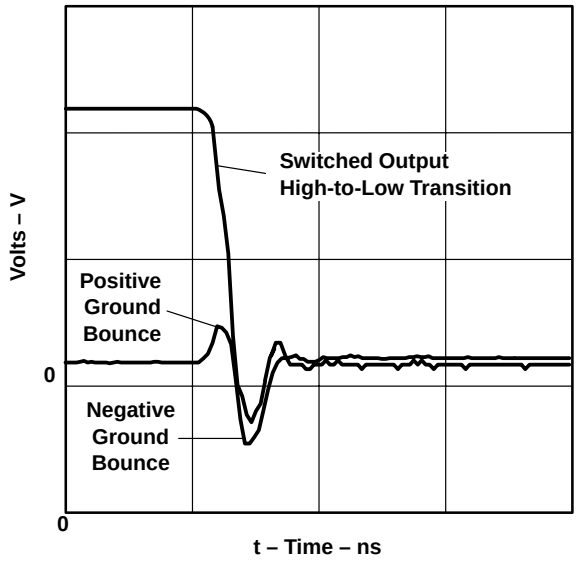

Figure 15. Simultaneous-Switching-Noise Waveform

Ground-Bounce Measurement

There is no industry standard for measuring ground bounce. However, the method most commonly used by IC vendors and customers is based on observing the disturbance of a logic-low level on an unswitched output of a multiple-output device while switching all other outputs from a high to a low state. Figure 16 shows the schematic for measuring ground bounce on a device such as the AHC244 octal buffer. One output is in the low state while the outputs are switched simultaneously. The load on each output consists of a 50-pF capacitor. Two outputs are connected to the oscilloscope: one for observing the high-to-low transition of a switched output and the other for observing the ground bounce on the quiet output.

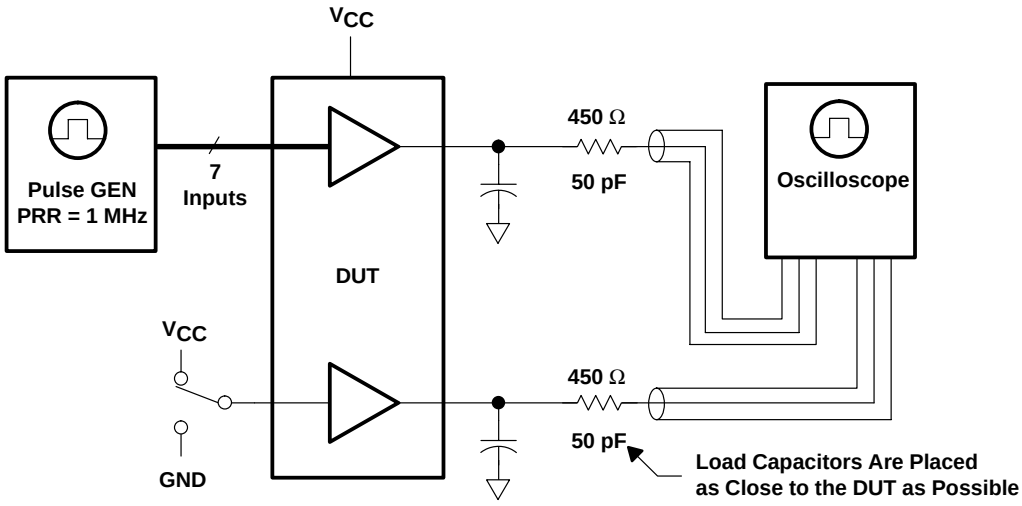

Figure 16. Ground-Bounce Test Circuit

With careful layout, proper bypassing to filter out high-frequency noise, and good oscilloscope probes, it is possible to observe the ground bounce on the internal ground of the chip by observing the voltage at the unswitched low output, whose sink transistor operates in the linear region and provides a Kelvin connection to the chip ground.

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip (see the *Advanced Packaging* section of this application report). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing*, in the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001B.

AHC Versus HC

A speed-versus-current-drive comparison between the AHC and HC families is shown in Figure 17. The speed for the AHC is much higher than the HC. Both these products support low-drive applications.

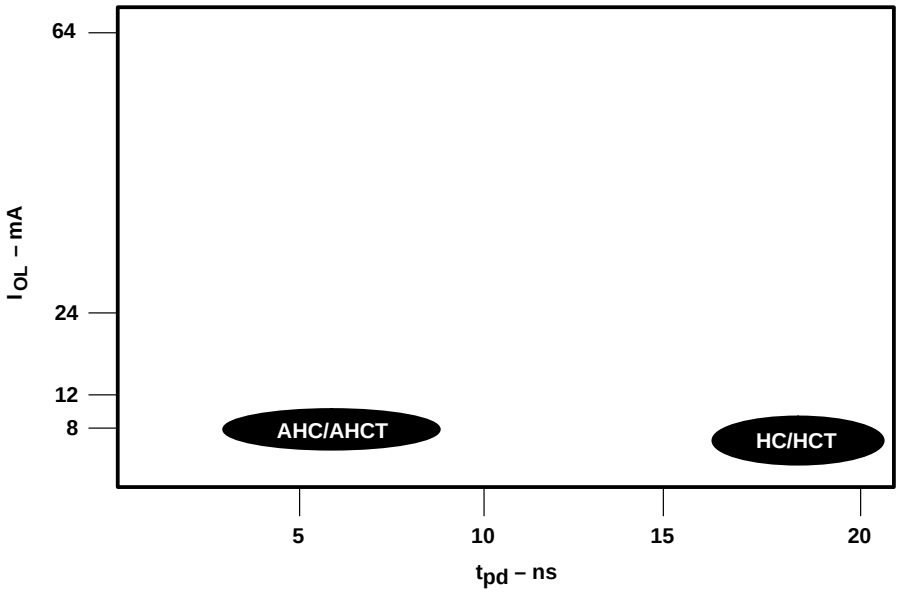

Figure 17. AHC/AHCT and HC Family Positioning

Table 6 shows the features of HC and AHC families. AHC provides much higher speeds with no noise penalty.

Table 6. AHC and HC Features (Typical Values)

PRODUCT FAMILY		AHC	HC
Technology		CMOS	CMOS
5-V tolerant†		Yes (inputs)	No
Octals and gates		Yes	Yes
Widebus™ (16-bit products)		Yes	No
Bus hold		Yes	No
Damping resistors		No	No
I_{CC}	’245	40 μA	80 μA
DC output drive		–8 mA/8 mA	–8 mA/8 mA
t_{pd}	’245	5 ns	18 ns
C_i	’245	2.5 pF	3 pF
C_{io}	’245	8 pF	10 pF

† When operated at 3.3 V

Advanced Packaging

Figure 18 shows a comparison of packages in which AHC devices are available; for ease of analysis, 14-pin packages and 20-pin packages are included. Figure 19 is not an all-inclusive list of pin counts and corresponding packages, e.g., the TSSOP package is available in both 14-pin and 20-pin format. The TVSOP package, which has a lead pitch of 0.4 mm (16 mil) and a device height of 1.2 mm, is also available in the AHC family. Continued advancements in packaging are making more functionality possible with smaller space requirements.

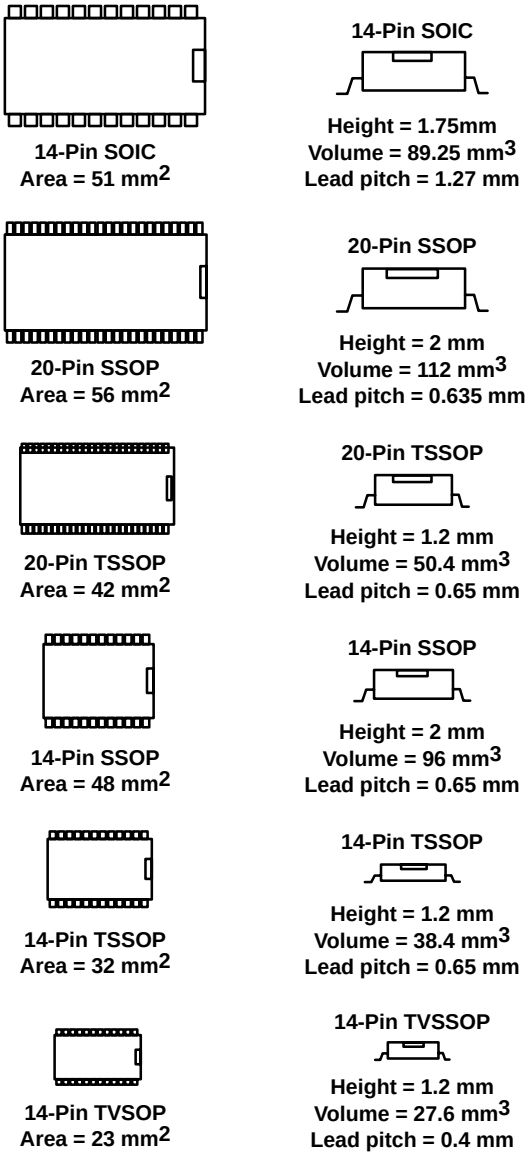

Figure 18. AHC Packages

Figure 19 shows a typical pinout structure for the 20-pin SSOP for the SN74AHC245. This provides for simultaneous switching improvements (see the *Signal Integrity* section of this application report).

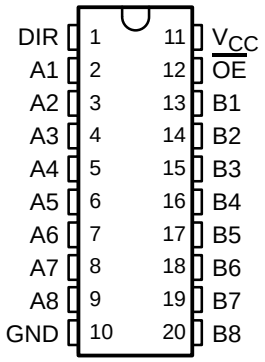

Figure 19. SN74AHC245 Pinout

For a comprehensive listing and explanation of TI's packaging options, consult the *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001C.

Microgate Logic

The Microgate Logic device is a single gate that is used instead of the two-, four-, or six-gate versions. The advantages of Microgate Logic are:

- Simplified circuit routing
- Help in ASIC modification
- 3.5-ns typical propagation delay

Microgate Logic is available in CMOS (AHC) and TTL (AHCT) versions. The AHC versions are compatible with Toshiba's TC7SHxx series. Figure 20 shows the pinout of the SN74AHC1G00.

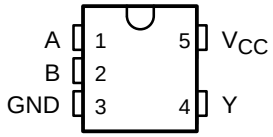

Figure 20. 5-Pin Microgate Logic Pinout

Acknowledgment

The author of this application report is Shankar Balasubramaniam.