Application Report
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SNx5DP159 Schematic Checklist

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ABSTRACT

This schematic checklist provides a brief explanation of each SNx5DP159 device pin for both packages (RSB and RGZ), and the recommended configuration of SNx5DP159 device pins for default operation. The SN65DP159 and SN75DP159 are pin-to-pin compatible, so this checklist applies to both devices. The SNx5DP159 device is an AC-Coupled HDMI signal to transition-minimized differential signal (TMDS) retimer supporting digital video interface (DVI) 1.0 and high-definition multimedia interface (HDMI) 1.4 b and 2.0 output signals. The SNx5DP159 supports four TMDS channels and Digital Display Control (DDC) interfaces. The SNx5DP159 has the ability to be configured through pin strap or I2C. Use this information to check the connectivity for each SNx5DP159 device on a system schematic.

This document is intended to aid design at the system level for general applications, but must not be the only resource used. In addition to this list, use the information in the *SNx5DP159 6-Gbps AC-Coupled TMDS™ to HDMI™ Level Shifter Retimer*, *DP159RSB Evaluation Module*, *DP159RGZ Evaluation Module*, and associated documents to gain a full understanding of device functionality.

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1 SNx5DP159RSB/RGZ Schematic Checklist

PIN NAME	PIN NUMBER (RSB)	PIN NUMBER (RGZ)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATION
Main Link Input Pins					
IN_D[0:2]p/n	1, 2, 4, 5, 6, 7	2, 3, 5, 6, 8, 9	Main link differential input		100 nF AC coupled from sink connector or GPU to SNx5DP159
IN_CLKp/n	9, 10	11, 12	Main link clock differential input	100 nF AC coupled from sink connector/GPU to SNx5DP159	
Main Link Output Pins					
OUT_D[0:2]p/n	24, 25, 26, 27, 29, 30	28, 29, 31, 32, 34, 35	TMDS data differential output	Direct connection from SNx5DP159 to source connector/sink	
OUT_CLKp/n	21, 22	25, 26	TMDS clock differential output	Direct connection from SNx5DP159 to source connector/sink	
AUX_SRCp/n	N/A	44, 45	Source side bidirectional DisplayPort auxiliary for I2C-over-AUX	100 nF AC coupled from sink connector/GPU to SNx5DP159	
Configuration and Miscellaneous Pins					
SDA_SRC	39	47	Source side TMDS bidirectional DDC data line	Snoop mode, tie it to GND.	
SCL_SRC	38	46	Source side TMDS bidirectional DDC clock line	Snoop mode, tie it to GND	
SDA_SNK	33	39	Sink side TMDS bidirectional DDC data line	SDA/SCL from the source is connected directly to the SDA/SCL sink. The SNx5DP159 needs its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Sink application: 47 k pullups to 5 V Source application: 2 k pullups to 5 V	Consider adding an external I2C buffer for DDC capacitance isolation.
SCL_SNK	32	38	Sink side TMDS bidirectional DDC clock line	SDA/SCL from the source is connected directly to the SDA/SCL sink. The SNx5DP159 needs its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Sink application: 47 k pullups to 5 V Source application: 2 k pullups to 5 V	Consider adding an external I2C buffer for DDC capacitance isolation.
HOT PLUG DETECT PINS					
HPD_SNK	28	33	Hot plug detect input from sink side	Connect to HPD output of the display or source connector. For snoop mode: Connect directly to GPU of the sink (check GPU supported voltage) directly connected HPD line HPD_SNK has internal 190 k pulldown. Consider adding an external switch to isolate potential leakage voltage from sink HPD when the sink is off.	Consider adding an external switch to isolate potential leakage voltage from sink HPD when sink is off.

PIN NAME	PIN NUMBER (RSB)	PIN NUMBER (RGZ)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATION
HPD_SRC	3	4	Hot plug detect output to source side	If HPD_SRC goes to the source connector, a level shifter from 3.3 V to 5 V is needed. If HPD_SRC goes to GPU, check the supported GPU voltages. If HPD snoop mode is implemented, leave HPD_SRC floating	
CONTROL PINS					
OE	36	42	Enable/reset pin	Start with 0.2 µF, tune depending on the RC time constant delay (Tr) requirement in regard to power ramp up time	See Table 1 for different timing values based on capacitance.
V_{sadj}	18	22	TMDS-compliant voltage swing control resistor	Start with 6.49 k resistor to ground resistor value, tuning depends on compliance result	
SCL_CTL	13	15	I2C clock signal	For pin strap mode, 1 k pulldown	2 k pullups to 3.3 V or value required by I2C master in I2C mode 10 k pullups to 3.3 V if unused
SDA_CTL	14	16	I2C data signal	For pin strap mode, 1 k pulldown	2 k pullups to 3.3 V or value required by I2C master in I2C mode. 10 k pullups to 3.3 V if unused
I2C_EN	8	10	I2C control mode	65 k (± 10%) pulldown resistor to GND for pin strap mode 0 - 65 k (± 10%) pullup resistor to 3.3 V for I2C mode	
EQ_SEL/A0	17	21	I2C address bit 0 or receiver equalization control	For pin strap mode, 65 k (± 10%) pullup to 3.3V, 0 - 65 k (± 10%) pulldown to GND, or NC SLEW = L: Fixed EQ at 7.5 dB SLEW = NC: Adaptive EQ SLEW = H: Fixed at 14 dB	Set address bit 0 in I2C mode
HDMI_SEL#/ A1	23	27	I2C address bit 1 or DVI/HDMI control	For pin strap mode, 65 k (± 10%) pullup resistor to 3.3 V to configure device for DVI 0 - 65 k (± 10%) pulldown resistor to GND configure device for HDMI	Set address bit 1 in I2C mode
SLEW_CTL	34	40	Transmitter slew control	For pin strap mode, 65 k (± 10%) pullup to 3.3 V, 0 - 65 k (± 10%) pulldown to GND, or NC SLEW = L: 5 ps, slow SLEW = NC 10ps, slowest SLEW = H: fastest data rate	Leave it floating when I2C_EN/PIN = high, control through I2C
TX_TERM_C TL	N/A	36	Transmitter termination control	For pin strap mode, 65 k (± 10%) pullup to 3.3 V, 0 - 65 k (± 10%) pulldown to GND, or NC TERM = L, 75 Ω–150 Ω (HDMI2.0) TERM = NC, automatically selects the termination impdeance TERM = H, No transmit termination	If the TMDS_CLOCK_RATIO_STATUS bit = 1, the SNx5DP159 automatically switches to approximately 75 Ω–150 Ω termination.
PRE_SEL	16	20	De-emphasis control	For pin strap mode, 65 k (± 10%) pullup to 3.3 V, 0 - 65 k (± 10%) pulldown to GND, or NC TERM = L, 2 dB de-emphasis TERM = NC, 0 dB de-emphasis TERM = H, Reserved	
CEC_EN	N/A	18	CEC control pin for Dongle applications	This pin is either NC or can be routed to control a CEC enable FET	
NC	N/A	17	No connect	Leave unconnected	

PIN NAME	PIN NUMBER (RSB)	PIN NUMBER (RGZ)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATION
SWAP/POL	N/A	1	Input lane SWAP and polarity control pin when I2C_EN/PIN = Low	For pin strap mode, 65 k (± 10%) pullup to 3.3 V, 0 - 65 k (± 10%) pulldown to GND, or NC SWAP/POL = L, receive lanes swap (retimer and redriver mode) TERM = NC, normal working TERM = H, receive lane polarity swap (retimer mode only)	
POWER PINS					
VCC	11, 37	13, 43	3.3-V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
VDD	12, 19, 20, 31, 40	14, 23, 24, 37, 48	1.1-V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
GND	15, 35	7, 19, 30, 41	Ground	Connect to board ground	
Thermal Pad	41	49	Ground	Connect to board ground	

Table 1. Enable (OE) Pin Timing Based on Capacitance

RISE TIME (T_r) (ms)	CAPACITOR VALUE (µF)
25	0.1
50	0.2
100	0.4
200	0.8
500	2

2 References

- *SNx5DP159 6-Gbps AC-Coupled TMDS™ to HDMI™ Level Shifter Retimer Datasheet*
- *DP159RSBEVM User's Guide*
- *DP159RGZEVM User's Guide*

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