Using SN65HVD96 to Create a Power-Over-Data and Polarity Immunity Solution

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ABSTRACT

The 2-wire bus communication system is widely deployed in many industries; the buses provide most of the required polarity identification. Every node is powered by the local power source or battery. This paper presents a system solution to resolve 2-wire bus polarity immunity, and a power-over-data-lines feature is supported simultaneously. In the solution, only a 2-wire bus is used while the power supply of some remote nodes is also delivered through the 2-wire bus. Furthermore, it is a fully automatic, polarity immunity communication system—after power up, negotiation between multinodes to switch A and B lines is never needed. The key effort of this solution is how to properly decode the signal as AC coupling is applied due to power delivery over the 2-wire data bus. Also, some technical tips regarding the system are included for the user's consideration.

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1 Introduction

A 2-wire bus is widely used in many fields; it includes many industry standard types such like RS-232, half-duplex RS-422/485, CAN, and so forth. Figure 1 shows a typical 2-wire bus topology. But for almost all of these 2-wire buses, the polarity of the bus lines must be identified (in other words, A or B, high or low).

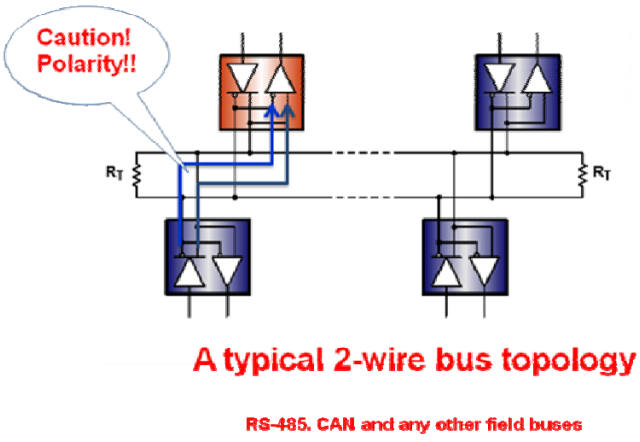


Figure 1. Typical 2-Wire Bus

The transceiver cannot work well if the bus lines are inversely connected. From the real field feedback, an operator often makes an incorrect connection when faced with a 2-wire bus in the real fields, even though the lines have different colors or another obvious sign. However, if the property of the transceiver or solution-self is polarity immunity, the operator would not

need to be concerned about line A or line B. It means data transmission can be achieved well even if 2-wire bus lines are inversed.

This paper focuses on the polarity immunity transceiver among TI industry interface products and discusses the method to achieve polarity immunity function. Meanwhile, it is better to get the power supply from the 2-wire bus, because then the node does not need local supply (which may cause trouble in some existing buildings). Also, delivering the power by the 2-wire bus facilitates easy installation and flexibility of specific applications like tower control or stage control. Doing this means the user only needs to connect the handset controller to the bus by inserting 2-wire without polarity identification, and then it works well with the power supplied from the 2-wire bus. To achieve polarity immunity and power over data, some critical challenges exist. These are discussed step by step.

2 Polarity Immune Transceiver SN65HVD96

When examining RS-485 and CAN bus connection, it is clear that line A or B, and CANH or CANL are described separately; this is subjected to the traditionally standard definition. But when a polarity immunity transceiver is considered, the easiest approach is to design a receiver that translates only the absolute differential voltage, but does not take its sign—positive or negative. TI SN65HVD96 is just such a device (Figure 2 shows the internal block of SN65HVD96, a half-duplex transceiver.

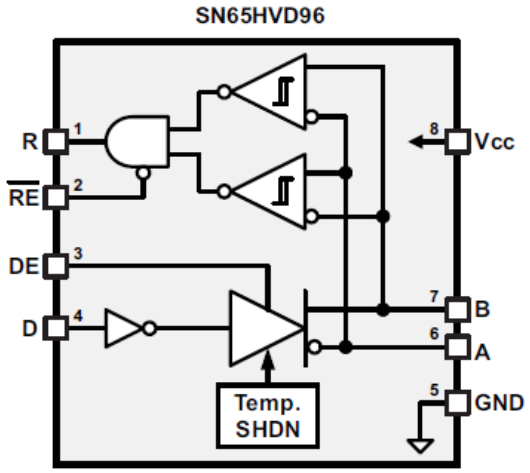


Figure 1. SN65HVD96 Internal Block

The core function of HVD96 is the logic portion includes two window comparator with crossed A and B line connected to both inverted and noninverted input terminals, respectively. Then both output signals go through AND gate logic portion to get the final output data. The final output of the logic portion always takes the absolute differential input voltage value but neglects its sign. The data output from terminal R is high if the differential voltage is between –0.5 and +0.5 V; it means data bit 1 receives the data, and will be 0 if the differential voltage is positively or negatively larger than 0.9 V. The other two spare regions –0.9 to –0.5 V and 0.5 to 0.9 V are the indeterminate area. Figure 3 explains the Sympol status. Figure 4 is the bus and logic relational chart.

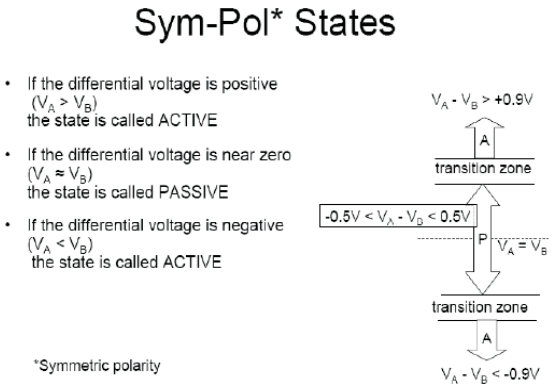


Figure 3 Sympol States

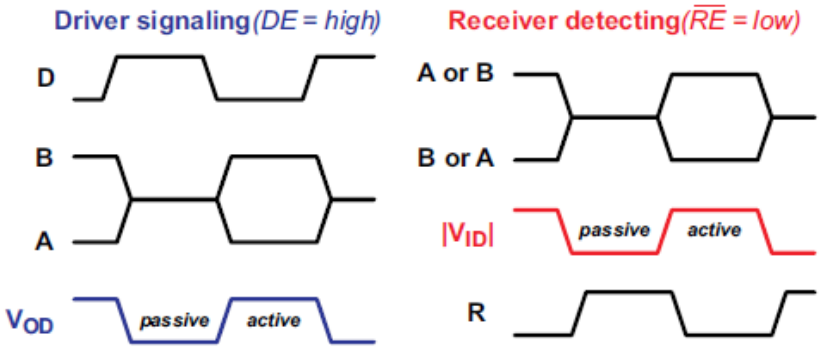


Figure 4. Passive and Active Status

For the signal of HVD96 transmitted, both A and B lines are brought to middle-level voltage at V_{cc} /2 by shutting off the up and down transistors when the logic 1 is sent. This status can be called passive mode. When logic 0 is transmitting, the up and down transistor is turned on, thus line B is pull to V_{cc} voltage while line A is pulled to GND with the load presented line bus. This status can be called active mode. It is similar to a CAN transceiver, but the difference is the receiver only takes the absolute differential voltage. Additionally, the SN65HVD96 has the same package and pin assignment as the popular RS-485 chips. So the benefit of this part is that a user can do a drop-in replacement but have the polarity immunity feature for the existing RS-485 application. However, the SN65HVD96 cannot use it to work together with the standard RS-485 part in one network because the SN65HVD96 electrical characteristics are not compatible with RS-485 transceivers.

3 Power-Over-Data Lines

3.1 Basic Architecture Discussion

As previously discussed, sometimes when power is also delivered through the 2-wire data bus, different methods are used to deliver the power. For example, when data transmission and power delivery are time-multiplexed in the same 2-wire, there is no conflict between power rail and AC signals. But such a solution needs more detailed software and hardware considerations, and also has many limitations. The best way is to deliver power and data together through the 2-wire bus simultaneously, but data and power must not affect each other. To address this requirement, it is necessary to block data and power from each other on the same bus when they are present at the same time. First, consider how a DC power rail will not affect a data signal. Because an active data signal is an AC signal but power is a DC signal, obviously the capacitor can be used to block the power and the inductor can be used to block the AC signal. One line can work as the V_{cc}, the other as GND, and SN65HVD96 transmitting data should be

connected with the 2-wire bus by AC coupling (the same AC coupling for SN65HVD96 as the receiver). Fortunately, SN65HVD96 can support common mode input voltage –7 to +12 V. Figure 5 shows and overall picture of power-over-data lines.

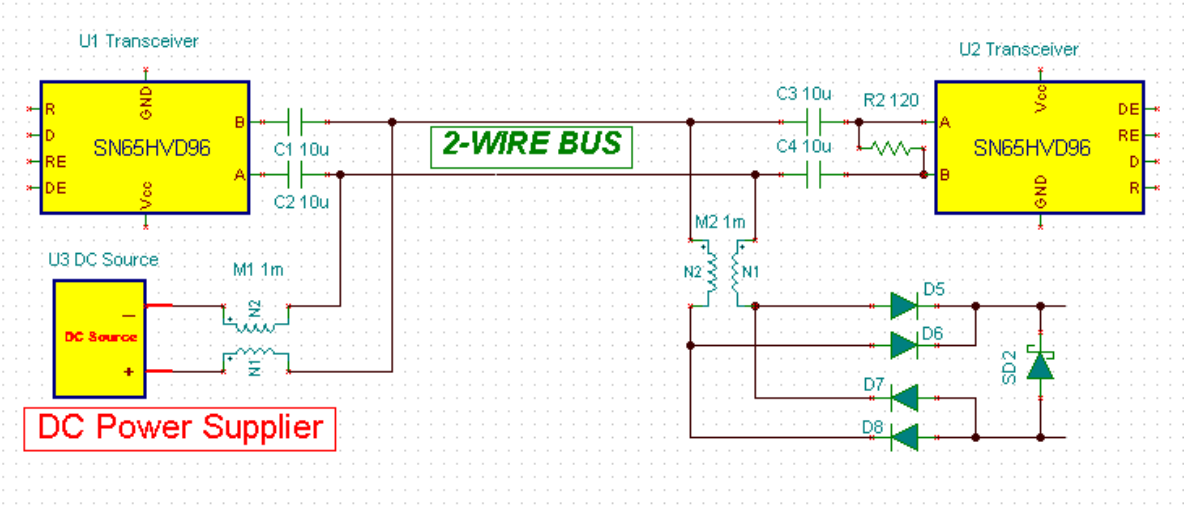


Figure 5. Power-Over-Data Lines

3.2 Considerations

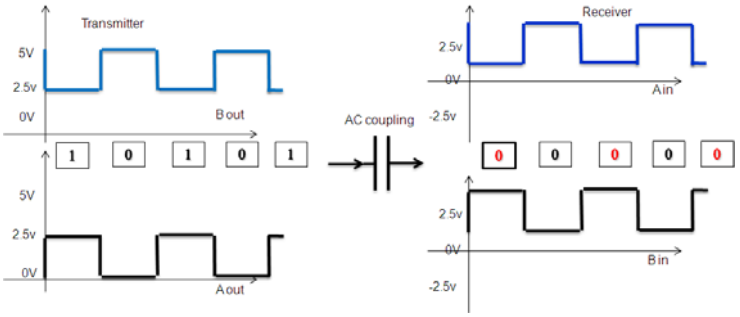
In the circuits in Figure 5, the right unit is the main machine; it has a DC source to supply the power to the 2-wire bus, its power rail voltage can be 5 volt or more, and it depends on the load requirements and drop-down caused by the inductor and diodes.

The transceiver at the right side can be treated as the controller unit which must get power from the 2-wire bus and also transmit or receive the data from the 2-wire lines. A value capacitor close to its output and input terminals passes the AC signals but blocks the DC power rail voltage. Remember, the impedance of capacitor is 1/jωc. The capacitor value should be big enough to have smaller impedance to easily pass the AC signal as the bus speed can be low in some application. DC power source output impedance is very low and must not be directly connected to the bus; it will greatly attenuate the AC signals. To increase its output impedance for the AC signal, but still pass the DC power rails, the inductor should be inserted into the bus close the output of DC source. The inductor has the impedance jωL; once ω is fixed for the certain transmission speed, the inductance value L is required as large as possible to provide a very high impedance to the AC signals. The value of the inductor should be big enough (like tens mH level), and if necessary, continue using coupling inductor to increase inductance of each. Because the 2-wire line can be reversed, D5, D6, D7, and D8 are used as a bridge rectifier to get the correct power direction to the load all the time.

4 Polarity Immunity in AC Coupling

4.1 SN65HVD96 Bilevel Signal in AC-Coupling System

The previous section described the solution of the power delivery through the 2-wire bus. It its now time to address how the SN65HVD96 can fit into this design for data transmission. In general, AC coupling eliminates its original DC component. Figure 6 shows the actual signal status at the receiver side after the coupling capacitors. We assume the input data is a continuous square wave 0 1 0 1…but the receiver behind the capacitor will translate it into 0 0 0



RECEIVER	$\overline{RE}$	V_{ID}	R	
	H or OPEN	X	Z	Receiver Disabled
	L	$V_{ID} < -0.9$ V	L	Active Bit Received
		-0.9 V $< V_{ID} < -0.5$	?	Indeterminate bus
		-0.5 V $< V_{ID} < 0.5$ V	H	Passive Bit Received
		0.5 V $< V_{ID} <$ 0.9 V	?	Indeterminate bus
		0.9 V $< V_{ID}$	L	Active Bit Received
		Open, Short, Idle	H	Failsafe Condition

Figure 6. Bilevel Signals After AC Coupling

Figure 7. SN65HVD96 Function Table

0… according to Figure 7, the function table of SN65HVD96. The reason is that the capacitor removes the DC component in both A and B signals, the final signal input to the receiver is coupled to V_{CC} /2 DC level, and then the differential input voltage is either larger than 0.9 V or smaller than -0.9 V. More importantly, SN65HVD96 only takes the absolute differential value.

4.2 SN65HVD96 Solution for Trilevel Transmitter in AC-Coupling System

In Figure 6, the signal transmitted is a DC-balanced signal of a high-frequency square-wave and we can increase the capacitor value to lower the high-pass cut-off frequency. However, it is not possible to avoid the wrong decoding of SN65HVD96 working as a receiver, because SN65HVD96 only takes the absolute differentially voltage value, but is not concerned with the sign (positive or negative). So DC balance cannot provide any help here.

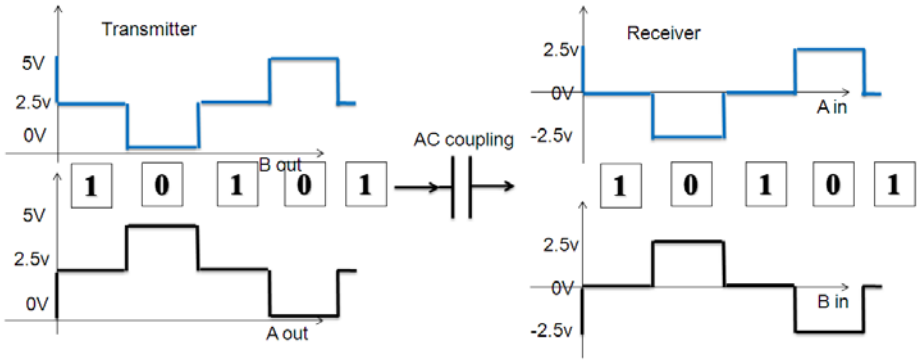


Figure 8. Trilevel Signals After AC Coupling

The threshold of the passive input status signal is defined as -0.5 to +0.5 V. The problem can be resolved by making both lines passive very close to each other and behind the coupling capacitor at the receiver input terminal. So if the transmitter can send the trilevel signal of Figure 8, then the problem is gone. The correct decoding is finished after AC coupling because the middle level of A and B are very close at zero volts. In Figure 8, the continuous square wave is still used to illustrate the status.

According to the function table of SN65HVD96, when the logic data is 0 at D terminal of SN65HVD96 and DE is high, the line B signal always drives to high voltage while the line A signal drives to low. To design a trilevel transmitter, a two-unit SN65HVD96 is used to work alternatively as the transmitter while cross-connecting their A and B terminals. Add one D-type flip-flop to alternatively select which SN65HVD96 is transmitting according to the input data rising edge changing. For a continuous square wave, this combined circuit can drive line A and line B to low or high, alternatively, every other logic data 0. This is achieved by the circuits of Figure 9; Figure 10 shows the actual test result in the lab.

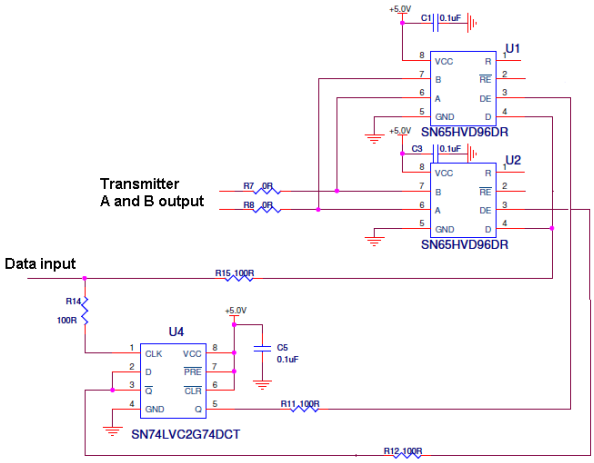


Figure 9. Circuit of Trilevel Transmitter

Transmitter test w/o dump resistor.

Green and Yellow trace are output of transmitter.

Blue trace is data transmitted.

Pink trace is one output of Flip Flop.

Figure 10. Waveform of Trilevel Transmitter

During the lab test, it is discovered that the bus changes very slowly to the passive status (see the waveform in Figure 10). The reason is that the discharge is too slow because there is no load between the lines. The driver outputs have two defined states, ACTIVE and PASSIVE. In the ACTIVE state the bus lines are pulled to +5V and GND. In the PASSIVE state, the driver outputs are disabled (high impedance) and both lines are at middle level of Vcc. In the PASSIVE state, the bus termination (if existing) can quickly do the discharge and reduce the differential signal to zero. But if there is no termination, the voltage of the bus lines can take a

while longer time to decay to zero. This effect is seen in the decay curves in the oscilloscope plots of Figure 10. Remember, however, that it is also advantageous to lower EMI.

As for the receiver, one SN65HVD96 is sufficient to correctly decode the differential signals from the 2-wire bus.

4.3 Exception and Considerations

We know that DC-balanced waveforms are useful in communications systems, because they can be used on AC-coupled electrical connections to avoid voltage imbalance problems between connected systems or components. To be specific, bit errors can occur when a (relatively) long series of 1s create a DC level that charges the capacitor of the high-pass filter used as the AC coupler, thus incorrectly lowering the signal input to a 0-level. To avoid these kinds of bit errors, most line codes are designed to produce DC-balanced waveforms.

This exception also occurs in the trilevel transmitter solution. To fully consider that all the possible data pattern could be transmitted, it is necessary to check the extreme condtion in Figure 11. The data being transmittted is kept as 0 always or for a very long time. There is no rising edge in the data, so the flip-flop cannot be triggered in the trilevel transmitter solution, thus only one SN65HVD96 is working there and no trilevel sigal occurs. If so, the input signal to the receiver after the AC coupling capacitor goes to zero volts. The received data output is 1 because the absolute $|V_{od}|$ will be near zero.

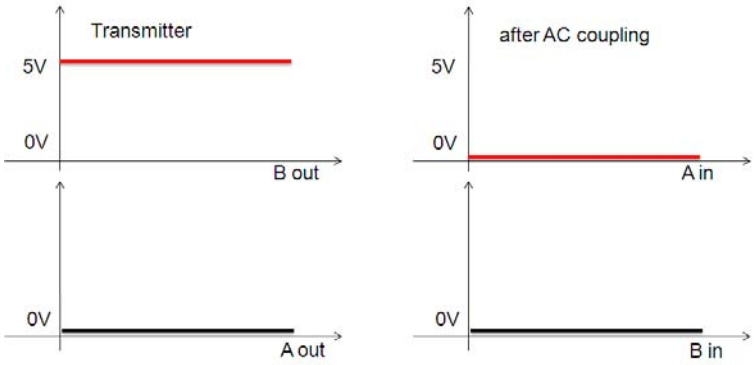


Figure 11. Exception Case

Sofware coding is the most feasible way to resolve this problem. When the data is being transmitted, the MCU inserts 1 after each bit to be trasmitted, then the data stream to the transmitter of the trilevel generator will never present the status of Figure 11.

Finally, with the total solution now determined, note that the circuit shown in Figure 12 is strongly recommnded when building your boards. The external serial resistor can help with the current limitation, the signal voltage reduction of over- and undershot, and so forth.

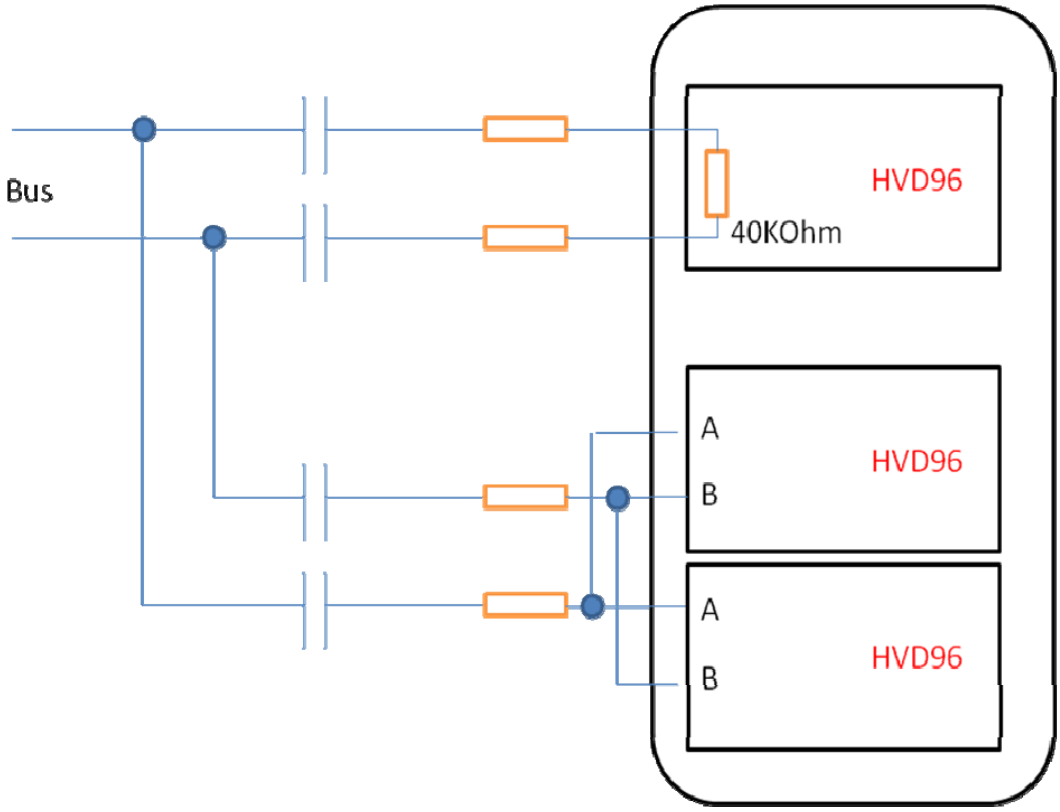


Figure 12. Recommended External Components

5 Conclusion

The preceding step-by-step discussion has addressed the solution to support power-over-data lines and polarity immunity together. This solution is examined in the real test; it can significantly enhance the flexibility of operation during deployment in the field. For the further requirements such as isolation, TI has a broad isolation portfolio ISO7xxx series for you selection.

6 References

- Kugelstadt Thomas, Training – SYMBOL, TI ESP database
- SLLSE35B – SN65HVD96 data sheet, WWW.TI.COM

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