How to Use a 3.3-V LVDS Buffer as a Low-Voltage LVDS Driver

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TEXAS INSTRUMENTS

This document discusses how to use a 3.3-V LVDS buffer as an LVDS driver that supports 1.8-V (or other low-voltage) LVTTL/LVCMOS input signals.

Introduction

An LVDS driver, such as the DS90LV011A or SN65LVDS1, accepts a single-ended LVTTL/LVCMOS input and translates it to a differential LVDS output, as shown in Figure 1. An LVDS buffer like the DS90LV001 or SN65LVDS100, on the other hand, accepts a differential LVDS input and outputs a differential LVDS signal, as shown in Figure 2.
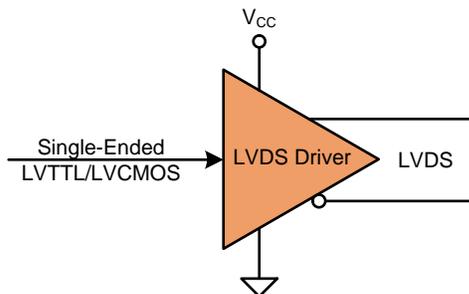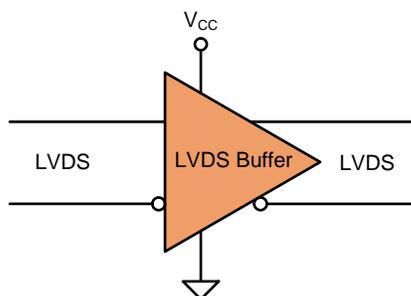

Figure 1. LVDS Driver

Figure 2. LVDS Buffer

Most LVDS drivers available on the market have a 3.3-V supply and only support 3.3-V LVTTL/LVCMOS signals. Sometimes the LVTTL/LVCMOS signals that need to be converted to LVDS are originating from devices that are powered by low voltages (such as 1.2 V, 1.8 V. 2.5 V, and so forth). Therefore, these signal normally have low-voltage swings ($V_{OH} - V_{OL}$) that follow the supply voltage (see Figure 3). In this case, the LVDS driver must support input single-ended signals with low-voltage swings. The approach described in this document achieves this using a 3.3-V LVDS buffer.

On the receiving side, a low-voltage LVDS receiver may also be needed to interface with a device powered from a low voltage. The SN65LVDS4 is an LVDS receiver from TI that is able to output 1.8-V or 2.5-V LVTTL/LVCMOS signals, and can be used in this case.
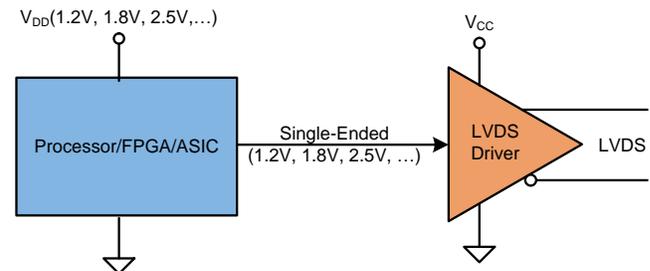

Figure 3. The Need for Low-Voltage LVDS Driver

Solution

Figure 4 shows the approach to solve this problem. An LVDS buffer, such as the DS90LV001 or SN65LVDS100, which is powered from 3.3-V supply, is used. The inverting input of the LVDS buffer is biased at a reference voltage (V_{REF}) that is appropriate for the input single-ended logic signal. This means that V_{REF} is set to be in the middle of the range between V_{OH}(min) and V_{OL}(max) of the input logic signal. A simple way to provide this reference voltage is to use a resistor divider with the 2 resistors (R1 and R2 in Figure 4) selected to generate the desired reference voltage. R1 and R2 should be large (kΩ range) to limit the quiescent current consumption.
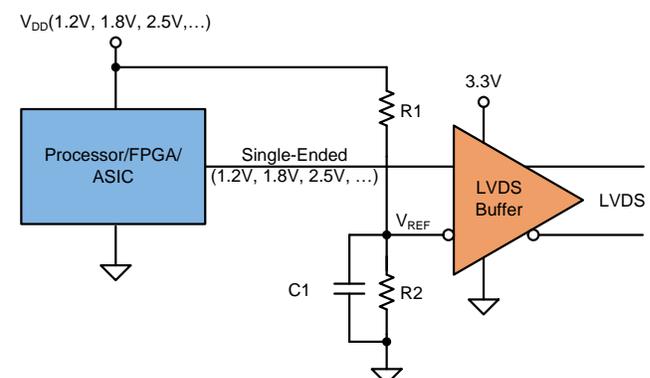

Figure 4. LVDS Buffer Used as a Low-Voltage LVDS Driver

The input single-ended LVCMOS/LVTTL signal is applied to the noninverting input of the LVDS buffer. When the input signal is logic high (specifically, when it is greater than V_{REF} by the amount of the threshold voltage of the LVDS buffer, which is usually 100 mV), the differential output of the LVDS buffer will be +350 mV. When the input signal is logic low (less than V_{REF} by the amount of the threshold voltage), the LVDS differential output will be –350 mV.

As an example, if the single-ended input is a 1.8-V signal, with $V_{OH}(min)$ = 1.17 V, and $V_{OL}(max)$ = 0.63 V, the reference voltage at the inverting input should be set to a voltage equal to $(V_{OH}(min) + V_{OL}(max))/2$, which is equal to 0.9 V. Suggested resistor values in this case are R1 = R2 = 10 kΩ.

Notice that the resistor divider is powered from the voltage supply of the source of the single-ended signal. This helps minimize duty cycle distortion. TI also recommends to add a capacitor (C1 = 0.01 μF) in parallel with R2 for stability.

The supported input voltage is, generally, any voltage in the input common-mode voltage range of the LVDS buffer. Most LVDS buffers support a wide input common-mode range (for example, 0 V to 4 V for the SN65LVDS100), therefore input voltage swings as low as 0.8 V (or even lower) can be supported with this approach.

Solution Cost

The cost of an LVDS buffer is generally comparable to the cost of an LVDS driver. There is additional cost for the two resistors and capacitor that are necessary for this solution, which is generally small. The additional PCB area necessary for this solution is also small, but it is dependent on the size of the chosen resistors and capacitor.

Limitations

Some of the limitations for this approach are:

- A buffer with integrated 100-Ω termination resistor cannot be used, because the termination resistor will alter the reference voltage on the inverting input and make it dependent on the input signal applied to the noninverting input.
- The data rate supported with this approach is only limited by the data rate supported by the LVDS buffer (like 800 Mbps for the DS90LV001 or 2 Gbps for the SN65LVDS100, for example).
- There is a small increase in the quiescent current consumption due to the current flowing through the voltage divider. The amount of this current depends on the values of the resistors R1 and R2 and it can be minimized by using large values for R1 and R2.

Conclusion

The approach described in this document provides a practical and inexpensive way to support the conversion of low-voltage LVTTL/LVCMOS signals to LVDS. It uses a 3.3-V LVDS buffer with a few passive components as an LVDS driver that supports input logic signals with voltage swings as low as 0.8 V.

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