- **Members of the Texas Instruments**
  Widebus™ **Family**

- **State-of-the-Art** *EPIC*-II*B*™ **BiCMOS Design**
  Significantly Reduces Power Dissipation

- **Typical V$_{OLP}$ (Output Ground Bounce) < 1 V**
  at V$_{CC}$ = 5 V, T$_A$ = 25°C

- **High-Impedance State During Power Up**
  and Power Down

- **Distributed V$_{CC}$ and GND Pin Configuration**
  Minimizes High-Speed Switching Noise

- **Flow-Through Architecture Optimizes PCB**
  Layout

- **High-Drive Outputs (–32-mA I$_{OH}$, 64-mA I$_{OL}$)**

- **Bus Hold on Data Inputs Eliminates the**
  Need for External Pullup/Pulldown
  Resistors

- **Latch-Up Performance Exceeds 500 mA Per**
  JESD 17

- **Package Options Include Plastic Shrink**
  Small-Outline (DL), Thin Shrink
  Small-Outline (DGG), and Thin Very
  Small-Outline (DGV) Packages and 380-mil
  Fine-Pitch Ceramic Flat (WD) Package
  Using 25-mil Center-to-Center Spacings

SN54ABTH16245 . . . WD PACKAGE
SN74ABTH16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V$_{CC}$	7	42	V$_{CC}$
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V$_{CC}$	18	31	V$_{CC}$
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$
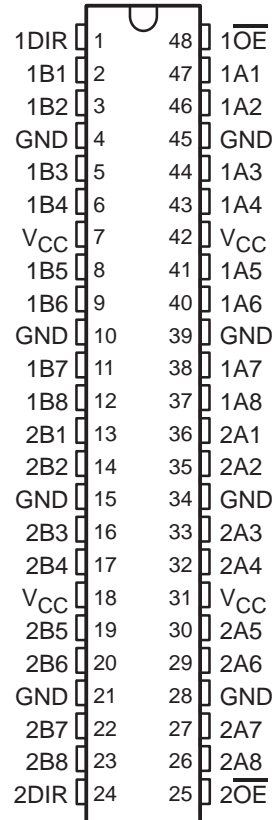
description

The 'ABTH16245 devices are 16-bit noninverting 3-state transceivers that provide synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the devices so that the buses are effectively isolated.

When V$_{CC}$ is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V$_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH16245 is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol[†]
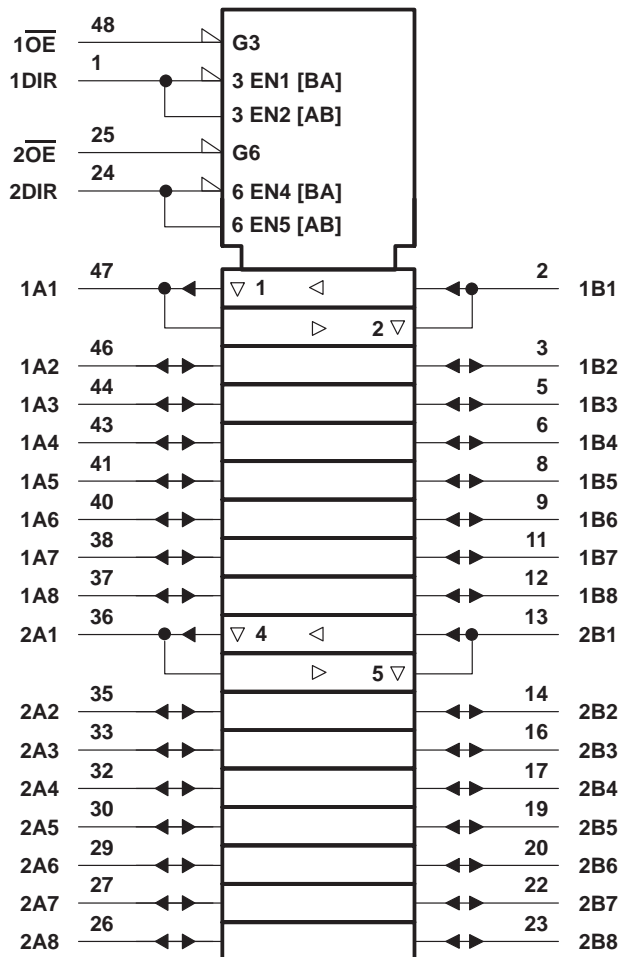
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels
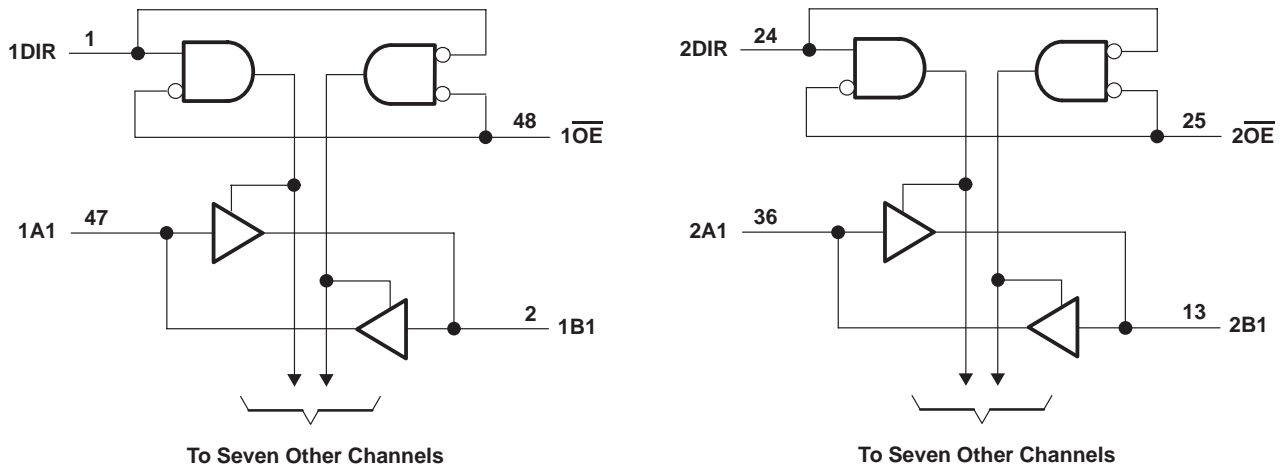
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABTH16245 .... 96 mA
SN74ABTH16245 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 89°C/W
DGV package .... 93°C/W
DL package .... 94°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54ABTH16245		SN74ABTH16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABTH16245, SN74ABTH16245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
SCBS662I – MARCH 1996 – REVISED MARCH 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABTH16245		SN74ABTH16245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
	A or B ports					±100		±100		±100	
$I_{I(hold)}$		$V_{CC} = 4.5$ V	$V_I = 0.8$ V	100			100		100		µA
			$V_I = 2$ V	−100			−100		−100		
I_{OZPU}		$V_{CC} = 0$ to 1.9 V	$V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$			±50**		±50**			µA
		$V_{CC} = 0$ to 2.1 V				±50				±50	
I_{OZPD}		$V_{CC} = 1.9$ V to 0	$V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$			±50**		±50**			µA
		$V_{CC} = 2.1$ V to 0				±50				±50	
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}		$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O‡		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	A or B ports	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}§		$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	Control inputs	$V_I = 2.5$ V or 0.5 V			3						pF
C_{io}	A or B ports	$V_O = 2.5$ V or 0.5 V			6						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
** On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
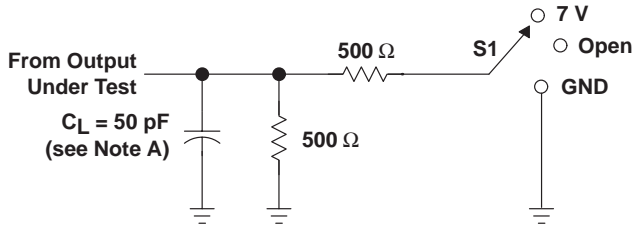
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C$_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH16245 V$_{CC}$ = 5 V, T$_A$ = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
t$_{PLH}$	A or B	B or A	1	2.2	3.6	0.5	4.1	ns
t$_{PHL}$			1	2.3	3.8	0.5	4.4	
t$_{PZH}$	$\overline{OE}$	B or A	1	3.6	5.2	0.8	6.4	ns
t$_{PZL}$			1	3.7	6.1	0.9	6.5	
t$_{PHZ}$	$\overline{OE}$	B or A	2	4.4	6.7	1.3	7.9	ns
t$_{PLZ}$			1.5	3.3	4.7	1.4	5.6	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C$_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABTH16245 V$_{CC}$ = 5 V, T$_A$ = 25°C					UNIT
			MIN	TYP	MAX	MIN	MAX	
t$_{PLH}$	A or B	B or A	1	2.2	3.4	1	3.9	ns
t$_{PHL}$			1	2.3	3.7	1	4.2	
t$_{PZH}$	$\overline{OE}$	B or A	1	3.6	5.2	1	6.3	ns
t$_{PZL}$			1	3.7	5.4	1	6.4	
t$_{PHZ}$	$\overline{OE}$	B or A	2	4.4	5.8	2	6.3	ns
t$_{PLZ}$			1.5	3.3	4.7	1.5	5.2	

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5

PARAMETER MEASUREMENT INFORMATION

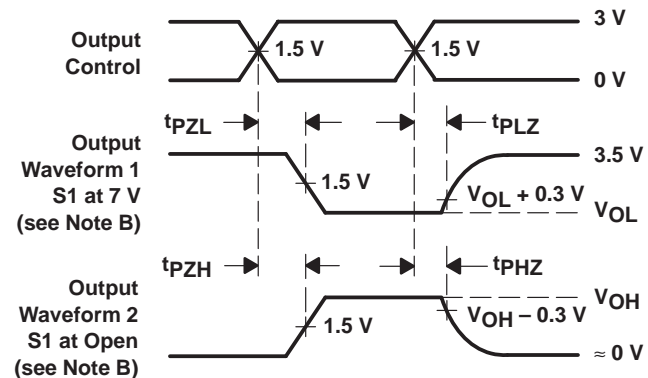| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION
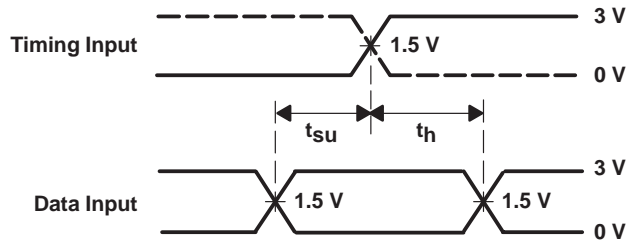
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
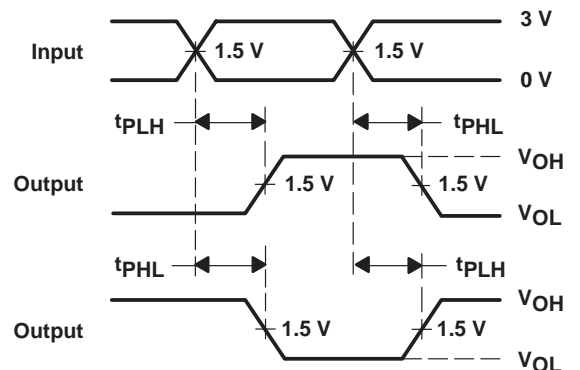
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABTH16245DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16245	Samples
SN74ABTH16245DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM245	Samples
SN74ABTH16245DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16245	Samples
SN74ABTH16245DLG4	ACTIVE	SSOP	DL	48	25	TBD	Call TI	Call TI	-40 to 85		Samples
SN74ABTH16245DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABTH16245DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ABTH16245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABTH16245DGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0
SN74ABTH16245DLR	SSOP	DL	48	1000	367.0	367.0	55.0

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABTH16245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

4040048−3/F   05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
                                    14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

8.3 / 7.9 TYP

PIN 1 ID AREA

A

1

46X 0.5

48

12.6 / 12.4 NOTE 3

2X 11.5

24

25

B

6.2 / 6.0

48X 0.27 / 0.17

⊕ 0.08 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

1.2 / 1.0

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° - 8°

0.75 / 0.50

0.15 / 0.05

DETAIL A
TYPICAL
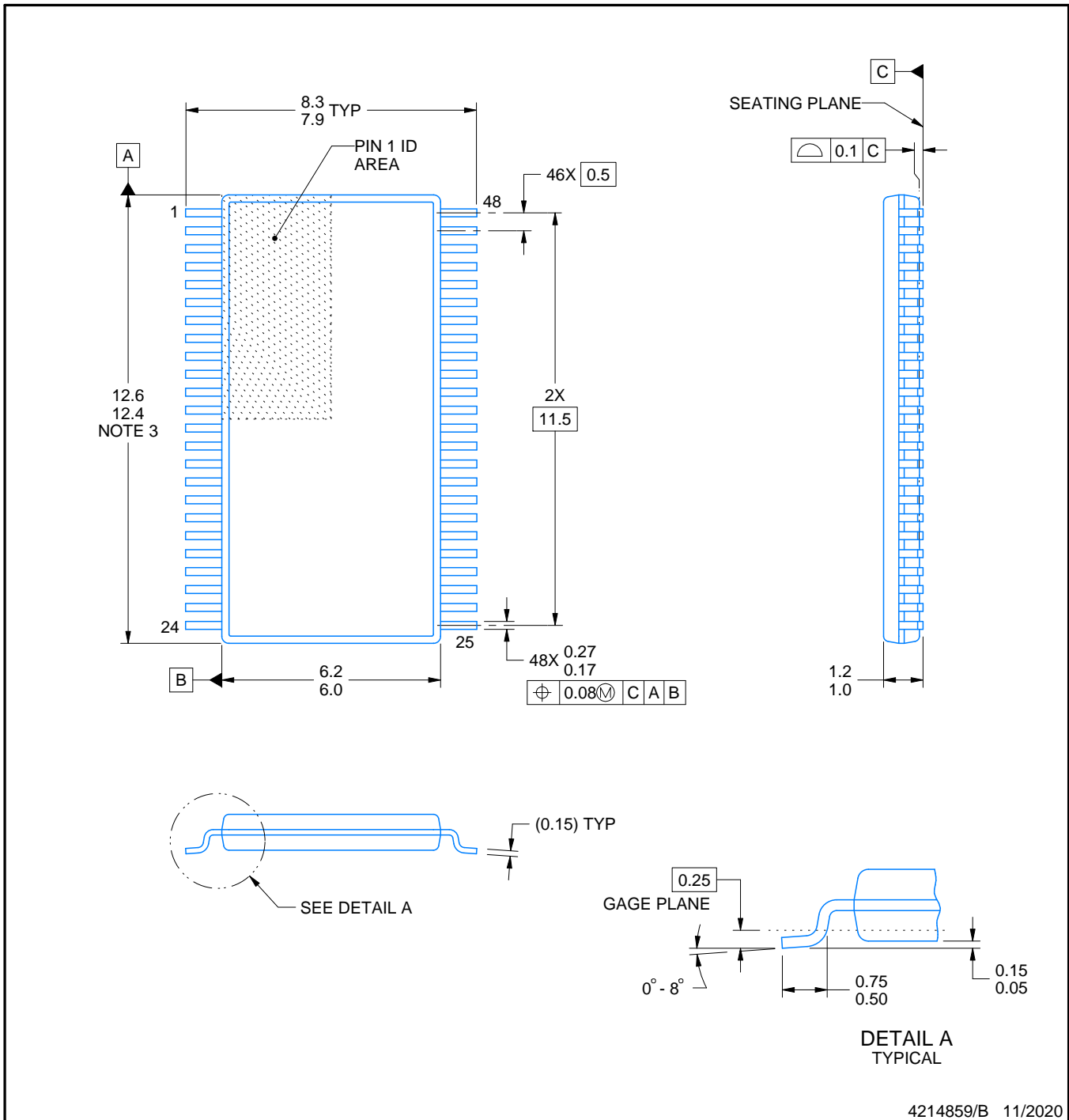
4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

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48X (1.5)

SYMM

1

48X (0.3)

48

46X (0.5)

(R0.05)
TYP

SYMM

24

25

(7.5)
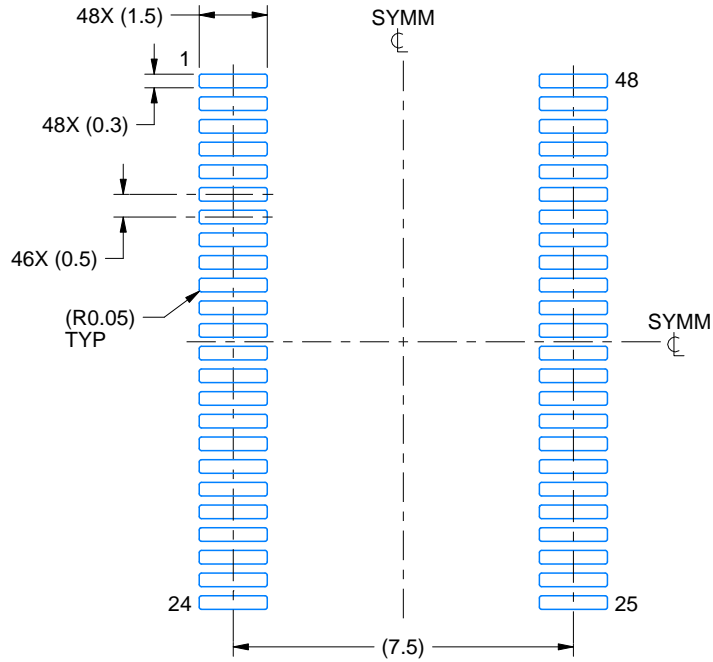
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214859/B   11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DGG0048A

48X (1.5)

1

SYMM

48

48X (0.3)

46X (0.5)

(R0.05) TYP

SYMM

24

25

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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