Advanced Schottky Family

SDAA010

TEXAS INSTRUMENTS

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INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high preformance state-of-the-art designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower that the 54S/74S series but had a much lower power consumption.

*Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product | efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table 1 provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

1. TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
2. Suppresses the effects of line ringing and significantly reduces undershoot
3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
4. Input current requirement reduced by up to 50%

Table 1. Typical Performance Characteristics by TTL Series

CIRCUIT TECHNOLOGY	MINIMIZING POWER					MINIMIZING DELAY TIME				
	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)
Gold Doped	TTL	10	10	100	35	TTL	10	10	100	35
	L TTL	33	1	33	3	H TTL	6	22	132	50
Schottky Clamped	LS TTL	9	2	18	45	S TTL	3	19	57	125
	'ALS	4	1.2	4.8	70	'AS	1.7	8	13.6	200

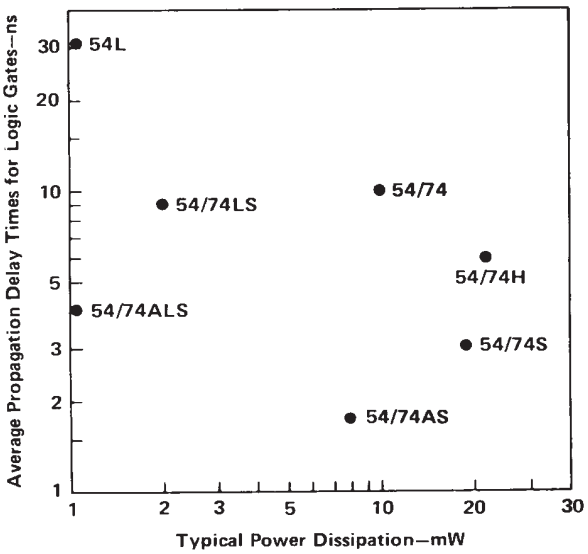


Figure 1. Speed-Power Relationships of Digital Integrated Circuits

5. Fanout is doubled
6. Terminated lines or controlled impedance circuit boards are normally not required.
7. The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
8. The maximum flip-flop frequency has been increased to 200 MHz.

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving effeciency at the lower speeds. The 'AS devices are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totem-pole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

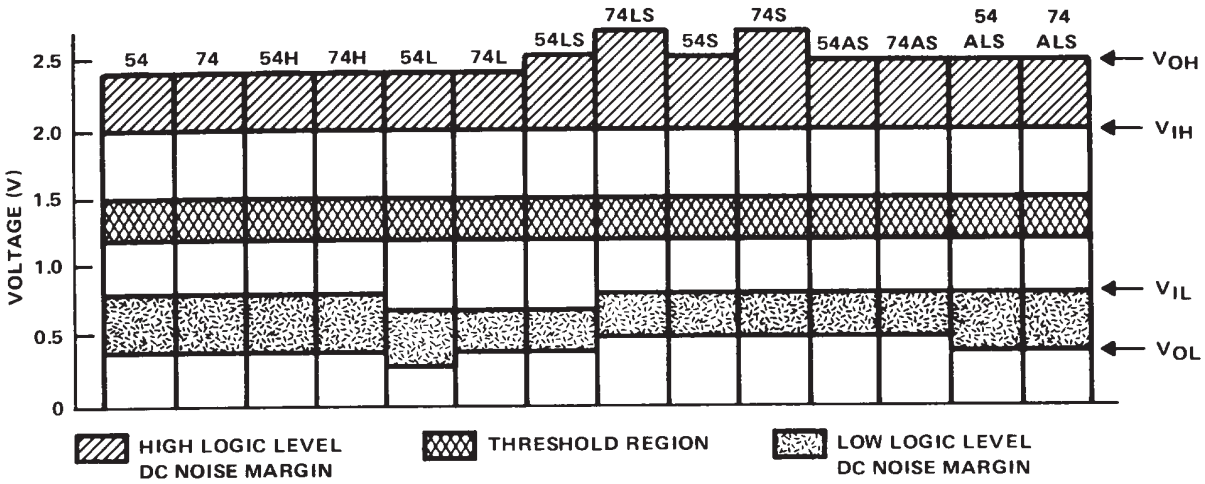


Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

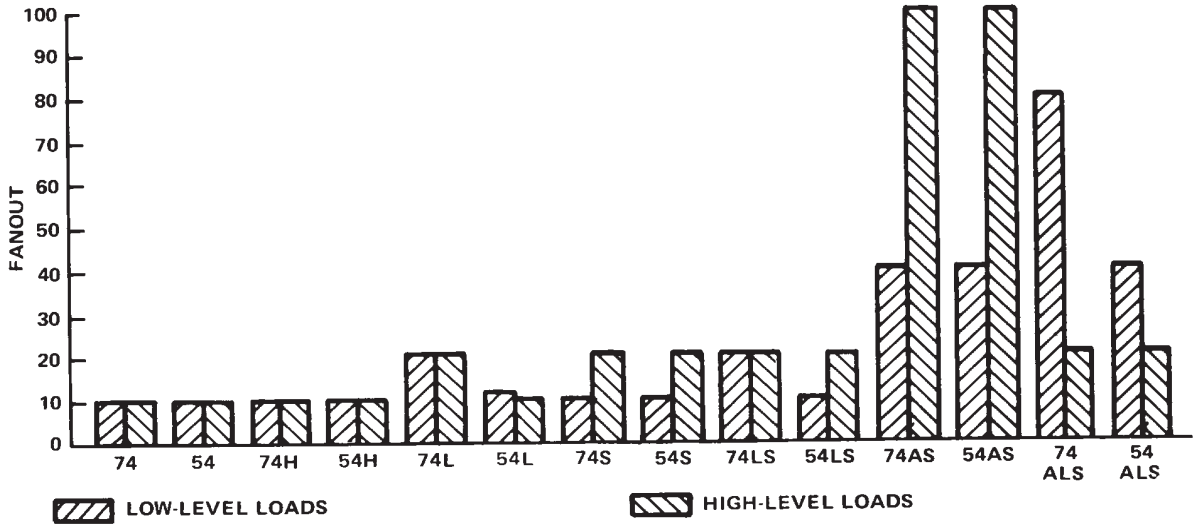


Figure 3. Fanout Capability

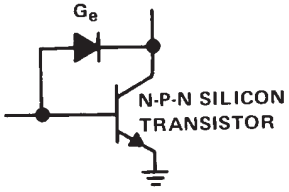


Figure 4. Baker Clamp

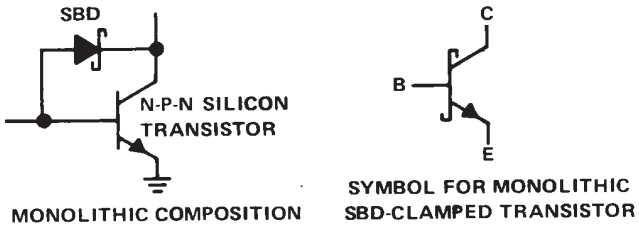


Figure 5. The Schottky-Clamped Transistor

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metal-semiconductor contact formed between a metal and a highly doped N semiconductor.

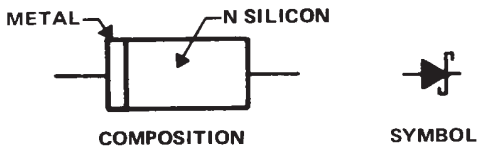


Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F.

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the current-voltage characteristics according the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

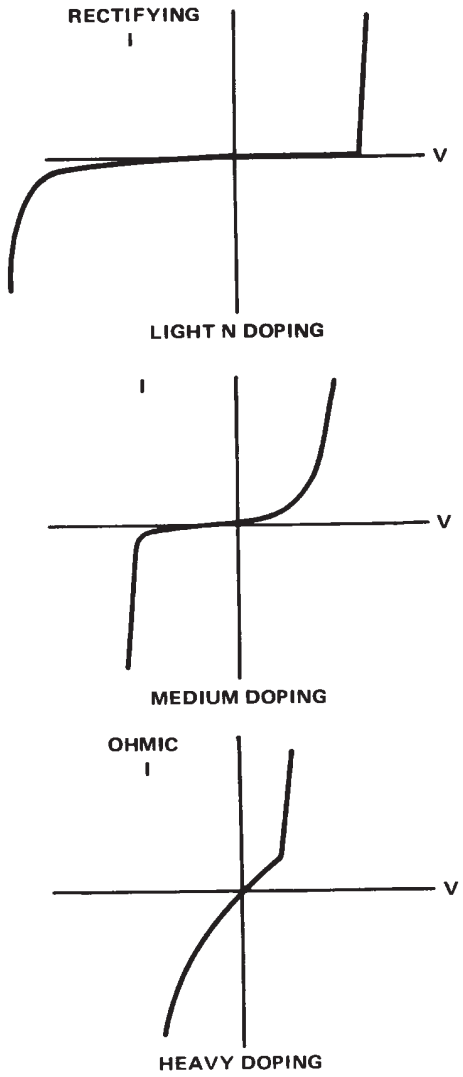


Figure 8. Metal-N Diode Current-Voltage Characteristics

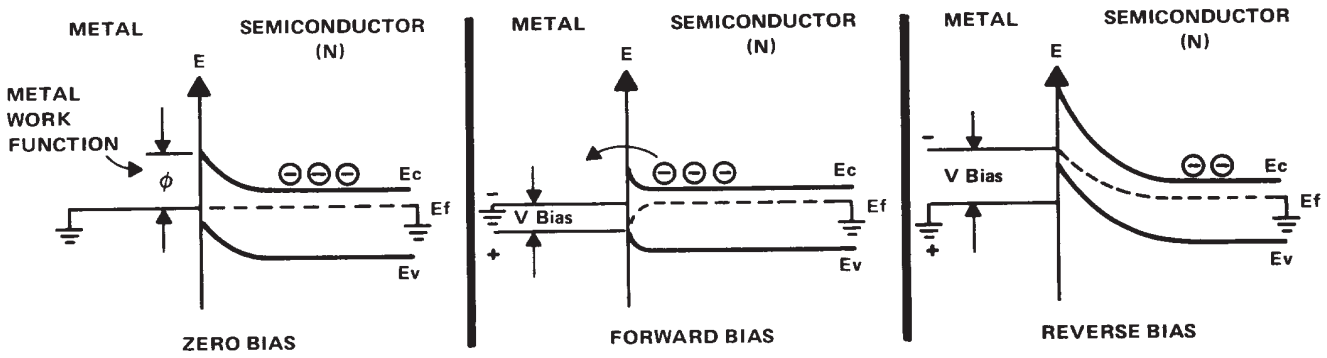


Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

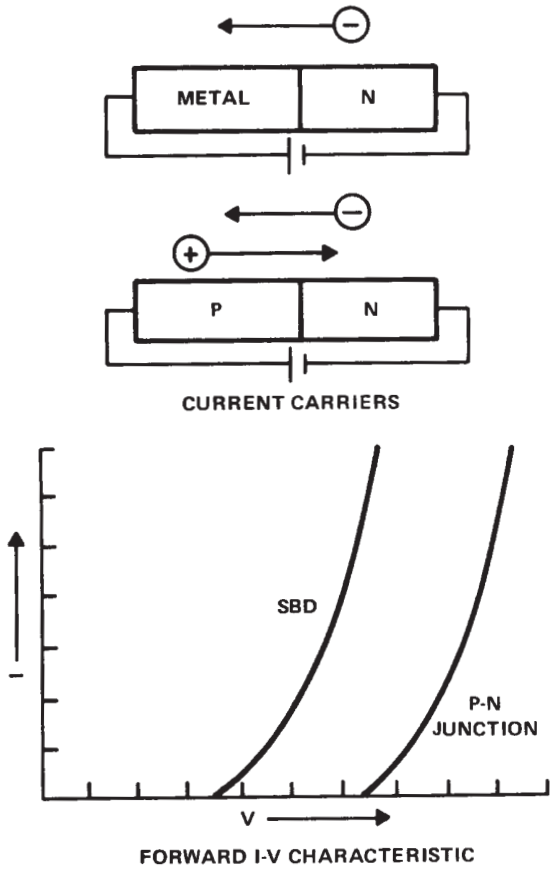


Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/'S process which consists of conventional masks, junction isolation, and a

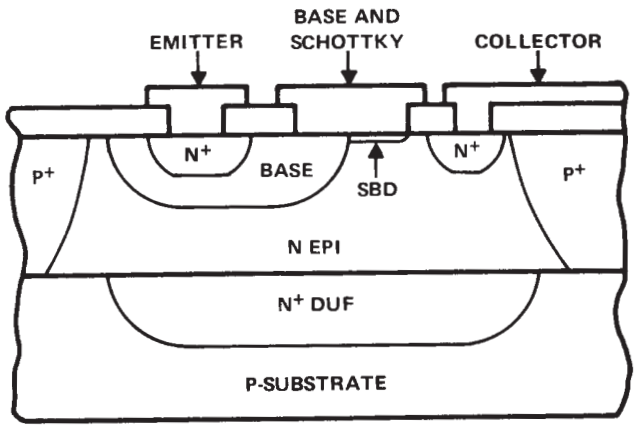


Figure 10. Standard Process ('LS/'S)

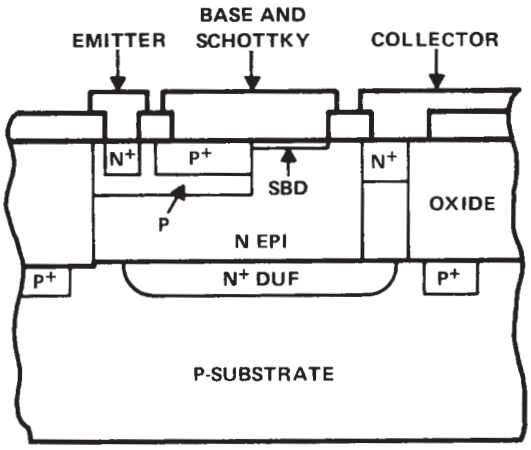


Figure 11. Advanced Process ('ALS/'AS)

standard metal system and Figure 11 illustrates the 'ALS/'AS process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

1. Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
2. Elimination of transistor storage time provides stable switching times across the temperature range.
3. An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

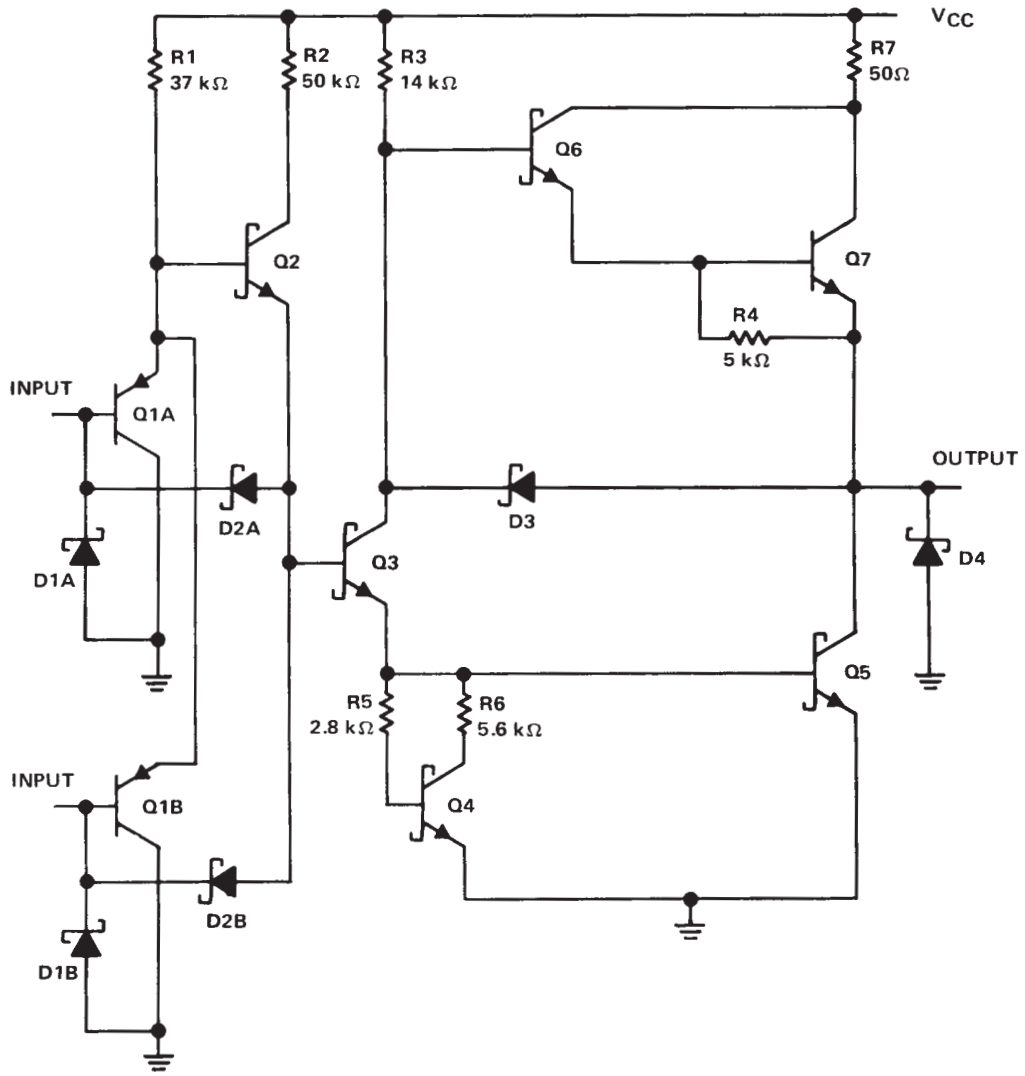


Figure 12. 'ALS00A NAND Gate Schematic

4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
5. The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
6. The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$VT = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5} - V_{BE} \text{ of Q1A (or } V_{BE} \text{ of Q1B)} \quad (1)$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = V_{CC} - V_{BE} \text{ of Q1A} - V_I/[R(h_{FE} \text{ of Q1A} + 1)] \quad (2)$$

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically $-10\ \mu A$ for the 'ALS00A and $-50\ \mu A$ for the 'AS00. High-level output voltage V_{OH} is determined primarily by V_{CC},

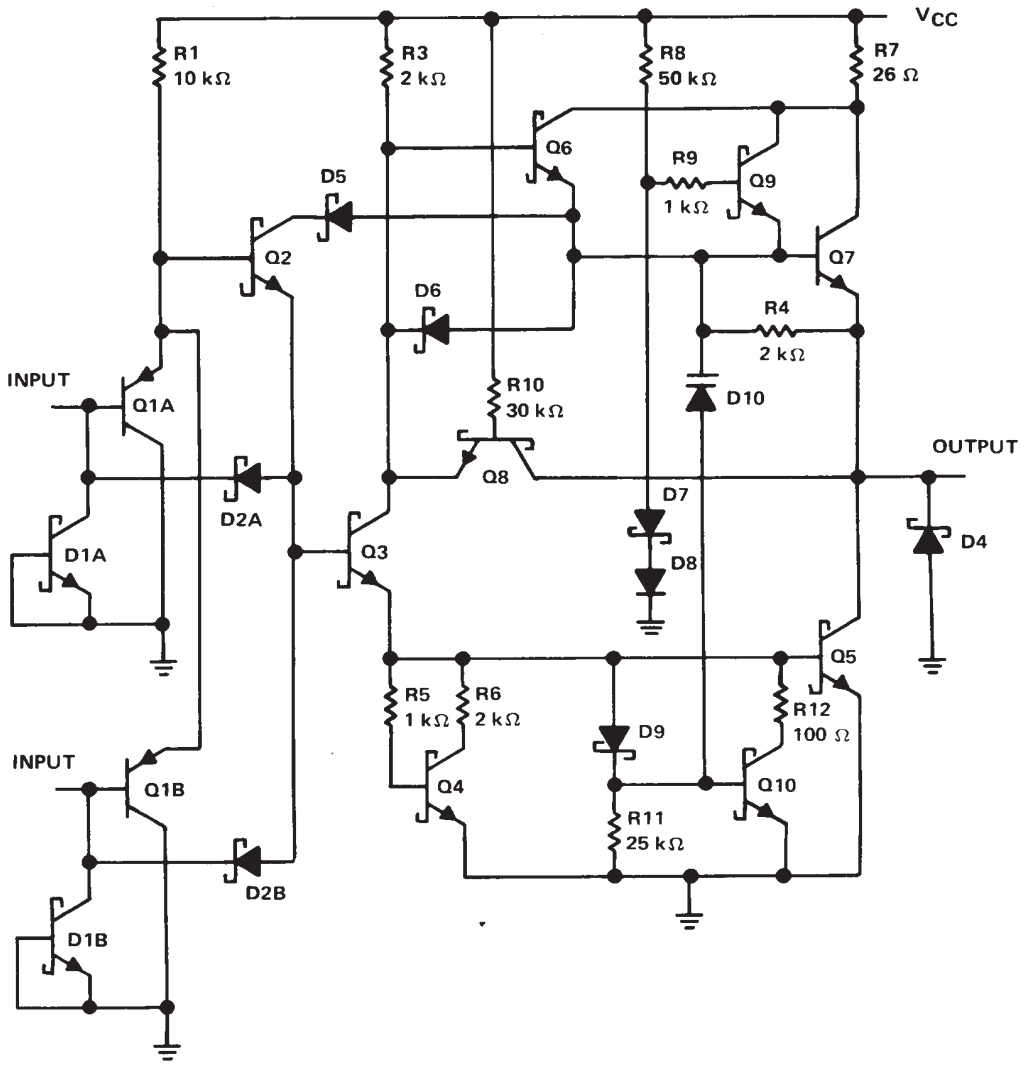


Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC} - V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC} - V_{BE}$ of Q6 $- V_{BE}$ of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than 1 μA and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through } R7} \times R7 - V_{CE} \text{ of Q6} - V_{BE} \text{ of Q7} \quad (3)$$

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14 Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a '54ALS device that is driving a '54ALS device and up to 80 for '74ALS device, that is driving a '74ALS device and provides an ensured low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of '54ALS/'74ALS devices, a factor four times better than '54LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction

overlap of transistor Q5. The same principle is used by diodes D2 and D3 and transistor Q3 in turning off transistor Q7. In addition, the active turn-off design produces a square transfer characteristic.

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are ensured over the entire temperature range (–55°C to 125°C) for series 54ALS/54AS and 0°C to 70°C for series 74ALS/74AS]. In addition, the dc limits are ensured over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} — The voltage value required for a low-level input voltage that ensures operation
- V_{IH} — The voltage value required for a high-level input voltage that ensures operation
- V_{OL} — The ensured maximum low-level output voltage of a gate
- V_{OH} — The ensured minimum high-level output voltage of a gate

With the exception of high-level ouput voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS/'AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

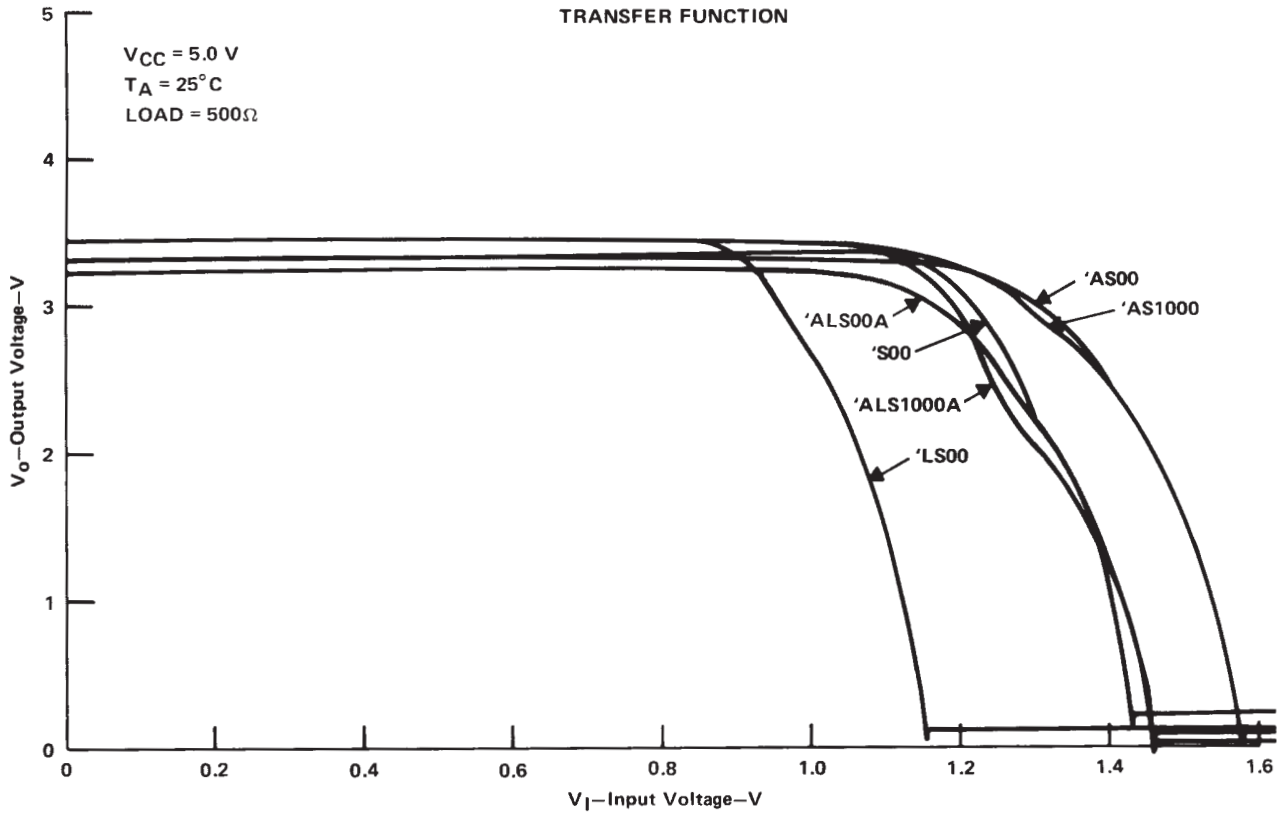


Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

a better high-level noise immunity in 'ALS and and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I, characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out of a device input terminal is designated as negative. Low-level input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

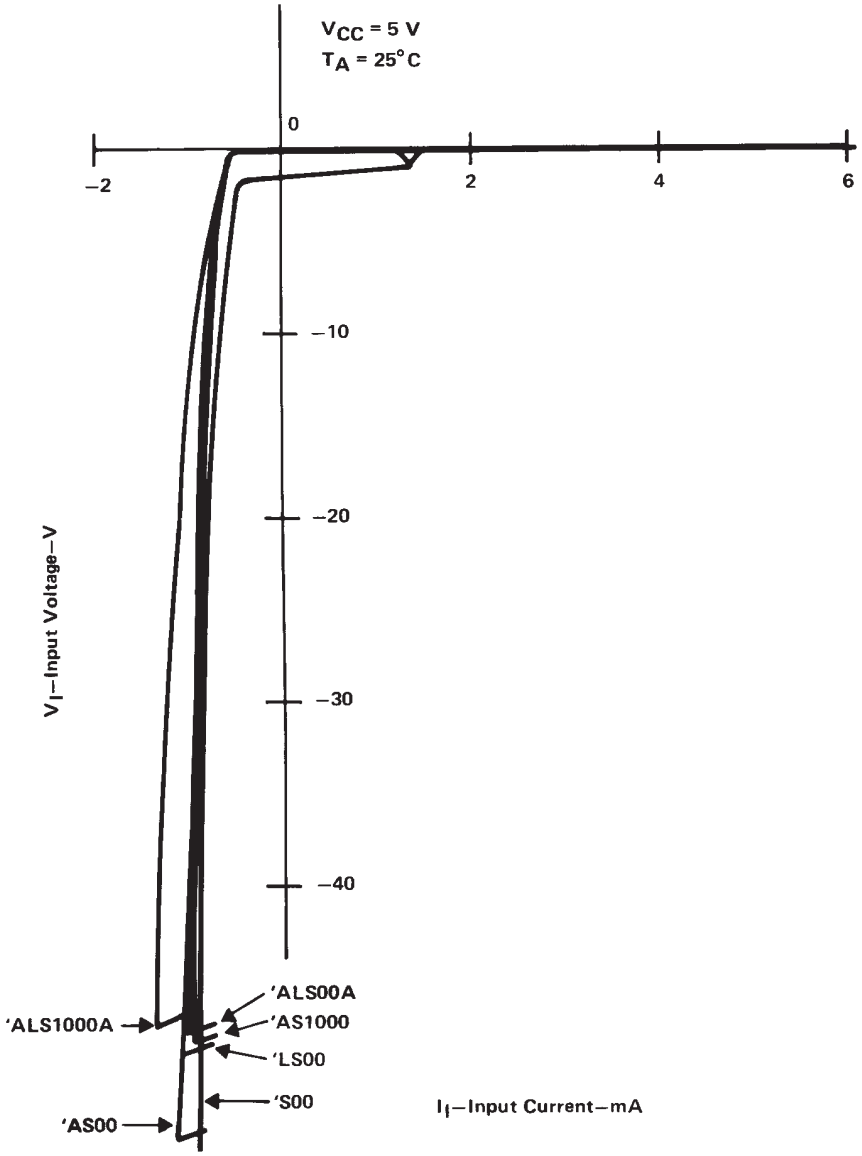


Figure 15. Input Current vs Input Voltage for TTL Families

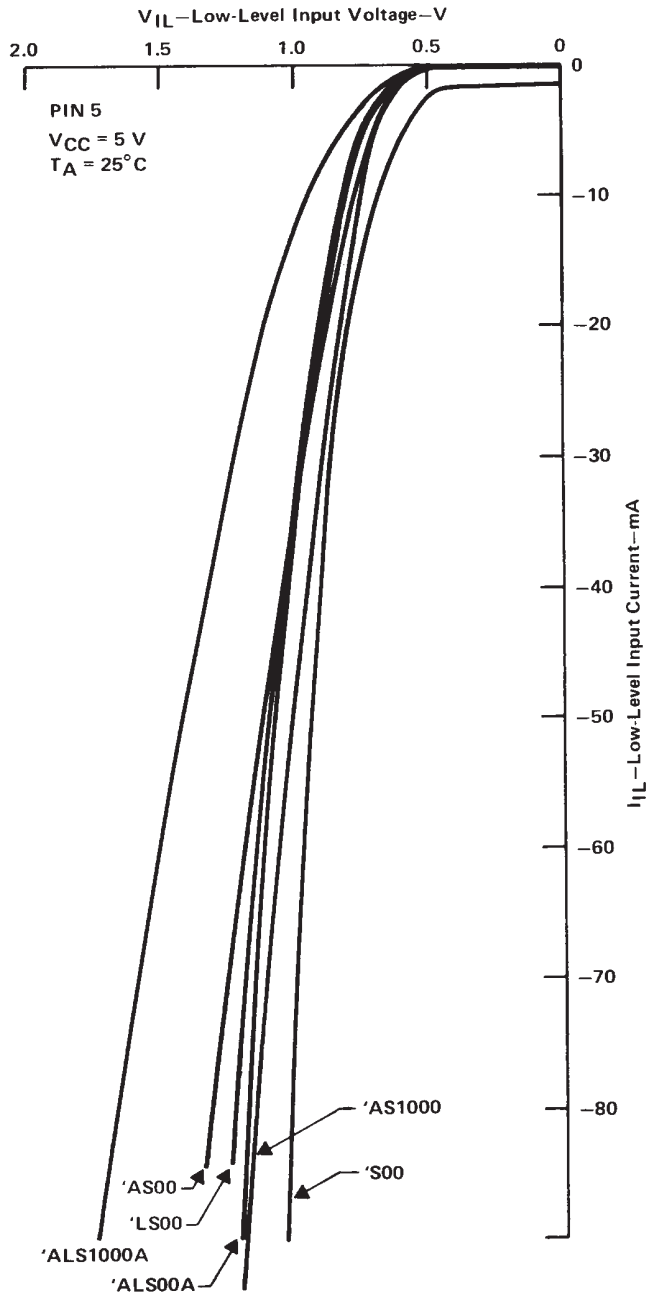


Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

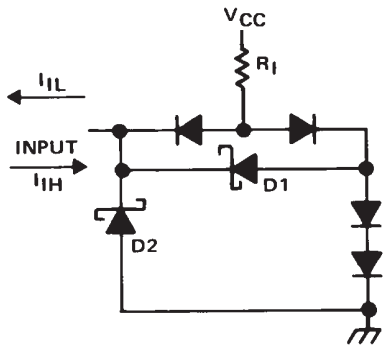


Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than −1.2 V for 'AS and −1.5 V for 'ALS with a forward current of 18 mA. These values are ensured at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdissipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the push-pull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing I_{OS} capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

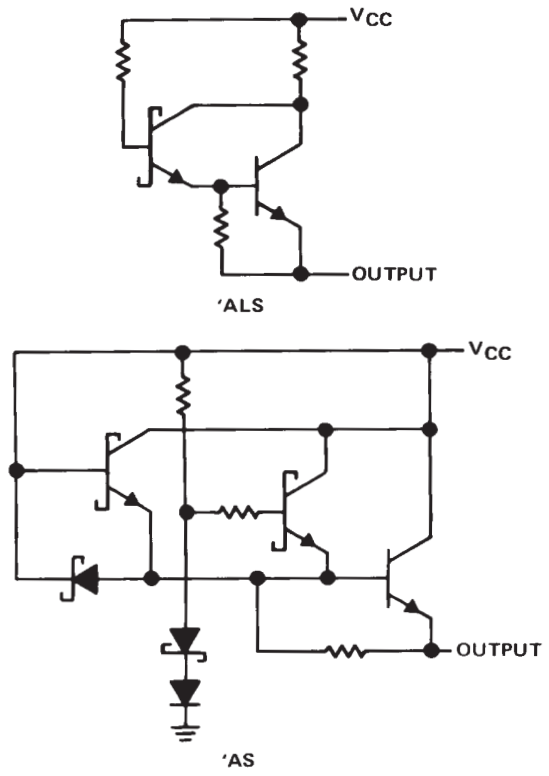


Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage V_{OL}. This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are ensured on Series 'ALS and 'AS gates: propagation delay time for a high-level to low-level at the output t_{PHL}, and a low-level to high-level transition time t_{PLH}. Both parameters are specified with respect to the input pulse using standard test conditions as follows:

V_{CC} = 4.5 V to 5.5 V
C_L = 50 pF
R_L = 500 Ω
T_A = MIN to MAX

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

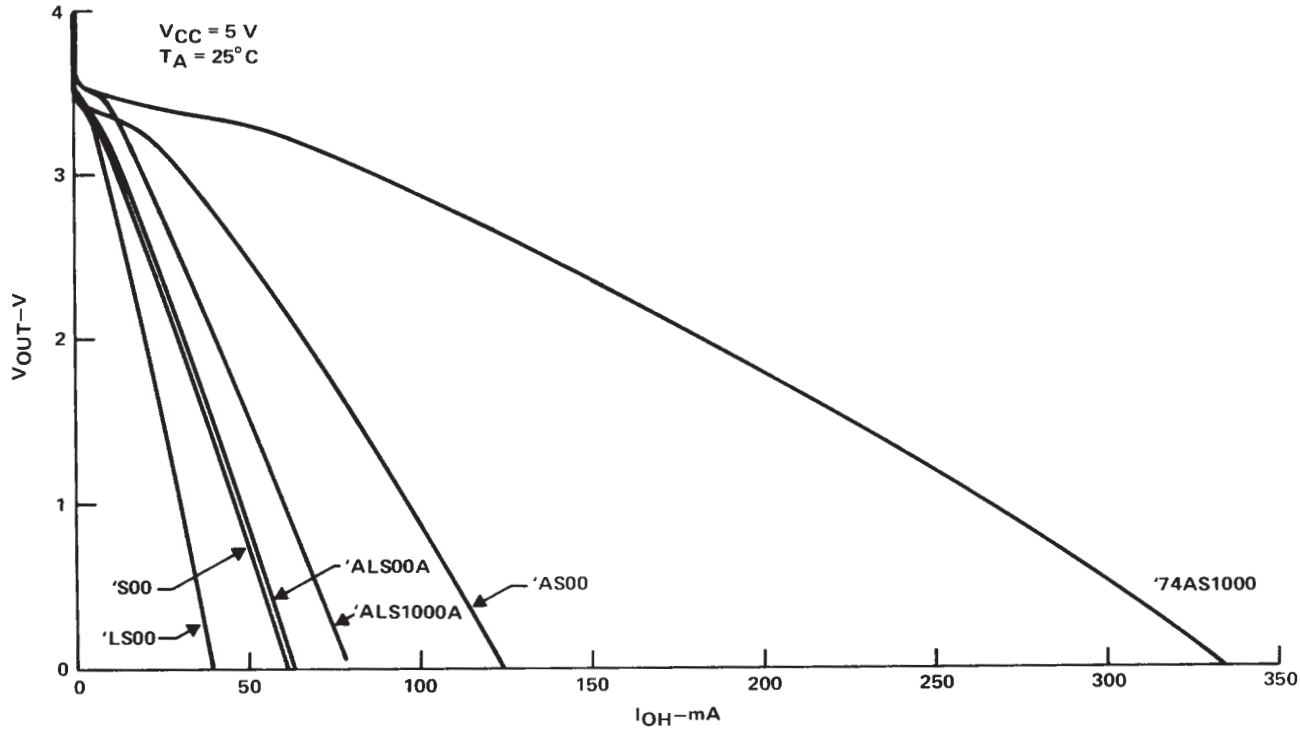


Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification that ensures the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL} maximum) and the ensured worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table 2 lists the worst-case output limits for the 'AS and 'ALS families.

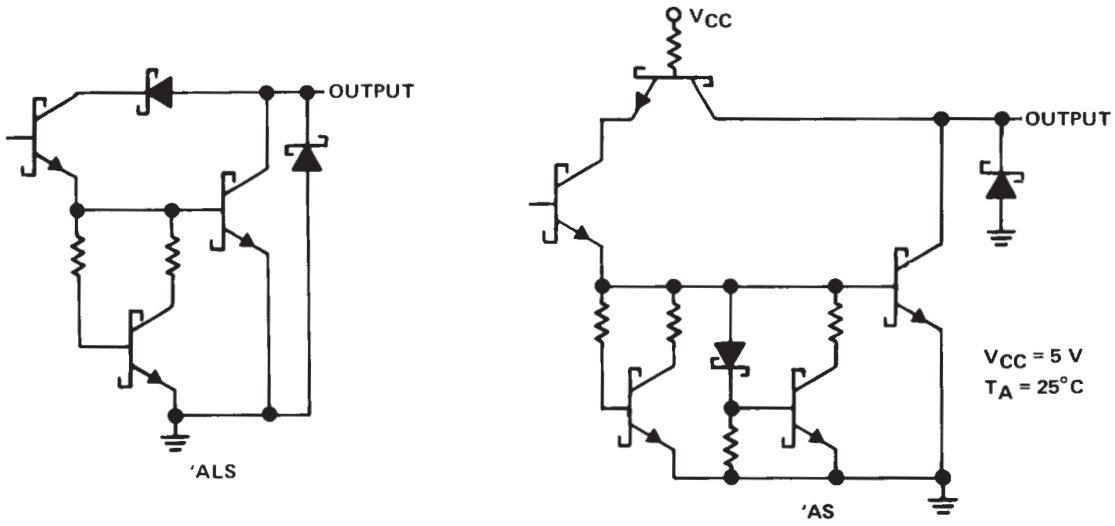


Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

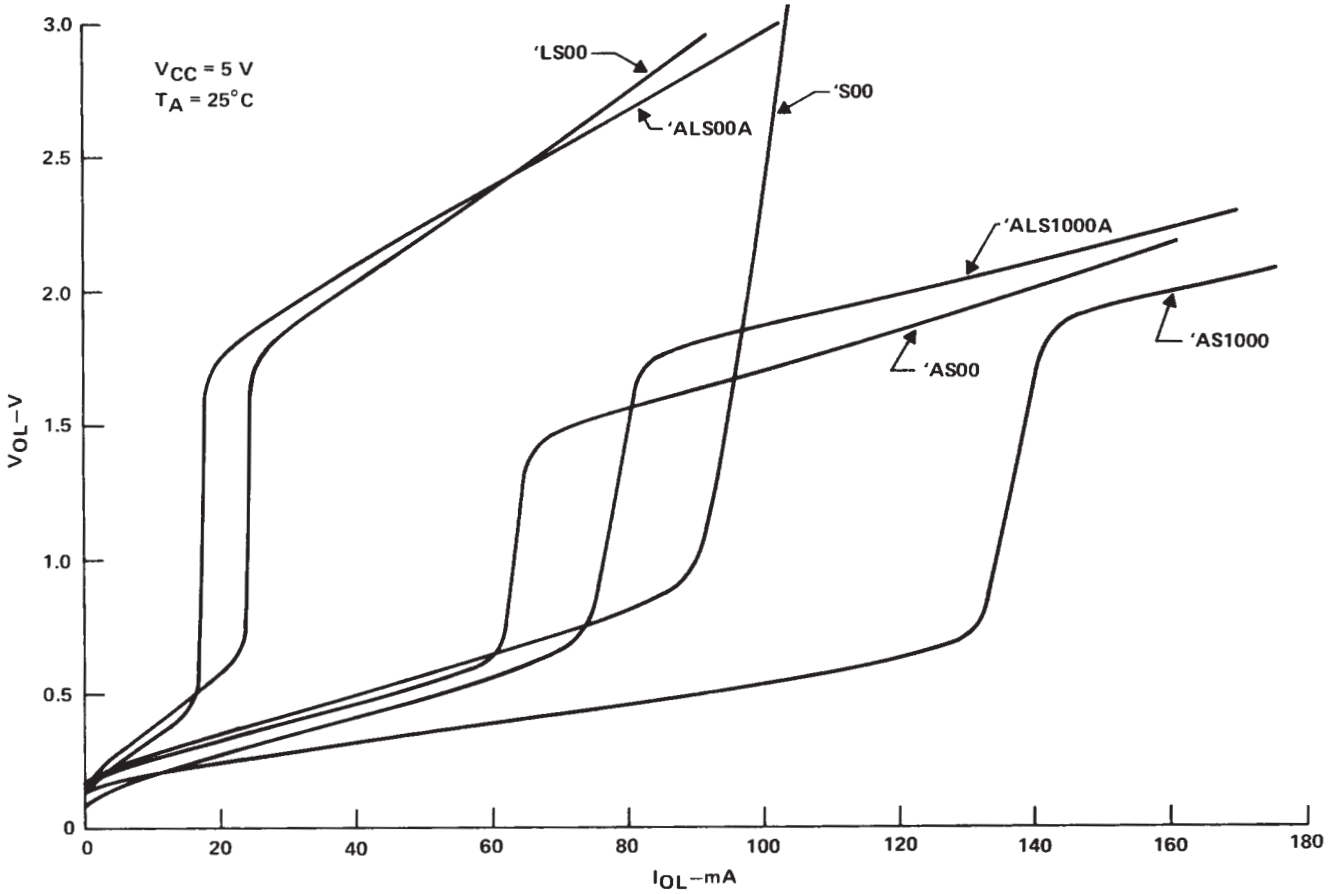


Figure 21. Low-Level Output Voltage vs Low-Level Output Current

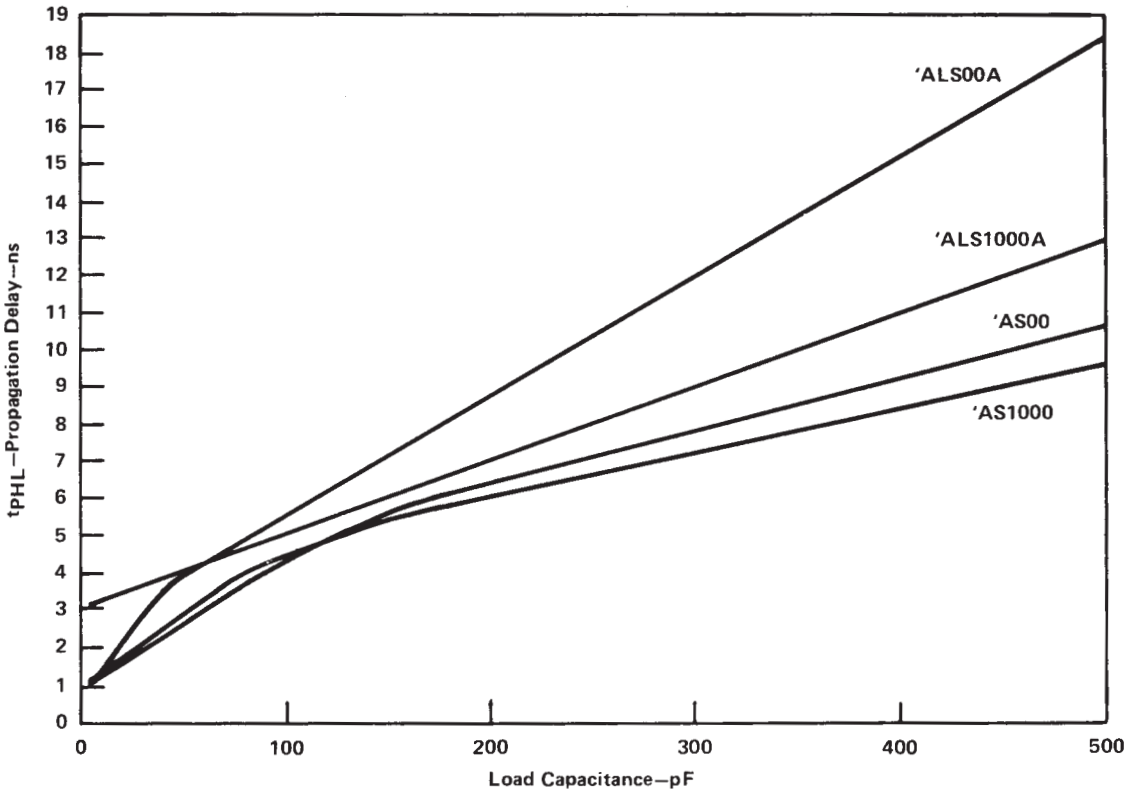


Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

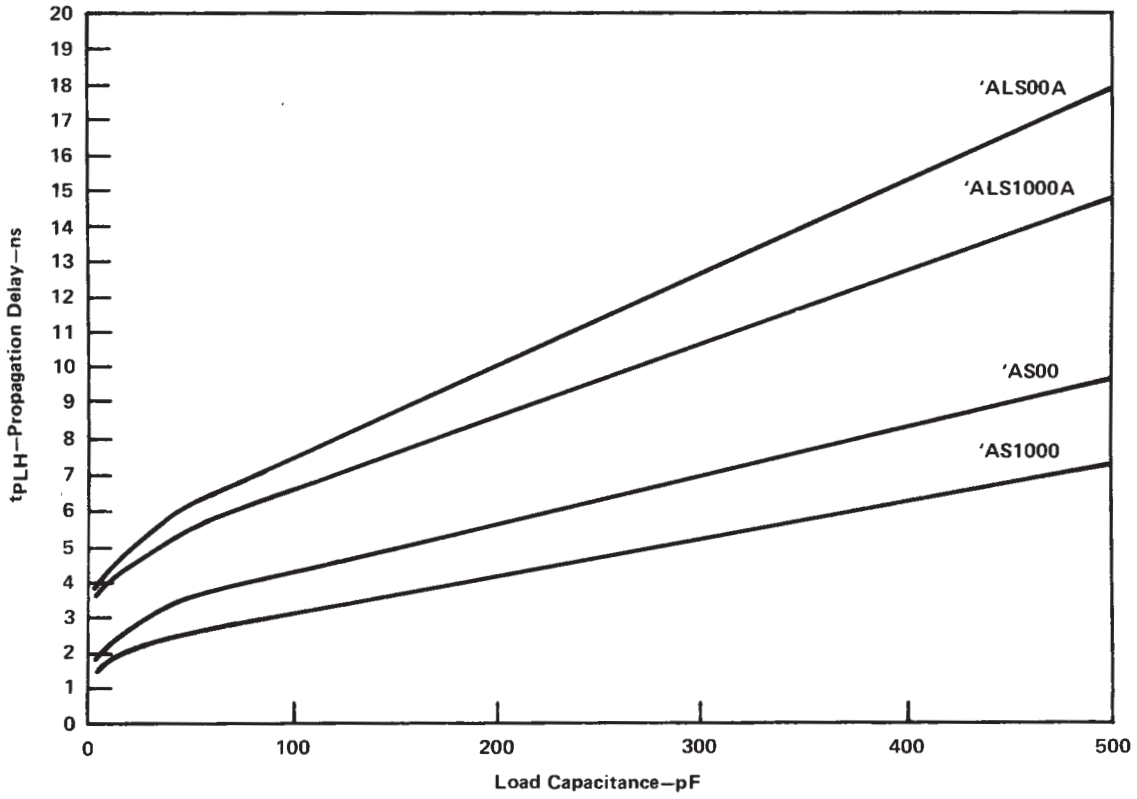


Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

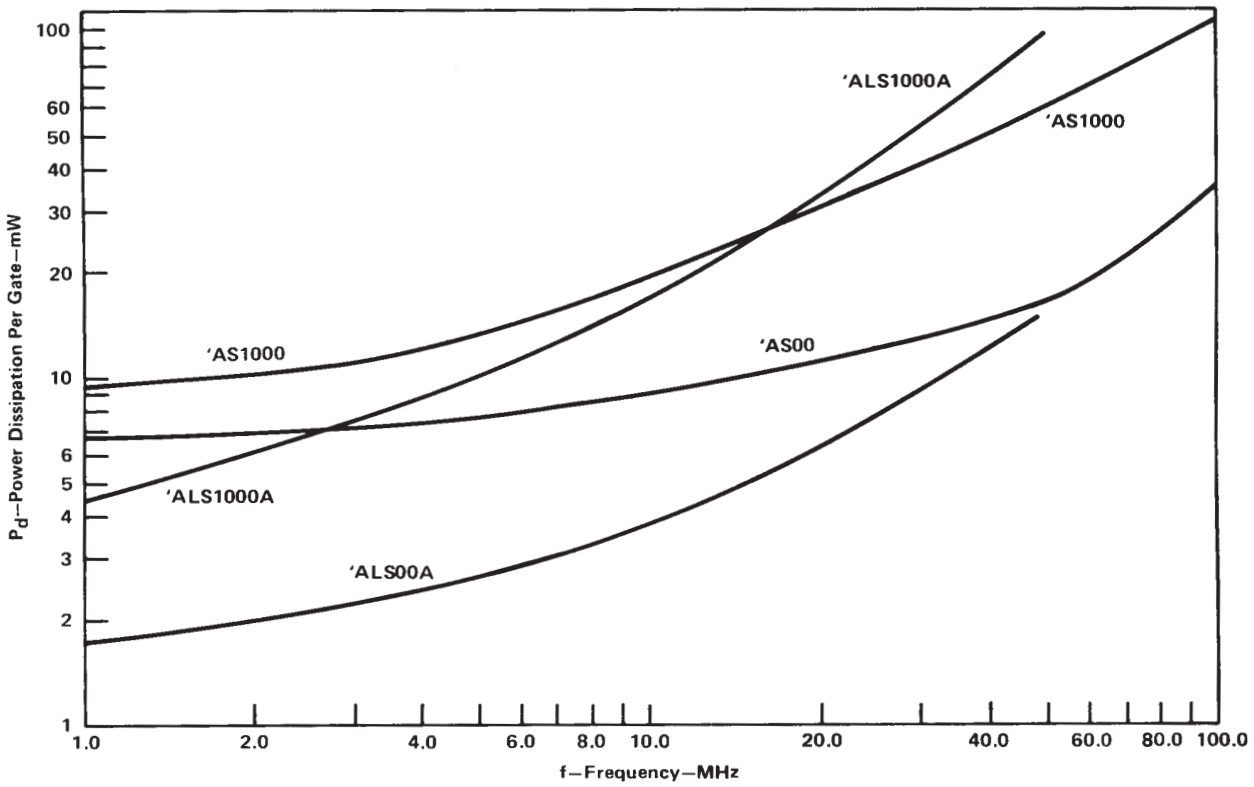


Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting V_{OH} minimum from V_{IH} minimum. The low-level noise margin is obtained by subtracting V_{IL} maximum from V_{OL} maximum. The worst-case high-level noise margin is ensured to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To ensure an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device does not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table 2. Worst Case Output Parameters

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (−55°C to 125°C)	'ALS (−55°C to 125°C)
V_{IH}(MIN)	2	2	2	2
V_{IL}(MAX)	0.8	0.8	0.8	0.8
V_{OH}(MIN) @ $_{CC}$ = 4.5 V*	2.5	2.5	2.5	2.5
V_{OL}(MAX)	0.5	0.5	0.5	0.4
High Level Noise Margin ($V_{OH}-V_{IH}$)	0.5	0.5	0.5	0.5
Low Level Noise Margin ($V_{IL}-V_{OL}$)	0.3	0.3	0.3	0.4

*Actual specification for $V_{OH(min)}$ is V_{CC} − 2 V.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

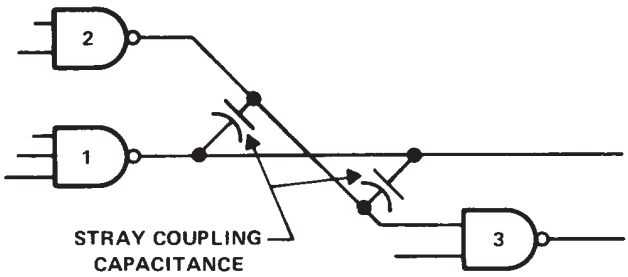


Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed[1] for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse shown in Figure 26(c) is a ramp input.

$$e_i(t) = \frac{E_i}{T}\ t$$

where

E_i = Maximum input voltage and
T = Total rise time of input voltage

The output pulse is represented analytically by

$$e_0(t) = \frac{E_i}{T}\ RC\left(1 - e^{-\frac{t/T}{RC/T}}\right)$$

$$e_0(i) = E_i\ \tau\left(1 - e^{-i/\tau}\right)$$

where

$$\tau = \frac{RC}{T}$$

$$\theta(i) = \tau\left(1 - e^{-i/\tau}\right)$$

$$\theta(i) = \frac{e_{0(i)}}{E_i}$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ. Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i. Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns

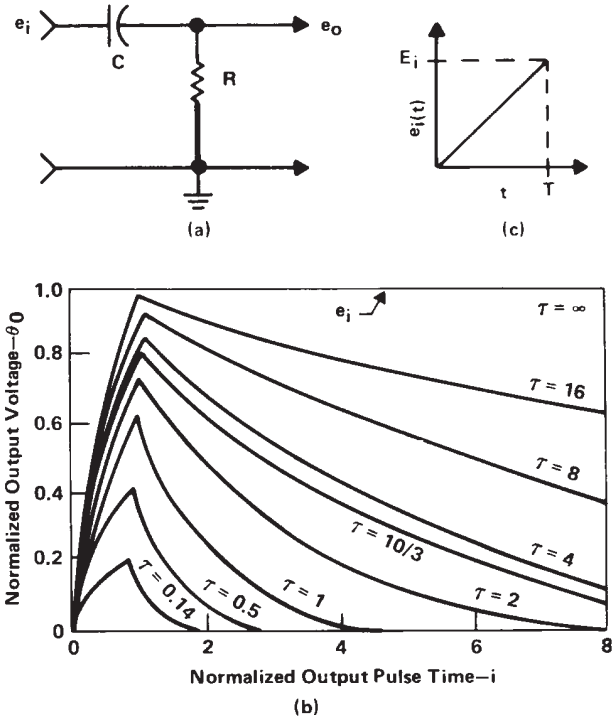


Figure 26. Evaluations of Gate Response to Fast Input Pulses

with gate 2 at a high-logic state. Assume a nominal output impedance of 58 Ω (30 Ω for 'AS) and coupling capacitance of 10 pF. Use the following formula:

$$\text{Total rise time } T = \frac{3\text{ V}}{1\text{ V/ns}^{**}} = 3\text{ ns}^{\dagger}$$

$$\tau = \frac{RC}{T} = \frac{(10 \times 10^{-12})(58)}{3}$$

$$= \frac{0.58 \times 10^{-9}}{3} = 0.19\text{ ns}$$

**2.5 V/ns for 'AS
†1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns. The output voltage scale will be multiplied by 3 V. Using the $\tau = 0.19$ curve gives a peak e_o of 0.57 V (0.19 × 3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (0.57 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

If an open-collector gate is used with a passive 1 kΩ pull-up resistor, the situation would change. Use the following formula:

$$\text{Total rise time} = \frac{3\text{ V}}{1\text{ V/ns}^{**}} = 3\text{ ns}^{\dagger}$$

$$\tau = \frac{(10 \times 10^{-12})(1 \times 10^{3})}{3}$$

$$= \frac{10 \times 10^{-9}}{3} = \frac{10}{3}\text{ ns}$$

**2.5 V/ns for 'AS
†1.2 ns for 'AS

Now the amplitude (from the curves) approaches 2.58 V (0.86 × 3) and the pulse width at the 50% points is approximately 8.52 ns (2.84 × 3). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emphasized noise rejection.

Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate networks and, because of their small size, are more superior in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.

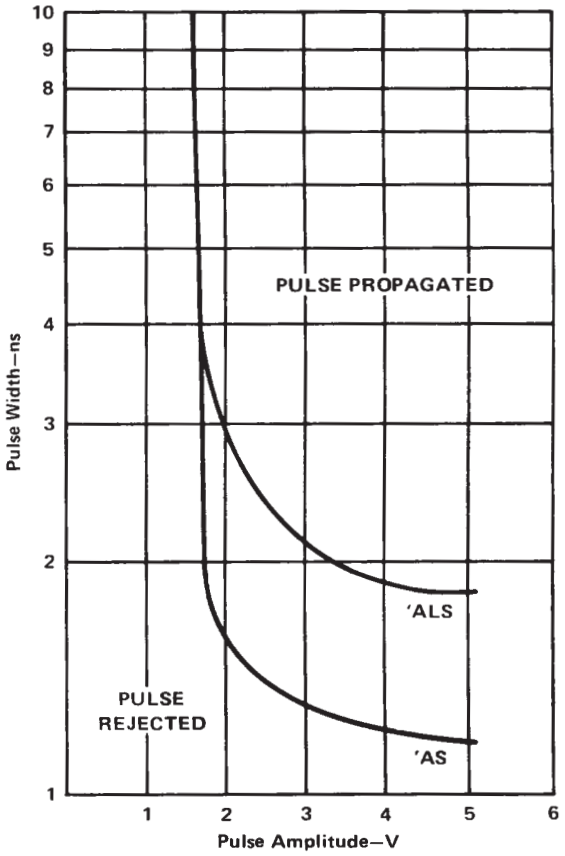
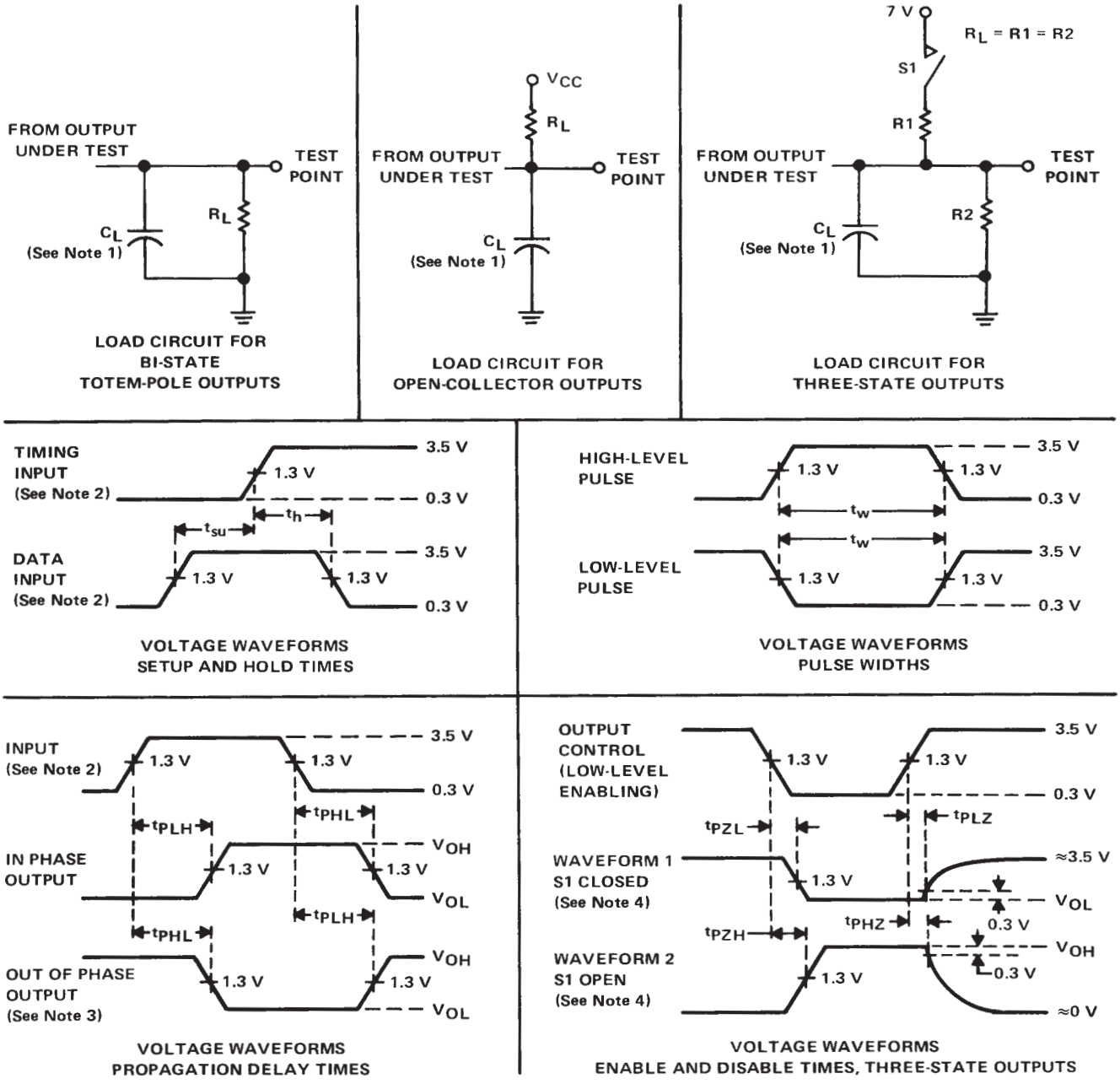


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables 3 through 6 provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.



NOTES: 1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still

operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS/'AS devices is specified as supply voltage -2 V (V_{CC} -2 V).

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

Table 3. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable. Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293−3913). For twisted-pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving end of long cables. This provides added noise margin and more rapid rise times.

Table 4. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table 5. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V_{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 μF capacitors between V_{CC} and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or V_{CC} mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table 6. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Input rise and fall times, as measured between the 10% and 90% amplitude points, should always be faster than 50 ns. Schmitt-trigger input devices do not have this requirement. Input signals should be essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows: 1. Directly to V_{CC}, if the input voltage rating of 5.5 V maximum is not exceeded. 2. Through a resistor equal to or greater than 1 kΩ to V_{CC}. Several inputs can be tied to one resistor. 3. Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased. 4. Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5}$$

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\Delta V_R = V_R\left(\frac{R1/\beta}{R1/\beta + R2}\right)$$

$$= V_R\left(\frac{R1}{R1 + \beta R2}\right)$$

where $R1$ = source impedance
β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30 Ω. Because of cancellation between the driving gate and the driven gate, low-frequency ripple is not a problem.

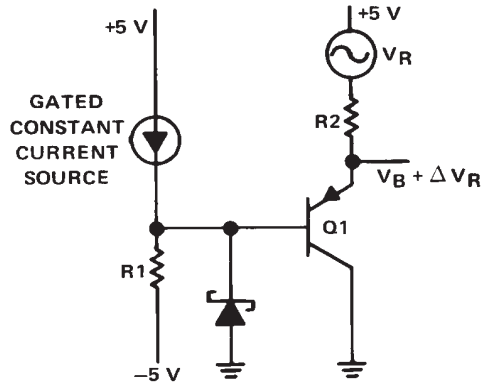


Figure 29. Effect of Source Impedance on Input Noise

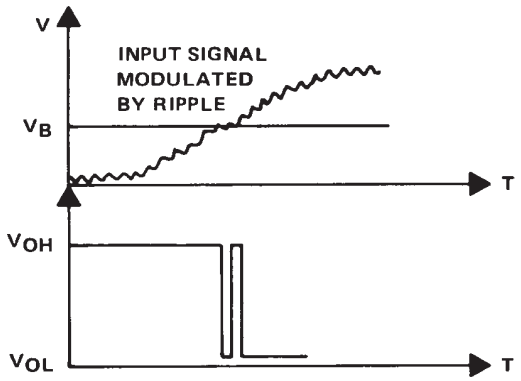


Figure 30. Spurious Output Produced by Supply Voltage Ripple

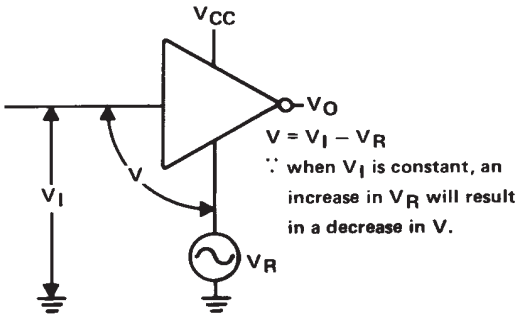


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic

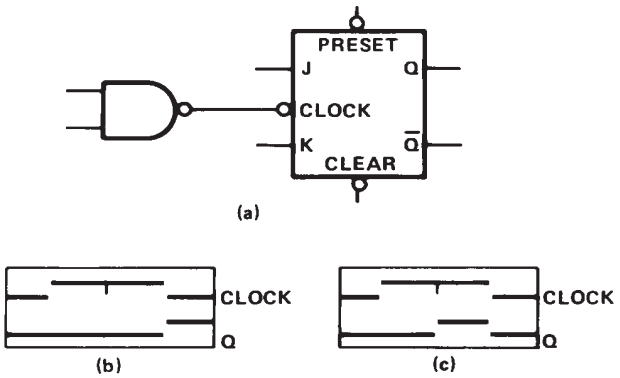


Figure 32. Typical Logic Circuit with Noisy Input

circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)], the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)], the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

1. External noise — External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field generators. The methods of control to be considered are shielding, grounding, or decoupling.
2. Power-line noise — Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
3. Cross talk — Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
4. Signal-current noise — Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
5. Transmission-line reflections — Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
6. Supply-current spikes — Noise caused by switching several digital loads simultaneously. The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc, line driving, etc., must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance Z_S connected to an impedance Z_0, and loaded with a resistance R_L.

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω. When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

$$V_I = E\frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where E = source voltage
Z_0 = line impedance
Z_S = source impedance

For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following equation:

$$I_{line} \quad \frac{V_{in}}{Z_0} \quad = \quad \frac{2.5}{50} \quad = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.

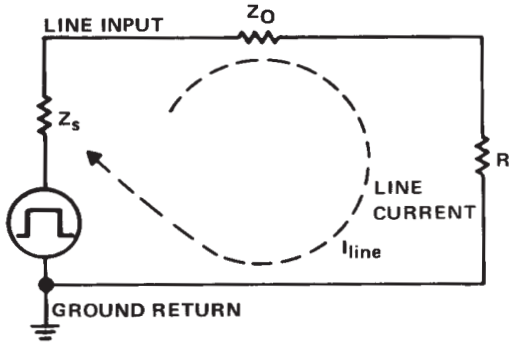
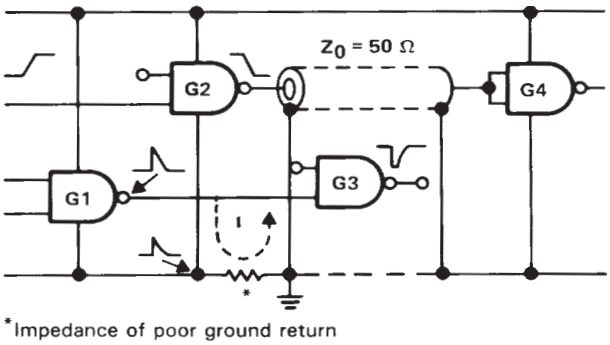


Figure 33. Diagram Representing a Gate Driving a Transmission Line



*Impedance of poor ground return

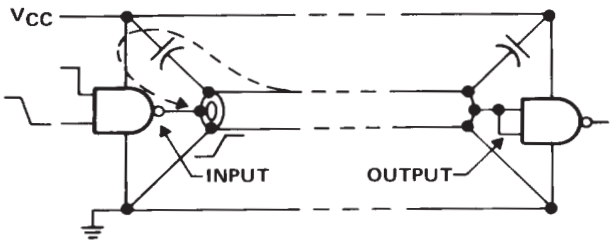
Figure 34. Noise Generation Caused by Poor Transmission-Line Return

2. Decouple the supply voltage of line-driving and line-receiving gates with a 0.1-μF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state, the external loading, the transients caused by charging and discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt} \tag{4}$$

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

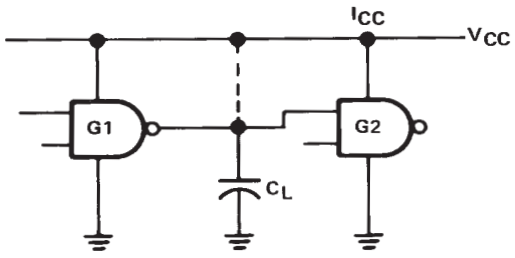


Broken arrow shows path of line-charging current

Figure 35. Ideal Transmission-Line Current Handling

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance C_L (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low,



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

the load capacitance is shorted to ground by transistor Q5 (shown in Figures 12 and 13) and has no effect on supply current.

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors Q7 and Q5 (shown in Figures 12 and 13). The situation arises because transistor Q7 can turn on faster than transistor Q5 can turn off. This places a direct circuit consisting of transistors Q7 and Q5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CC}max = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects: the difference in high-level and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring V_O and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

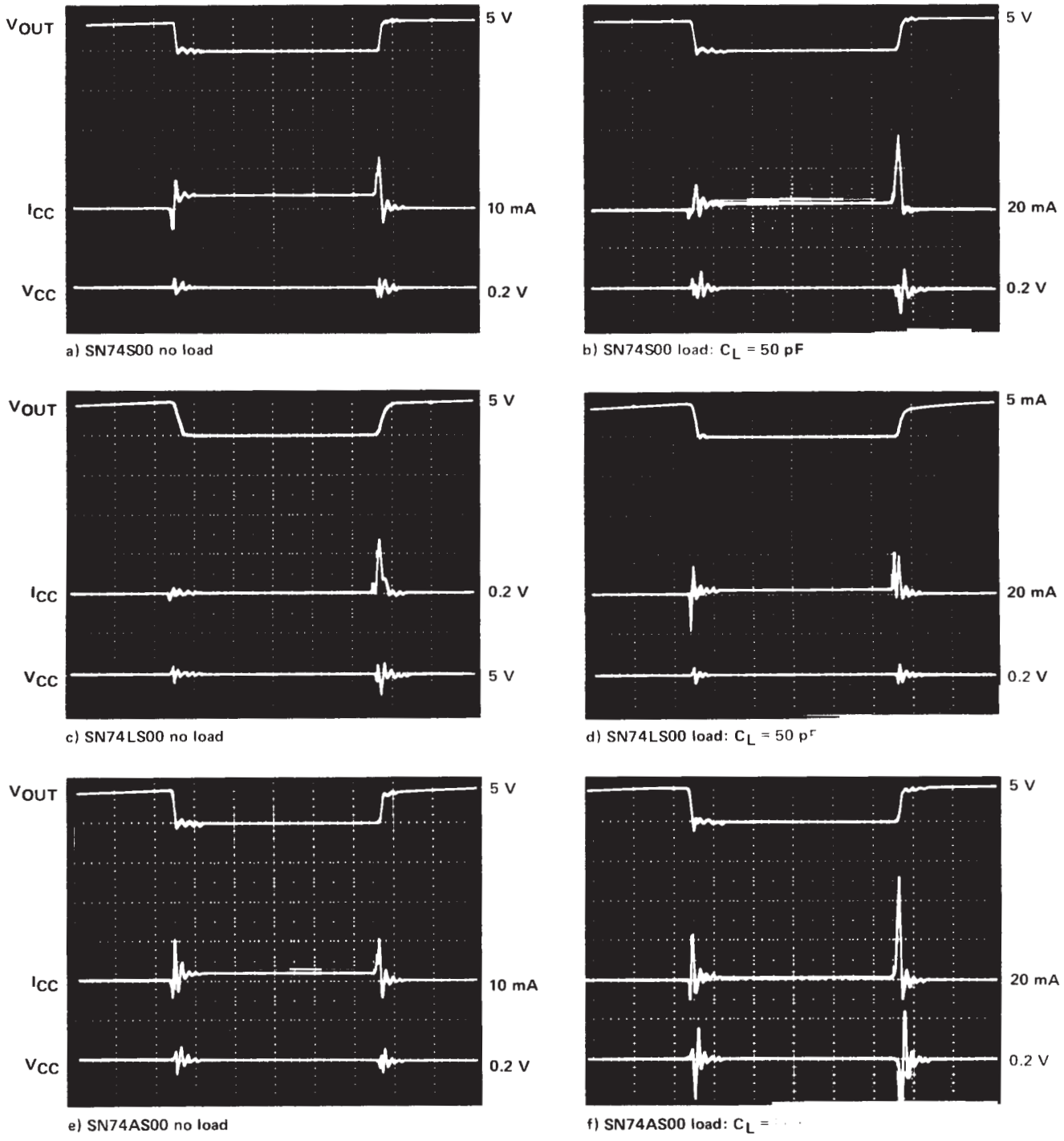
The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of 50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

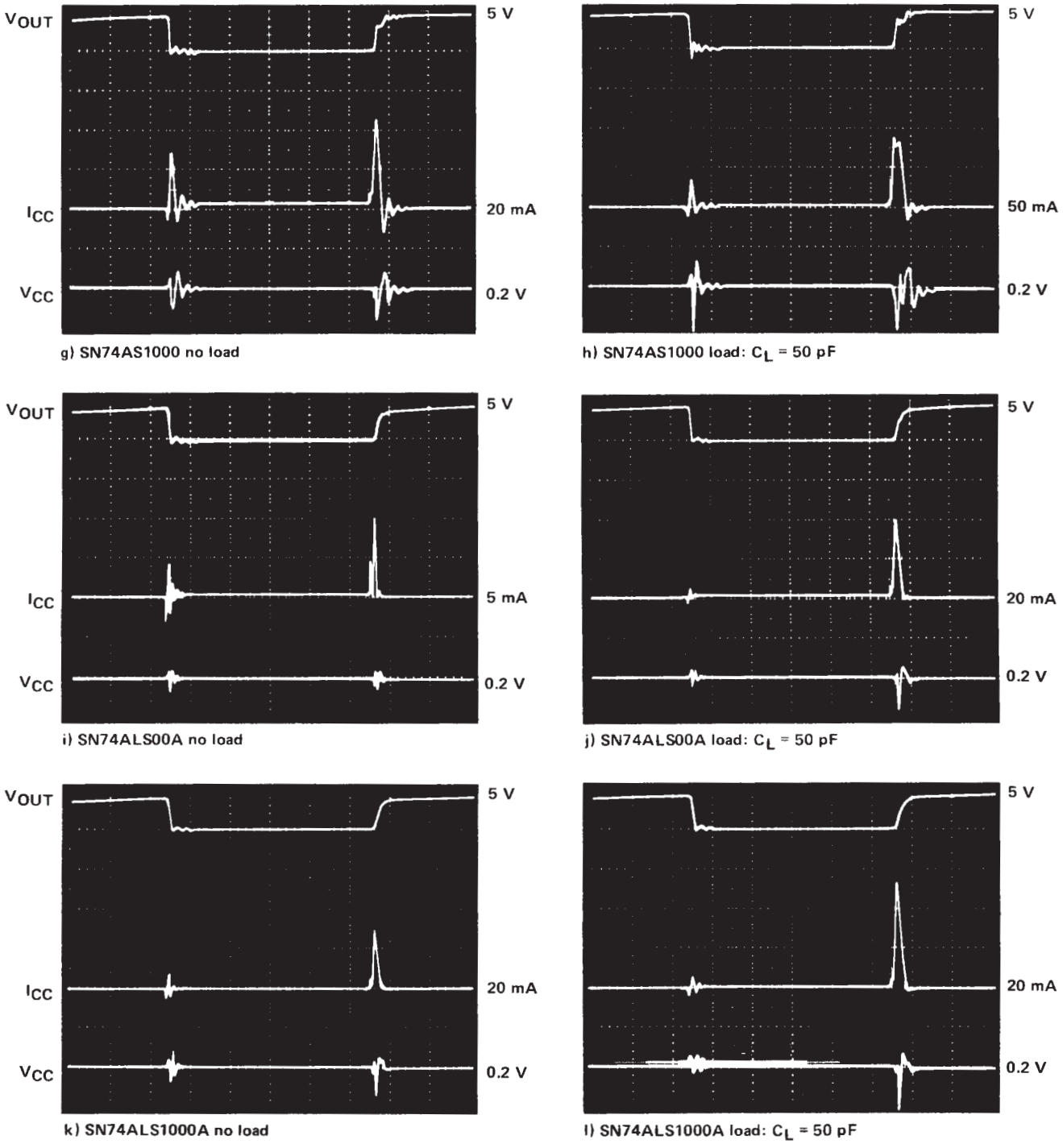
From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(a). Supply-Current Transient Comparisons



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

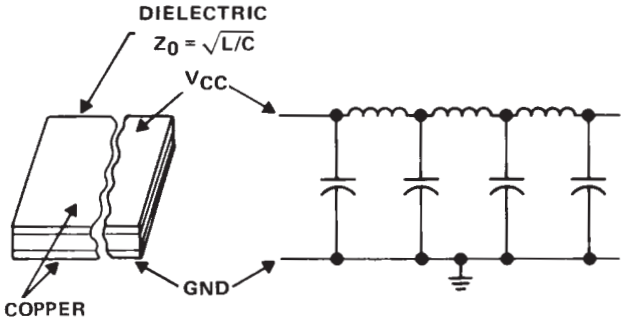


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

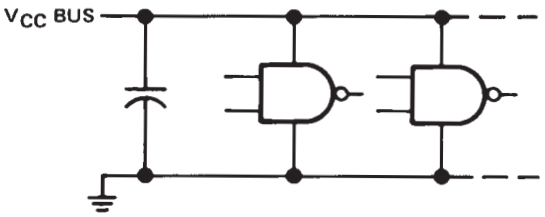


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C1 by assuming that the parameters have common values as follows:

$$\Delta I_{CC} = 50 \text{ mA}$$
$$\Delta V = 0.1 \text{ V}$$
$$\Delta T = 20 \text{ ns}$$

Then the equation is as follows:

$$C1 = \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})}$$

$$= \frac{50 \times 10^{-3}}{0.1} = 10{,}000 \times 10^{-12}$$

$$= 0.01 \ \mu F$$

The same method may be used for the low-frequency capacitor C2. However, the factor ΔT, which was a worst-case transient time for calculating C2, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using 10 μF to 50 μF capacitors.

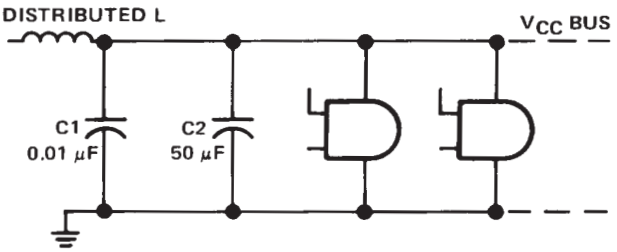


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μH to 10 μH is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

1. Use as wide a ground strap as possible.
2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 μF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

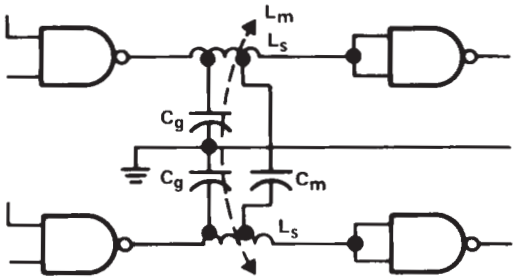
Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

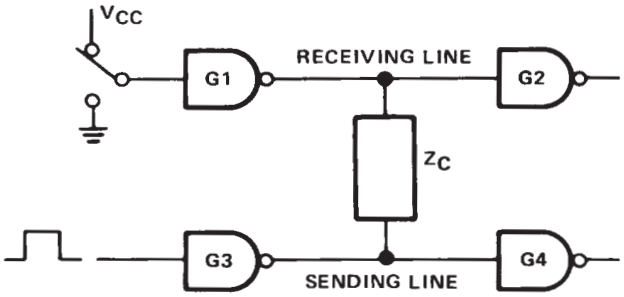


ALL GATES SN74ALS00

Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_c onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.



(Z_C) – COUPLING IMPEDANCE

Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \qquad (5)$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3
R_{S3} = output impedance of gate G3
Z_0 = line impedance
V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_c into

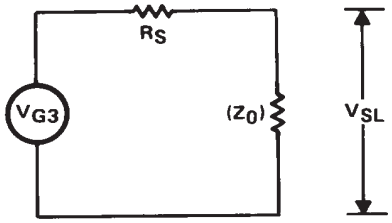


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z_{01} (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5\ Z_0 + Z_c)}$$

The voltage impressed on the receiving line (V_{RL}) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2\ V_{RL} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)\left(\frac{Z_0}{RS3 + Z_0}\right)$$

In the switching period, the transistor has a very low output impedance. Then $R_{S3} \ll Z_0$ and $V_{in(2)}$ can be simplified to the following:

$$V_{in(2)} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)$$

The term $V_{in(2)}/V_{G3}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very high-speed logic circuits has an ensured noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

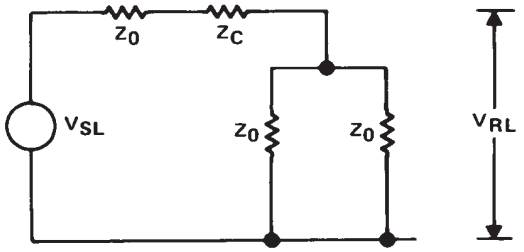


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

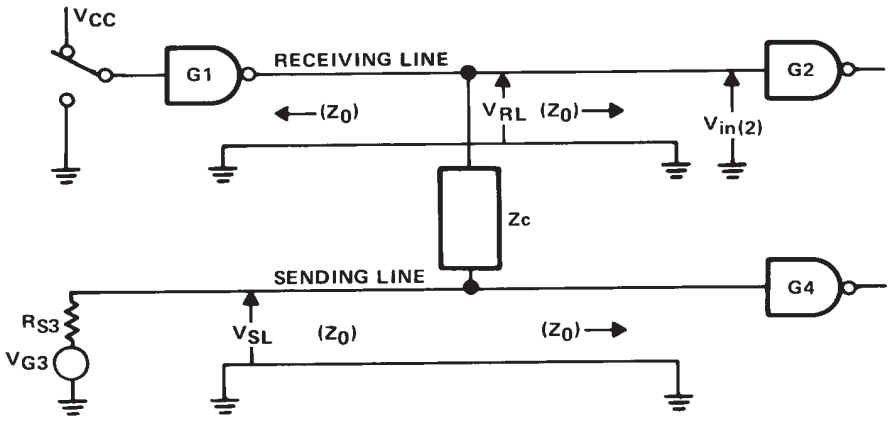


Figure 44. Coupling Impedances Involved in Cross Talk

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables 7 and 8.

Table 7. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance	Capacitance
H (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Relative dielectric constant ≈ 5

Table 8. Typical Impedance of Strip Lines

Dimensions		Line Impedance	Capacitance
H'a = H'b = (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

Relative dielectric constant ≈ 5, and H'a = H'b

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

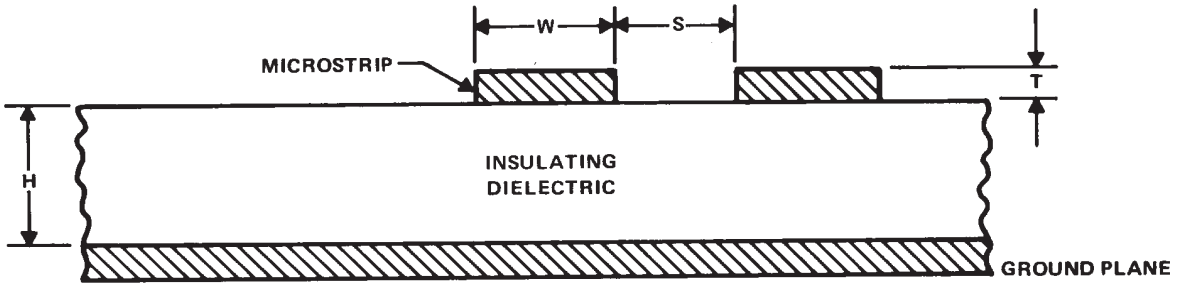


Figure 46. Microstrip Line

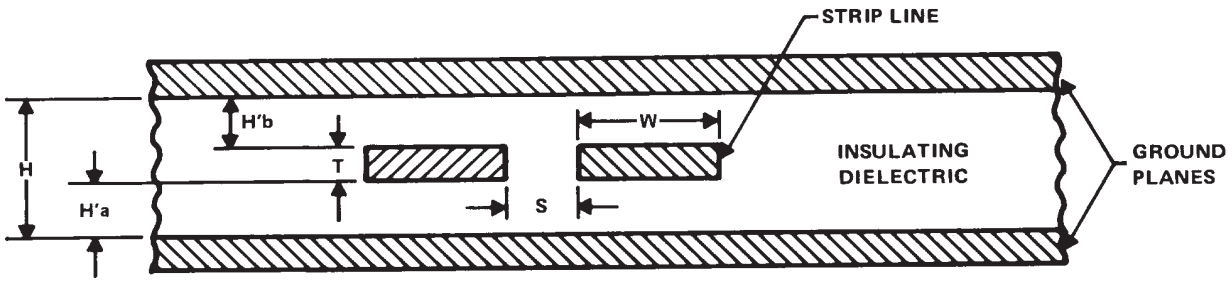


Figure 47. Strip Line

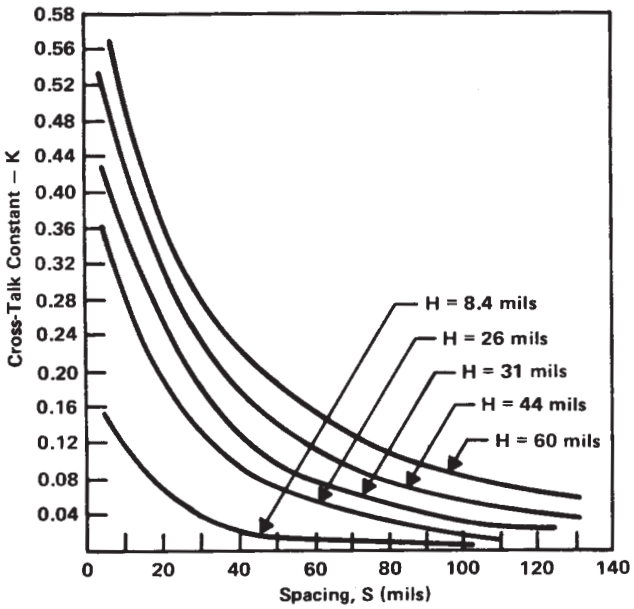


Figure 48. Line Spacing Versus Cross-Talk Constant

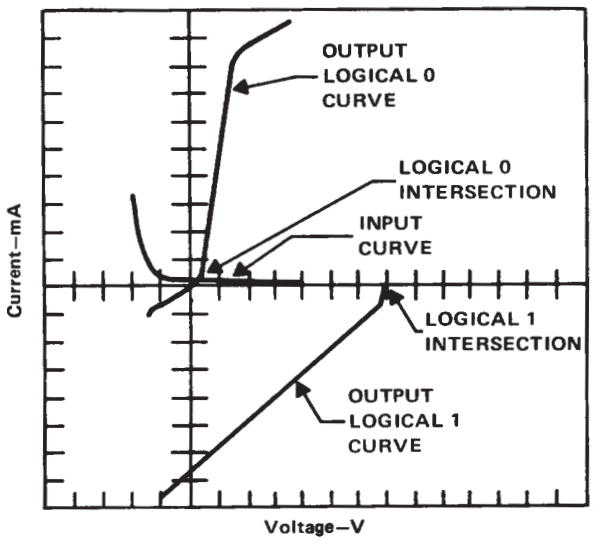


Figure 49. TTL Bergeron Diagram

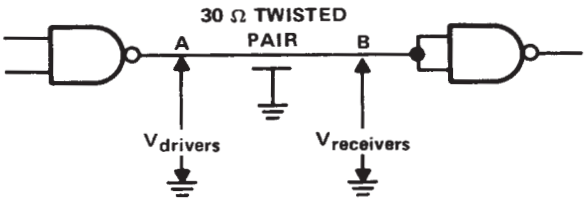


Figure 50. 'ALS/'AS Driving Twisted Pair

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately 30 Ω. To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ (Z_0 = 30 Ω), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)} - t_n$ = time delay of line], the receiving gate sees −0.7 V. Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0, the driver output rises to 2.2 V and, at time t_1, the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

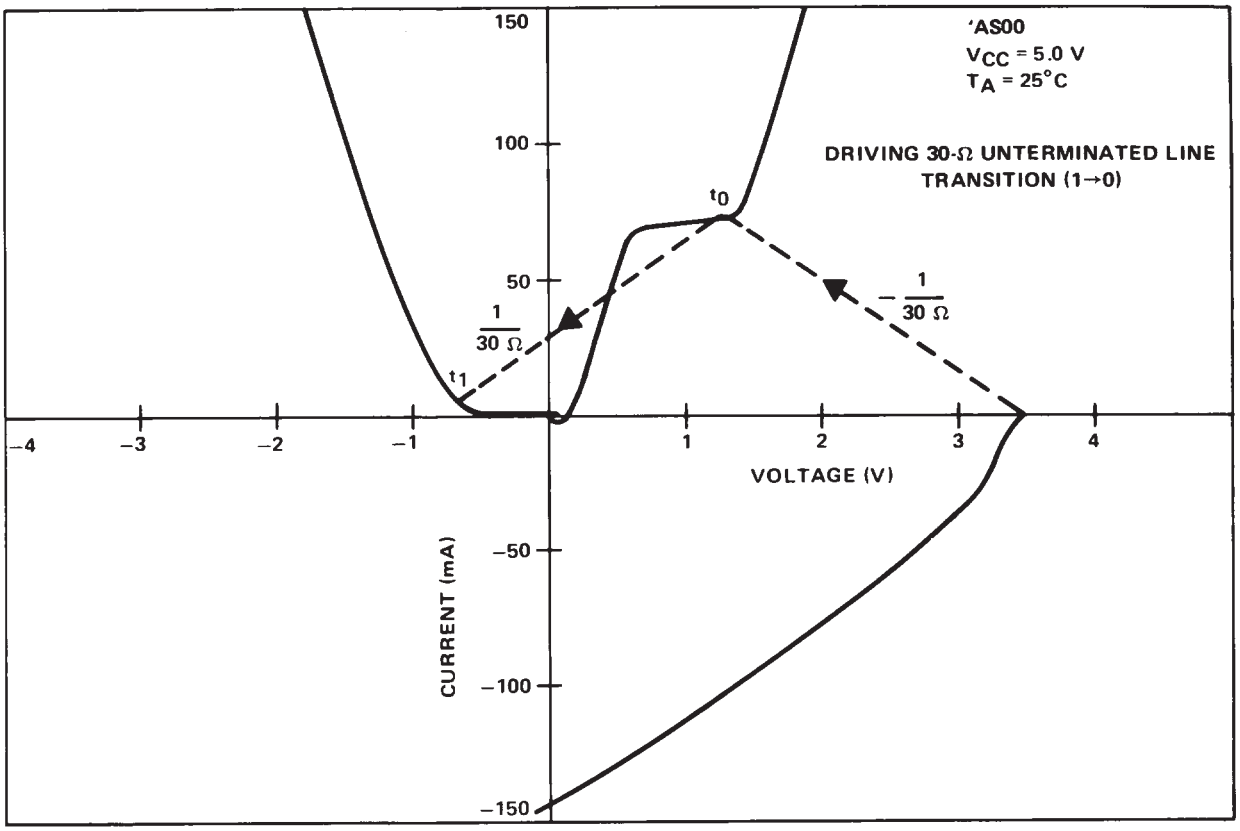


Figure 51. 'AS −ve Transition Bergeron Diagram

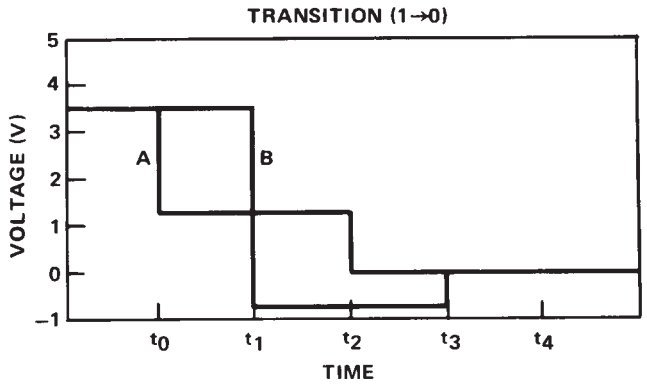


Figure 52. 'AS −ve Voltage/Time Plot

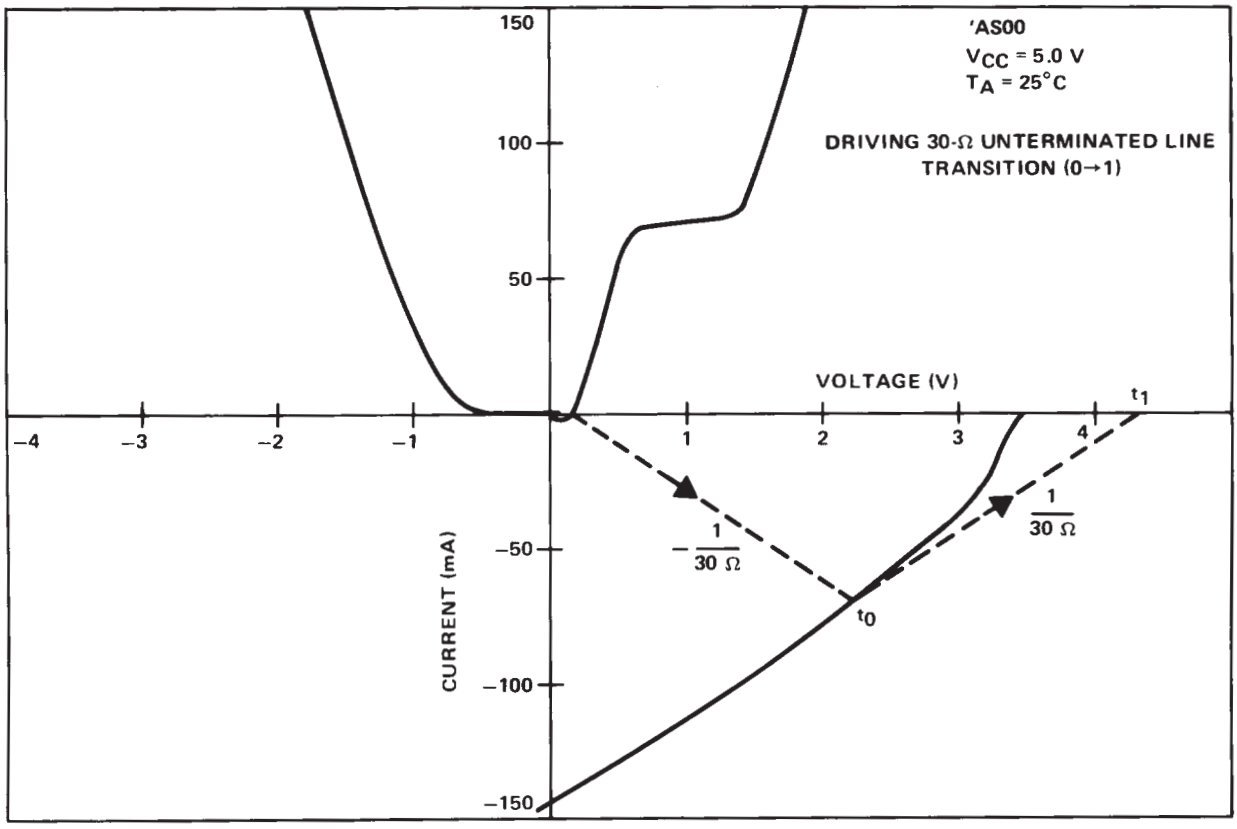


Figure 53. 'AS +ve Transition Bergeron Diagram

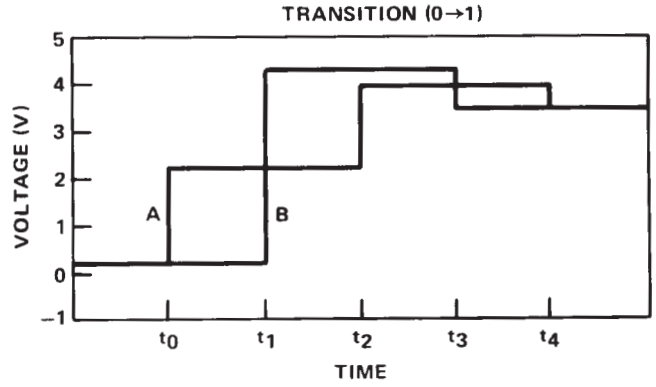


Figure 54. 'AS +ve Voltage/Time Plot

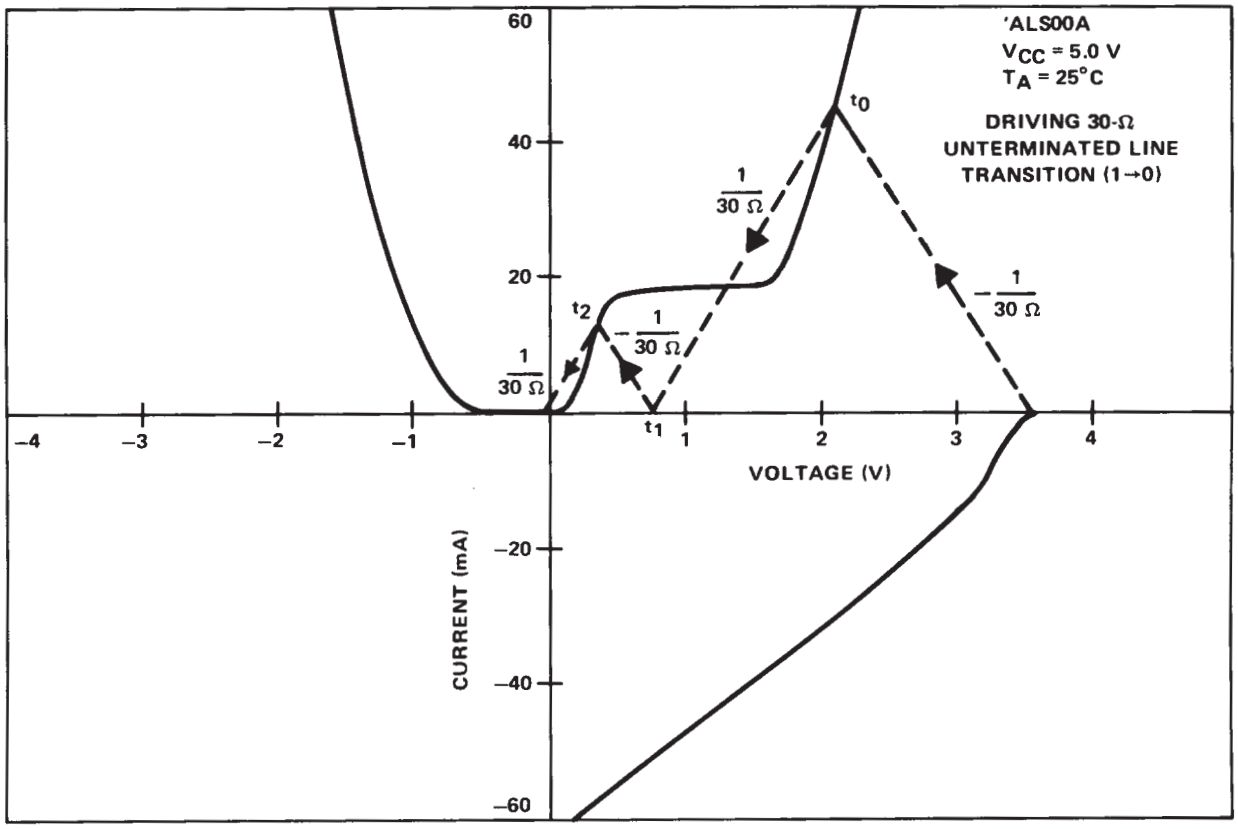


Figure 55. 'ALS −ve Transition Bergeron Diagram

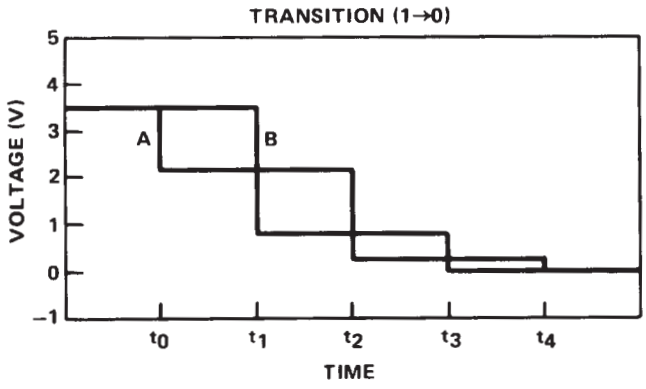


Figure 56. 'ALS −ve Voltage/Time Plot

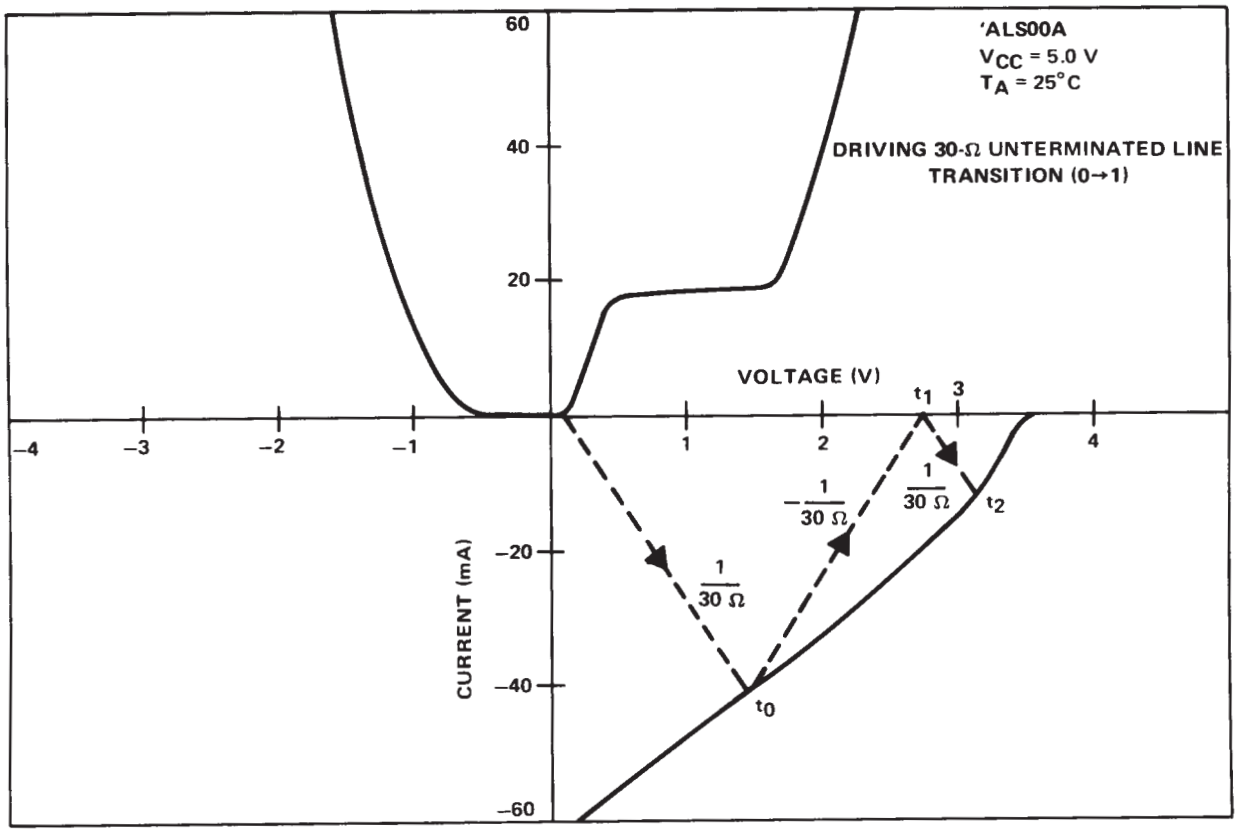


Figure 57. 'ALS +ve Transition Bergeron Diagram

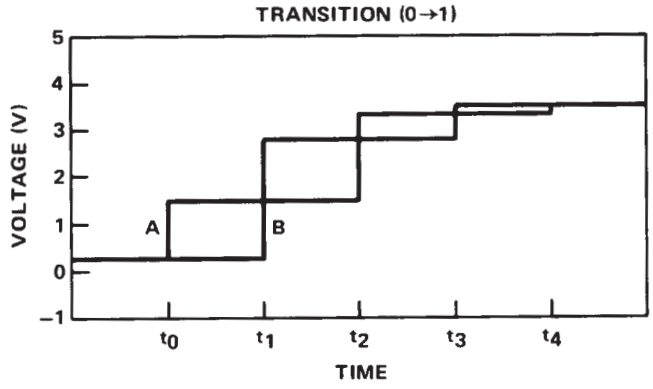


Figure 58. 'ALS +ve Voltage/Time Plot

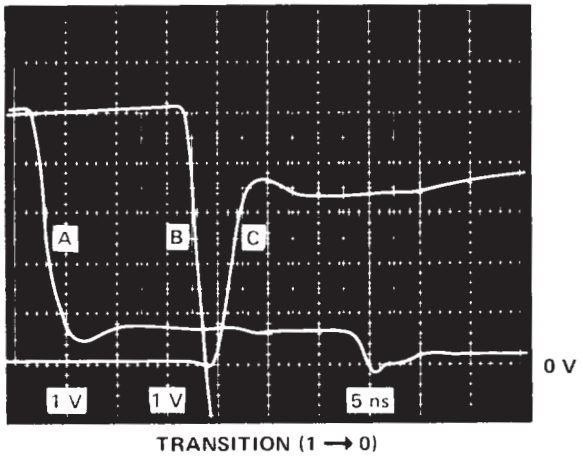


Figure 59. Oscilloscope Photograph of 'AS001 −ve Transition Using 50-Ohm Line

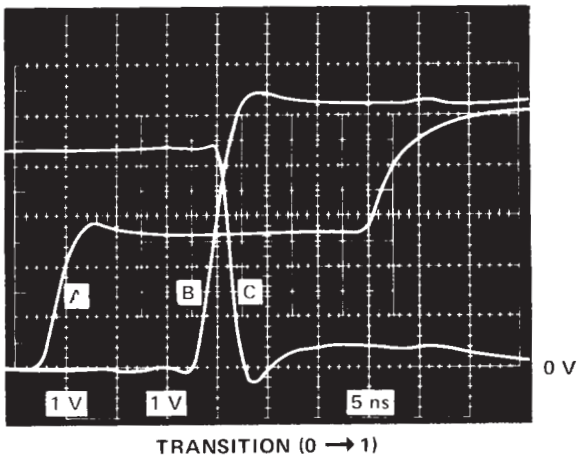


Figure 60. Oscilloscope Photograph of 'AS00 +ve Transition Using 50-Ohm Line

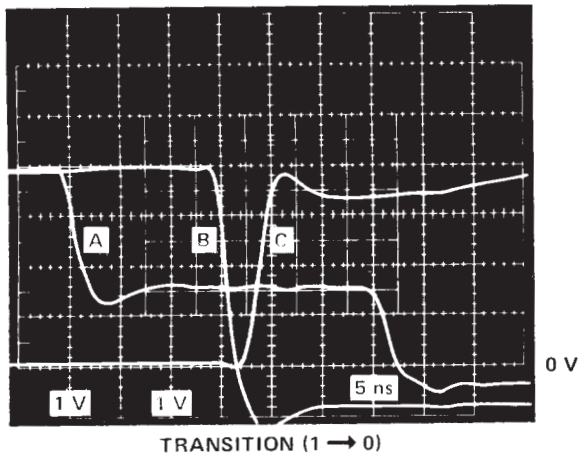


Figure 61. Oscilloscope Photograph of 'AS00 −ve Transition Using 25-Ohm Line

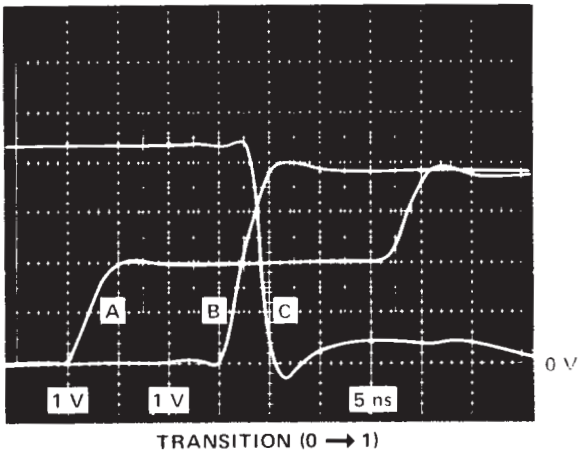


Figure 62. Oscilloscope Photograph of 'AS00 +ve Transition Using 25-Ohm Line

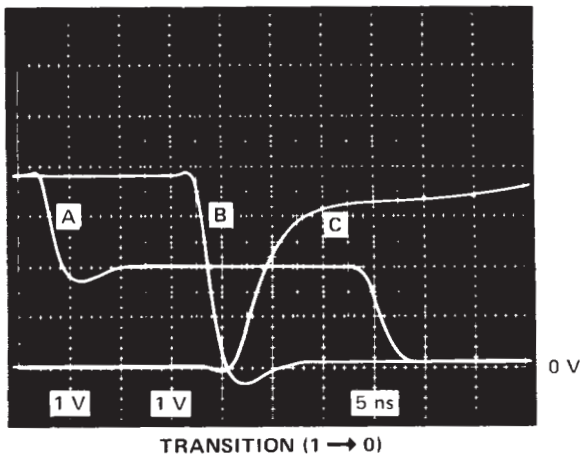


Figure 63. Oscilloscope Photograph of 'ALS00A −ve Transition Using 50-Ohm Line

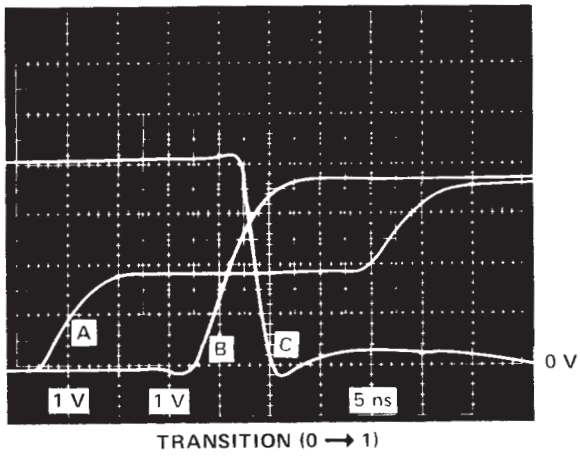


Figure 64. Oscilloscope Photograph of 'ALS00A +ve Transition Using 50-Ohm Line

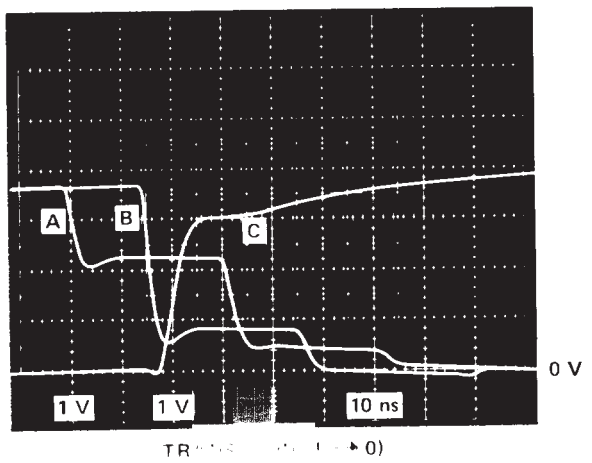


Figure 65. Oscilloscope Photograph of 'ALS00A −ve Transition Using 25-Ohm Line

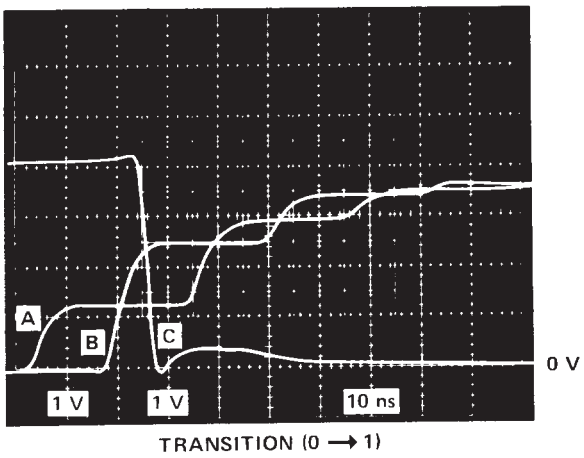


Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

1. W.C. Elmore and M. Sands, *Electronics Experimental Techniques*, McGraw-Hill Book Co., New York, 30ff. (1949).
2. M. Williams and S. Miller, *Series 54ALS/74ALS Schottky TTL Applications B215*, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A
Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input cuurent requirements in Table A-1), which can be summed and compared directly to the fanout capability (see Table A-2) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-1 AND A-2

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-1). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-2.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

Table A-1. Normalized Input Currents

SERIES	I/O	INPUT CURRENT (mA)	INPUT CURRENT NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
54/7400	HI	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54/74L00	HI	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-1 is normally used (in combination with Table A-2) when replacing one logic family with another in an existing system.

Table A-2 is normally used when originally designing a system which employs several TTL families to optimize performance.

Table A-2. Fanout Capability (Output Currents Normalized to Input Currents)

SERIES	I/O	OUTPUT CURRENT (mA)	OUTPUT DRIVE NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
			*HI 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02
			†LO 1.6	2	0.18	0.4	2	0.5	0.1	0.5	0.1
54/7400	HI	0.4	10	8	40	20	8	20	20	20	20
54/7400	LO	16	10	8	88.89	40	8	32	160	32	160
54H/74H00	HI	0.5	12.5	10	50	25	10	25	25	25	25
54H/74H00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54L00	HI	0.1	2.5	2	10	5	2	5	5	5	5
54L00	LO	2	1.25	1	11.11	5	1	4	20	4	20
74L00	HI	0.2	5	4	20	10	4	10	10	10	10
74L00	LO	3.6	2.25	1.8	20	9	1.8	7.2	36	7.2	36
54LS/74LS00	HI	0.4	10	8	40	20	8	20	20	20	20
54LS00	LO	4	2.5	2	22.22	10	2	8	40	8	40
74LS00	LO	8	5	4	44.44	20	4	16	80	16	80
54S/74S00	HI	1	25	20	100	50	20	50	50	50	50
54S/74S00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54AS/74AS00	HI	2	50	40	200	100	40	100	100	100	100
54AS/74AS00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54ALS/74ALS00A	HI	0.4	10	8	40	20	8	20	20	20	20
54ALS00A	LO	4	2.5	2	22.22	10	2	8	40	8	40
74ALS00A	LO	8	5	4	44.44	20	4	16	80	16	80
54AS1000	HI	40	1000	800	4000	2000	800	2000	2000	2000	2000
54AS1000	LO	40	25	20	222.22	100	20	80	400	80	400
74AS1000	HI	48	1200	960	4800	2400	960	2400	2400	2400	2400
74AS1000	LO	48	30	24	266.67	120	24	96	480	96	480
54ALS1000A	HI	1	25	20	100	50	20	50	50	50	50
54ALS1000A	LO	12	7.5	6	66.67	30	6	24	120	24	120
74ALS1000A	HI	2	65	52	260	130	52	130	130	130	130
74ALS1000A	LO	24	15	12	133.33	60	12	48	240	48	240

*Input Current HI

†Input Curent LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} **High-level input voltage**
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is expected.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is expected.

V_{T+} **Positive-going threshold voltage**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold voltage**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} **High-level output voltage**
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ **On-state output voltage**
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ **Off-state output voltage**
The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} **High-level input current**
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current flowing into* an input when a specified low-level voltage is applied to that input.

*Current flowing out of a terminal is a negative value.

I_{OH} **High-level output current**
The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

$I_{O(off)}$ **Off-state output current**
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} **Short-circuit output current**
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} **Supply current, output(s) high**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} **Output disable time (of a three-state output) from high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} **Output disable time (of a three-state output) from low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} **Transition time, low-to-high-level output**
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} **Transition time, high-to-low-level output**
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Average pulse width**
The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

*Current flowing out of a terminal is a negative value.

t_h **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

$t_{release}$ **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated ''release time'' falls within the setup interval and constitutes, in effect, a negative hold time.

t_{su} **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**
Integrated circuits of less complexity than medium-scale integration (MSI).

*Current flowing out of a terminal is a negative value.