# *Advanced Low-Voltage Technology*

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## Abstract

ALVT, the advanced low-voltage logic family, offers high-performance BiCMOS devices that are functional at 3.3-V and 2.5-V $V_{CC}$ and have low propagation delay, low static-power consumption, and 64 mA current drive. Other features include 5-V tolerance; auto3-state; bus hold; partial power down, hot insertion, and live insertion; and excellent simultaneous-switching and output-skew performance.

## Introduction

Texas Instruments (TI™) ALVT (advanced low-voltage logic) family is the next-generation low-voltage technology that has been optimized for customer applications. This application report includes ALVT characterization information to aid design engineers in more accurately designing their digital logic systems. The focus is on the family's features and benefits, product characteristics, and design guidelines. The state-of-the-art features that have been available in the 5-V Advanced BiCMOS technology, are now available with the ALVT, the higher performance low-voltage technology that is fabricated using state-of-the-art 0.65-micron BiCMOS technology for bus-interface functions. This application report is intended to be used as a designer's guide for component selection and usage. The ALVT family is functional at 3.3-V and 2.5-V $V_{CC}$ and is 5-V tolerant at 3.3-V $V_{CC}$. ALVT provides superior performance, with 2.5-ns propagation delay, current drive of 64 mA, and static power consumption of 0.1 mA.

## Customer Applications for ALVT

The ALVT family was created to drive lower impedances in backplane applications. Several key issues are important in backplane applications, including topics such as live insertion; power-up 3-state; 5-V tolerance; signal integrity, including ground bounce; bus hold; and bus contention.

The ALVT family can operate at a $V_{CC}$ from 2.5 V to 3.3 V. It is 30% faster than the LVT family and is one of the fastest families in 5-V and the 3.3-V ranges. The ALVT family is initially targeted for the Widebus™ (16-bit) devices and features damping-resistor versions that minimize undershoot in bus-driving applications.

## Input Characteristics

ALVT has a CMOS input structure (see Figure 1). The input is an inverter consisting of a p-channel to $V_{CC}$ and an n-channel to GND. When a low voltage level is applied to the input, the p-channel transistor is on, and the n-channel transistor is off, resulting in current flowing from $V_{CC}$, pulling the $V_{out}$ node (at the input stage) to a high state. When a high level is applied, the n-channel transistor is on, the p-channel transistor is off, and the current flows to GND, pulling the $V_{out}$ node (at the input stage) to a low state. However, there is a state at the input transition when the n-channel and the p-channel transistors are turned on simultaneously, generating a current path between $V_{CC}$ and GND. This could damage the transistors, depending on the length of time the signal lies in the threshold region, which is 0.8 V to 2 V ($V_{CC}$ = 3.3 V ± 0.3 V). The supply current can increase to 35 mA per input, peaking at approximately 1.5-V $V_I$ (at 3.6-V $V_{CC}$) (see Figure 2).

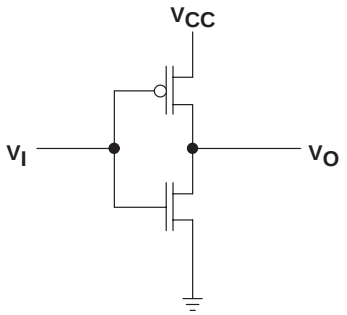


**Figure 1. ALVT Input Structure**

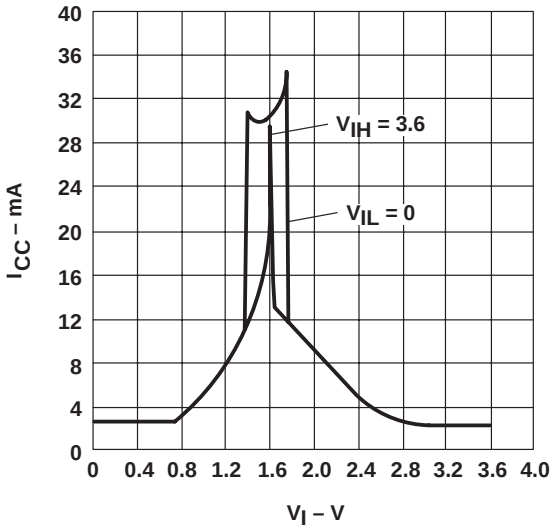


**Figure 2. $I_{CC}$ vs $V_{IN}$ for ALVTH16244**

ALVT devices function at 2.5-V and 3.3-V $V_{CC}$, and the corresponding input-high and input-low levels are shown in Table 1.

**Table 1. ALVT Functions at 2.5 V and 3.3 V**

| VOLTAGE LEVELS | 2.5-V $V_{CC}$ | 3.3-V $V_{CC}$ |
|---|---|---|
| $V_{IH}$ (min) | 1.7 V | 2.0 V |
| VIL (max) | 0.7 V | 0.8 V |

## Output Characteristics

Figure 3 shows the simplified output circuit of a typical ALVT device. The Schottky diode (D1) is used to block the reverse current in certain power-down applications. The MOS transistors at the output allow rail-to-rail switching, while the bipolar transistors provide current switching and high-drive capability. The NMOS transistor (M2) is responsible for the low level and provides edge-rate control in the high-to-low transition. The circuit for the 5-V tolerance and the auto3-state are connected as shown in Figure 3.

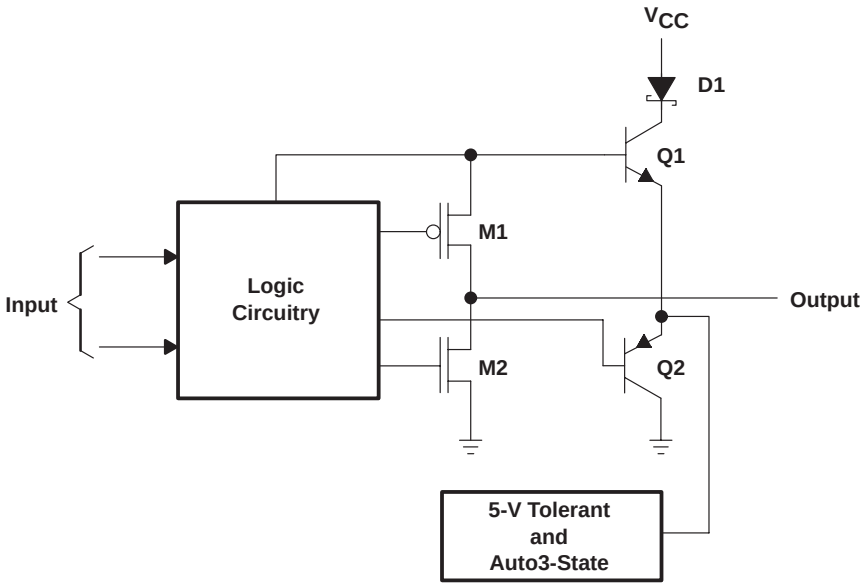


**Figure 3. ALVT Output Circuit**

Figure 4 illustrates values of $I_{OH}$ and $I_{OL}$ and the corresponding values of $V_{OH}$ and $V_{OL}$ for the ALVTH16244 device.

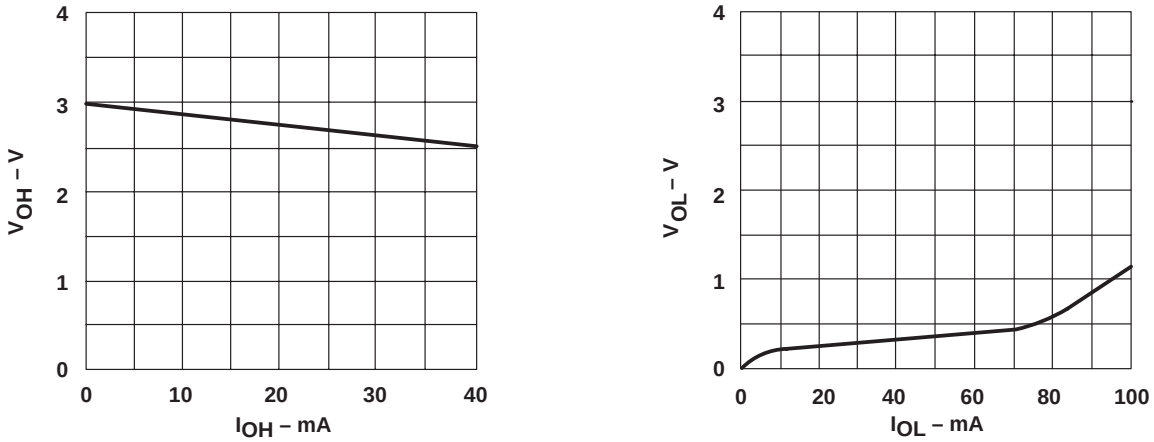


**Figure 4. Output Drive for ALVTH16244**

### 5-V Tolerance

Any 5-V TTL or CMOS device can drive the 5-V tolerant inputs of the ALVT device. A device without the 5-V tolerant capability at the inputs would require a dual-level $V_{CC}$ shifter to avoid current flow between the 5-V supply and the 3-V supply. The devices in the TI portfolio that a designer can use to perform the level shifting include the ALVC164245, LVC4245A, LVCC4245, and LVCC3245.

The 5-V-tolerant outputs help establish a connection between the device and any 5-V TTL bus. A non-5-V-tolerant output would require a dual $V_{CC}$ level shifter to drive the output.

The 5-V tolerance at the inputs is implemented by not including a diode to $V_{CC}$ in the input circuitry, making the inputs 5-V tolerant. The output 5-V tolerance is achieved by including a blocking diode between the backgate and the source to block the parasitic diode current as shown in Figure 5. P1 and D2 clamp the gate and backgate to the output after the output rises over $V_{CC}$, preventing turnon of the output PMOS.

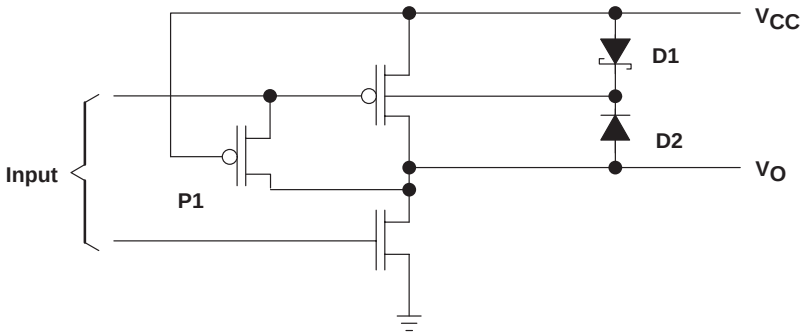


**Figure 5. 5-V-Tolerant Output**

### Auto3-State

The auto3-state feature in the ALVT is demonstrated in Figure 6. This feature is not the same as the power-up 3-state feature. Auto3-state provides short-circuit current limiting (approximately 40 mA) at approximately $V_O = V_{CC} + 0.5$ V. As the outputs are swept above $V_{CC} + 0.5$ V, the outputs are in the 3-state condition, preventing bus contention in cases where the bus is driven to a higher voltage by a competing driver. The output overvoltage protection is illustrated in Figure 6 by a simple comparator circuit that compares the output voltage to $V_{CC}$ and limits the current by turning off the PMOS transistor when the output is approximately 0.5 V greater than $V_{CC}$. This helps protect the PMOS transistor in the active-high state. The output current in this case is represented by $I_{ex}$ and is specified in the data sheet at 125 µA, for $V_O = 5.5$.

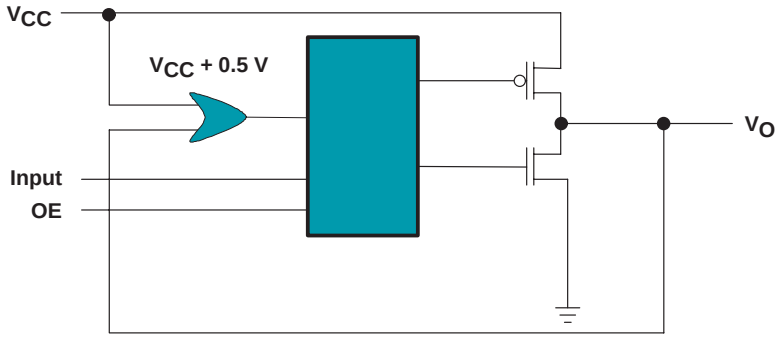


**Figure 6. Auto3-State Circuitry**

Figure 7 shows the V-I curve at the outputs for the condition where the output is pulled above $V_{CC}$ (3.0 V) for the ALVTH16244. If $V_O$ is greater than $V_{CC}$, the current sinks into the output PMOS transistor until the comparator senses the difference in the output voltage and shuts off the transistor. The maximum current sinking into the PMOS transistor is 45 mA.

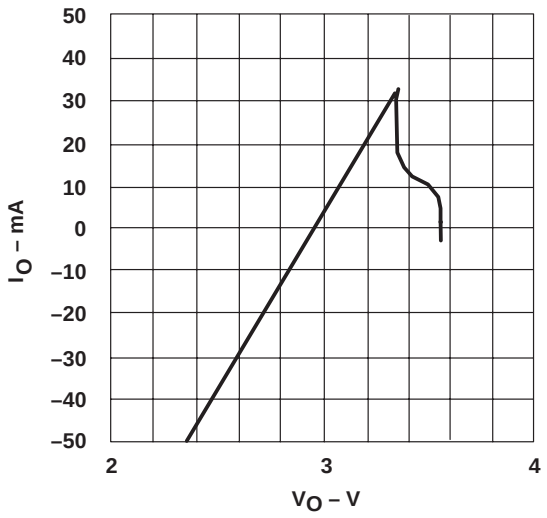


**Figure 7. Auto3-State Implementation for ALVTH16244**

### Bus Hold

All devices in the ALVT family have bus-hold circuits. The bus-hold circuit is an internal feedback circuit that keeps the unused input pins from floating and eliminates the need for external pullup resistors. This feature is implemented in ALVT devices by using input transistors that act either as pullups or pulldowns (see Figure 8), allowing the inputs of the CMOS transistors to be left open. The circuit also shows a Schottky diode between the input and the PMOS transistor that blocks the input current if the device is connected to a 5-V signal when the device is powered off. Figure 9 shows the bus-hold characteristic for the ALVTH16244.

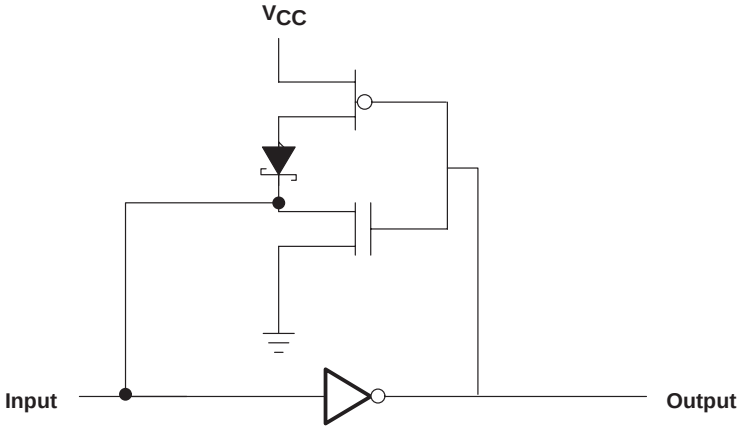


**Figure 8. Bus-Hold Circuitry**

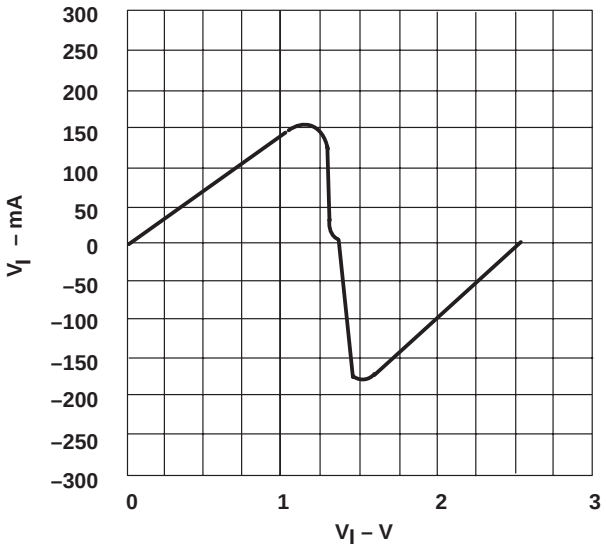


**Figure 9. Bus-Hold Current With $V_{CC}$ = 3 V and $V_I$ Sweep From 0 V to 3 V**

### Partial Power Down, Hot Insertion, and Live Insertion

A device that is hot-insertable prevents driver conflicts as the card is being inserted or removed from a loaded backplane. Both $I_{off}$ and power-up 3-state (PU3S) circuitry are needed for hot insertion. The ALVT family has these features, which are used for both partial-power-down and hot-insertion applications. The power-up 3-state feature, as shown by the power-up control circuit in Figure 10, maintains the output in a 3-state condition when $V_{CC}$ is lower than 1.2 V. The high-impedance state at the output prevents any current sinking into the device to prevent damage in hot-insertion applications. The internal circuitry consists of a transistor that turns off if $V_{CC}$ is lower than 1.2 V. This keeps the output at 3-state while $V_{CC}$ is lower than 1.2 V. This is important for applications where the device is connected to an operating backplane, which results in a device being powered up from 0 to $V_{CC}$. After $V_{CC}$ passes 1.2 V, the transistor turns on, which, in combination with the external OE signal, activates the device.

The ALVT devices feature the $I_{off}$ specification and include the PU3S circuitry. For a glitch-free live insertion to the data bus an additional precaution must be taken. Typically, board I/Os must be precharged. This can be implemented internally or externally to the bus-interface device. A power-sequencing scheme with the ground, precharge circuitry ($V_{CC}$Bias), $V_{CC}$ and I/O must be followed to facilitate live insertion. ALVT devices do not include this feature with internal precharging circuitry. If live insertion is required, external precharging circuitry is required.

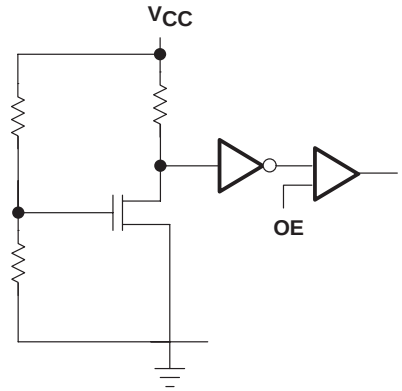


**Figure 10. Power-Up Control Circuit**

Figure 11 shows the output of the ALVTH16244 as $V_{CC}$ is powered up or powered down between 0 and 3.6 V. In this example, the output has a 3.0-V force when it is in 3-state and remains in 3-state well outside the data-sheet specification of $V_{CC} \leq 1.2$ V. The power-up 3-state currents are specified as $I_{OZPU}$ and $I_{OZPD}$ in the data sheet.

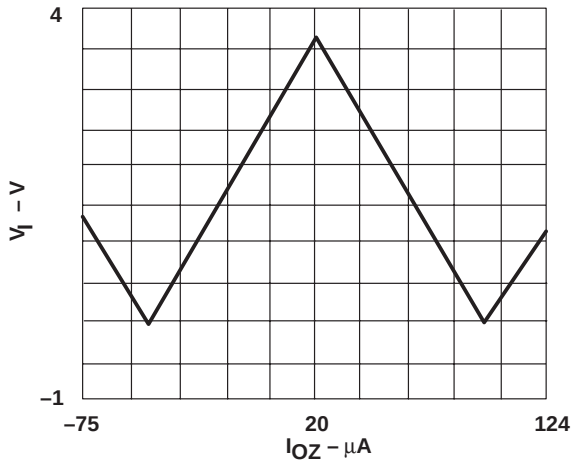


**Figure 11. Power-Up/Power-Down Test With $V_O$ = High, ALVTH16244**

### Interfacing Between 3 V and 5 V

With the trend toward lower voltages, it is extremely important for inputs and outputs to be compatible with mixed-mode operations. As lower-voltage ASICs, processors, and memories come into existence, it becomes important to operate in these mixed-mode voltage applications. In today's market, there is a mix of both 5-V and 3-V systems, with subsequent migration to 2.5 V and, eventually to 1.8 V. The 3-V I/O pins must tolerate both 3 V and 5 V at the inputs and the outputs. Table 2 summarizes the mixed-mode operating capability of the ALVT family.

**Table 2. ALVT Mixed-Mode Operation**

| FEATURES | ALVT |
|---|---|
| Drive 5-V TTL levels | Yes |
| Drive 5-V CMOS levels | No |
| 5 V on inputs/control pins | Yes |
| 5 V on outputs | Yes (when in 3-state and active high) |

Inputs of ALVT devices are designed without the diode, making them 5-V tolerant. The Schottky diode at the outputs prevents the current from flowing from the output transistor. The auto3-state feature, explained previously, also protects the internal circuit of the device, making the outputs 5-V tolerant.

### Signal Integrity

A designer is concerned about the performance of the device when the outputs are switching. The most common method of assessing this behavior is by observing the impact on one unswitched signal output, when multiple outputs are switching.

### Simultaneous Switching and Ground Bounce

Simultaneous switching is a method used to measure the magnitude of noise a device produces while switching. The method of measuring simultaneous-switching noise (ground bounce) consists of holding one output low and switching all other outputs from the high state to the low state. Mutual inductance causes transient current to flow through the package and into the output pin that is being held low. This results in a rise in voltage and the output begins to ring. The peak of this ringing is called $V_{OLP}$ (output low peak voltage) and is the most common and critical measure of ground bounce due to the relatively small noise margin between a valid output low state and beginning of the threshold region of 0.8 V. $V_{OLV}$ (output low valley voltage) is the lowest point that the output that is being held low reaches. ALVT devices are optimized for ground-bounce performance, and can be measured with respect to GND or $V_{CC}$. When measuring with respect to GND, $V_{OLP}$ is the impact of one quiet, logic-low output when all other outputs are switched from high to low.

In a similar fashion, two other measurements of simultaneous switching exist. In this scenario, a single output is held high and all other outputs are switched from the low state to the high state. Mutual inductance occurs and results in the output voltage dipping from its logic high state and ringing. The valley of this phenomenon is called output high valley voltage ($V_{OHV}$) and the peak is called output high peak voltage ($V_{OHP}$).

Simultaneous switching performance is extremely important. If the value of $V_{OLP}$ goes above 0.8 V, the threshold region is entered and the device could switch from the low state to the high state. Conversely, if the value of $V_{OHV}$ drops below 2 V, the device could switch from the high state to the low state. For this reason, simultaneous-switching values always are monitored closely when designing, testing, and implementing devices.

Figures 12 and 13 show the $V_{OHV}$ and $V_{OLP}$ levels for the ALVTH16244 for high-to-low and low-to-high transitions.

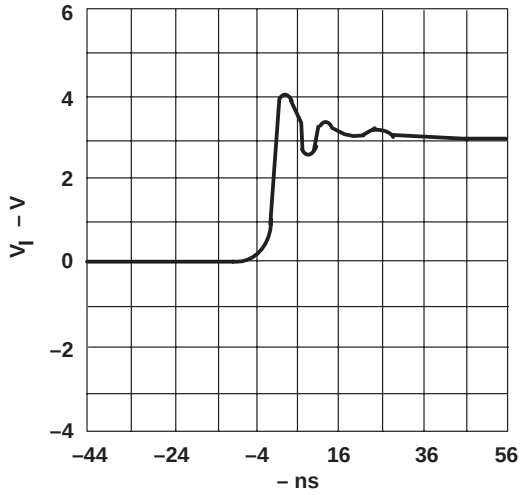


**Figure 12. $V_{OHV}$**

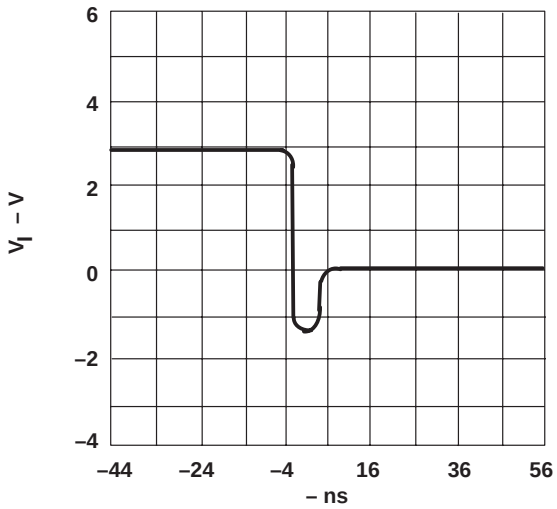


**Figure 13. $V_{OLP}$**

The technique used to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. This reduces the mutual inductances between the signals.

### Propagation Delay, Load, and Number of Outputs Switching

The ALVT family has been characterized for faster speeds and has a typical propagation-delay time of 2.5 ns. Propagation delay is an important parameter because it is a direct indication of the speed of the device and can be a primary parameter in determining whether or not a given logic family is suitable for a particular application.

The standard load for testing the ALVT family is 50 pF and 500 ohms. In most applications in which the ALVT families can be used, the load is 50 pF, but they are also commonly used in systems that require up to 100-pF loads. Figure 14 shows propagation-delay time versus load capacitance for the TI ALVTH16244. As the load increases, an increase in propagation delay occurs.

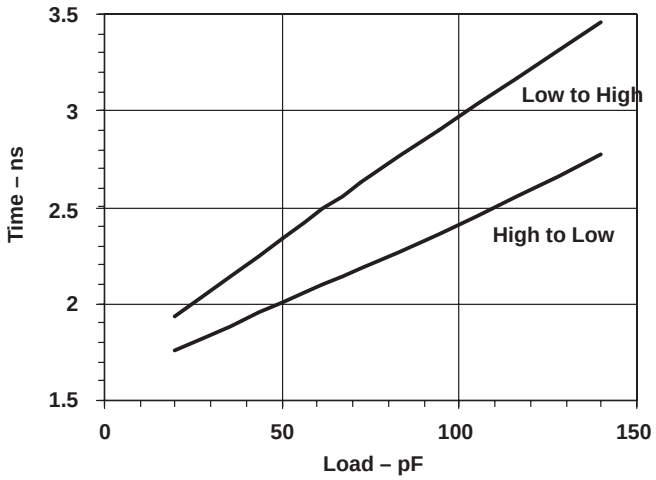


**Figure 14. $t_{pd}$ vs $C_L$**

Figure 15 shows the results of single outputs switching, 4 outputs switching, 8 outputs switching, and 16 outputs switching at one specific load. Additionally, a distinction is made between whether the output is switching from a low-to-high state or from a high-to-low state.

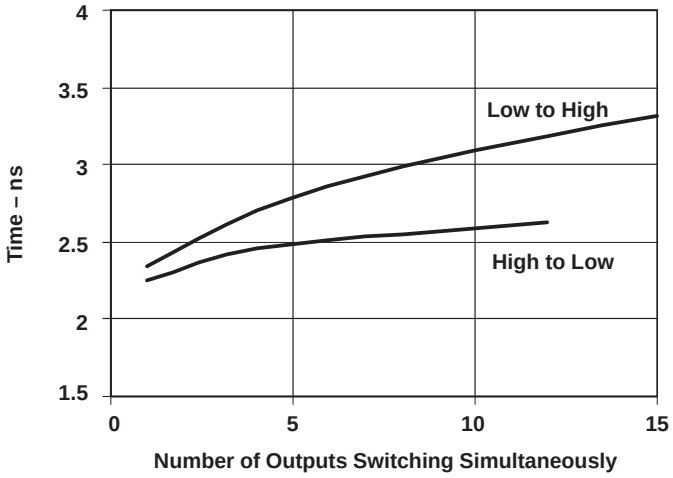


**Figure 15. $t_{pd}$ vs Simultaneous Switching, $V_{CC}$ = 3.3 V and 50 pF**

## Supply Current Versus Frequency

The supply current ($I_{CC}$) is critical because it is an indication of the amount of power consumed by the device. A small value for $I_{CC}$ is desirable because $I_{CC}$ is a factor in the dynamic power dissipated by the device. Reducing the amount of power consumed yields many benefits, including less heat generated, which eventually increases the reliability of a system. This could also enhance the performance because lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise.

Figures 16 and 17 illustrate the relationship of $I_{CC}$ to frequency for the TI ALVTH16244. The data were taken at 25°C for single-output and all-outputs switching.

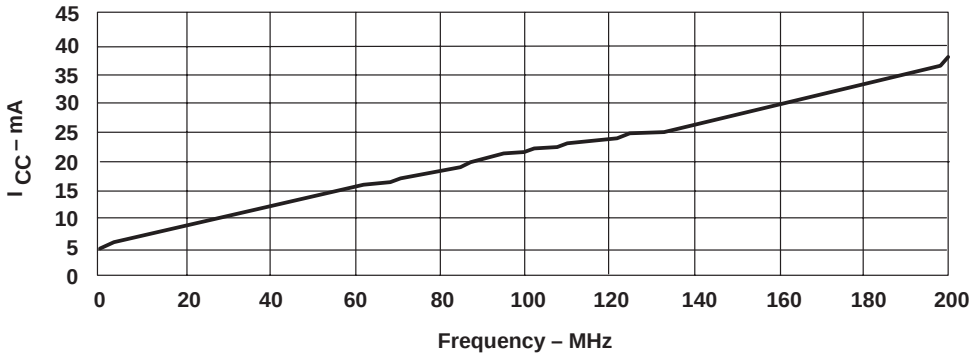


**Figure 16. $I_{CC}$ vs Frequency (Single-Output Switching Enabled)**

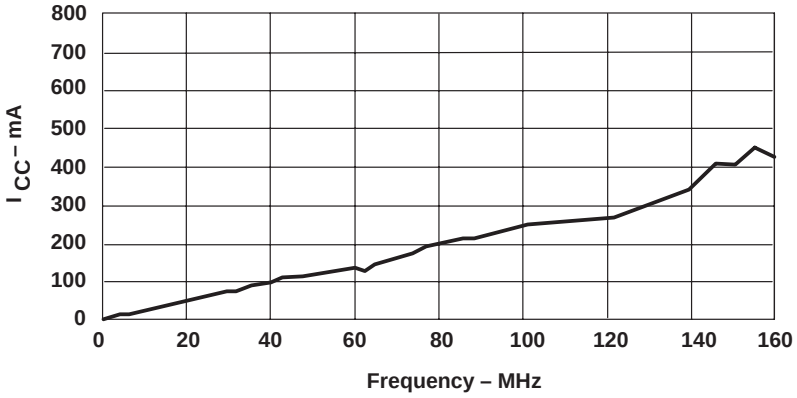


**Figure 17. $I_{CC}$ vs Frequency (16 Outputs Switching)**

## Output-to-Output Skew

This feature is important in an application in which clock distribution and high-speed data buffering are an issue, mostly found in backplane applications. Output-to-output skew indicates the variance in the output switching times. If an application has a requirement for a minimum amount of skew, this is probably the parameter with which the engineer is concerned. When conducting this test, the inputs were tied together and switched and the difference in the outputs was subsequently computed; for comparison purposes, competitors have labeled this value $t_{sko}$. For the ALVTH16244, observed $t_{sko}$ is ≤ 250 ps (typical).

## Packaging Availability and Nomenclature

The ALVT family is available in the SSOP (DL), TSSOP (DGG), and the TVSOP (DGV) packages. For order entry, the device part number is limited to 18 alphanumeric characters; therefore, the package designation for DGG (TSSOP) is shortened to G, and DGV (TVSOP) is shortened to V, as shown in the data sheets.

## Summary

The ALVT family is optimized for high-performance applications. With the high-drive capability and the low propagation delays, along with low power dissipation and good signal integrity, this family is useful for high-end telecom and networking end equipments. The advanced features, such as auto3-state and the 5-V-tolerant I/Os, make the family compatible with mixed-mode environments.

## Acknowledgment

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