Designing With TI Ultra-Low-Voltage CMOS (AUC) Octals and Widebus™ Devices

Sagir Hasnain, Gene Hinterscher, and Will Hutchinson *Standard Linear & Logic*

ABSTRACT

System designers are continuously seeking ways to improve signal integrity, increase speed, and reduce power consumption in personal computers, telecommunication equipment, and other electronic systems. The Texas Instruments (TI) next-generation Advanced Ultra-low-voltage CMOS (AUC) octals and Widebus™ devices are designed to achieve these goals. These devices are designed for a 0.8-V to 2.7-V power supply and are optimized for 1.8-V operation. With the help of a unique output structure, the AUC logic devices achieve excellent signal integrity, while maintaining the highest possible speed in the industry.

Contents

List of Figures

List of Tables

1 Introduction

The Advanced Ultra-low-voltage CMOS (AUC) devices from Texas Instruments (TI) are the industry's first logic family that is optimized at 1.8-V V_{CC}, but is operational from 0.8 V to 2.7 V, with a tolerance of 3.6 V. This sub-1-V family operates at low power and high speed, while maintaining overall system signal integrity for use in telecommunications equipment, high-performance workstations, and portable consumer electronics. The AUC offers I_{off}, which protects the device while supporting partial-power-down applications. Selected AUC devices offer the bus-hold feature, which eliminates the need for an external pullup or pulldown resistor when there is no active driver on the bus.

This application report discusses AUC Widebus™ and octal device features, characteristics, and applications. The use of AUC logic in this application report refers to the AUC Widebus and octal devices. Please refer to the application report, *Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027, for information specific to the AUC Little Logic devices.

2 AUC Logic Features

The AUC logic devices are designed for high-speed applications with optimum signal integrity. With a unique output structure (see section 2.1), the AUC device switches very fast and still maintains very low transition noise. Among the noted features, the characteristic output structure, level-translation support capability, bus hold, and partial-power-down support features of the AUC devices facilitate their use in the target applications.

2.1 Novel Output Structure

The AUC Widebus and octal devices feature a unique output driver that minimizes the switching noise in high-speed applications. The output driver achieves this by using three impedance phases during the output transition.

To achieve the three impedance phases, the AUC output employs a three-branch, p-channel, upper-output and a three-branch, n-channel, lower-output structure (see Figure 1). The first branch, the ac branch (ACB), which uses a diode in the output structure, provides the high dynamic current required to drive through the threshold. This initial high drive provides the quick transition to the desired logic level and ensures that system timing is preserved. The second branch, the transmission line branch (TLB), which contains a series resistor, provides optimized impedance matching into the transmission line to help minimize ringing and to optimize signal integrity. The third branch, the dc branch (DCB), provides the additional dc current drive for applications requiring more than 4-mA output drive current at 1.8-V V_{CC}.

For a detailed description of the AUC output driver, please refer to the application report, *Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.

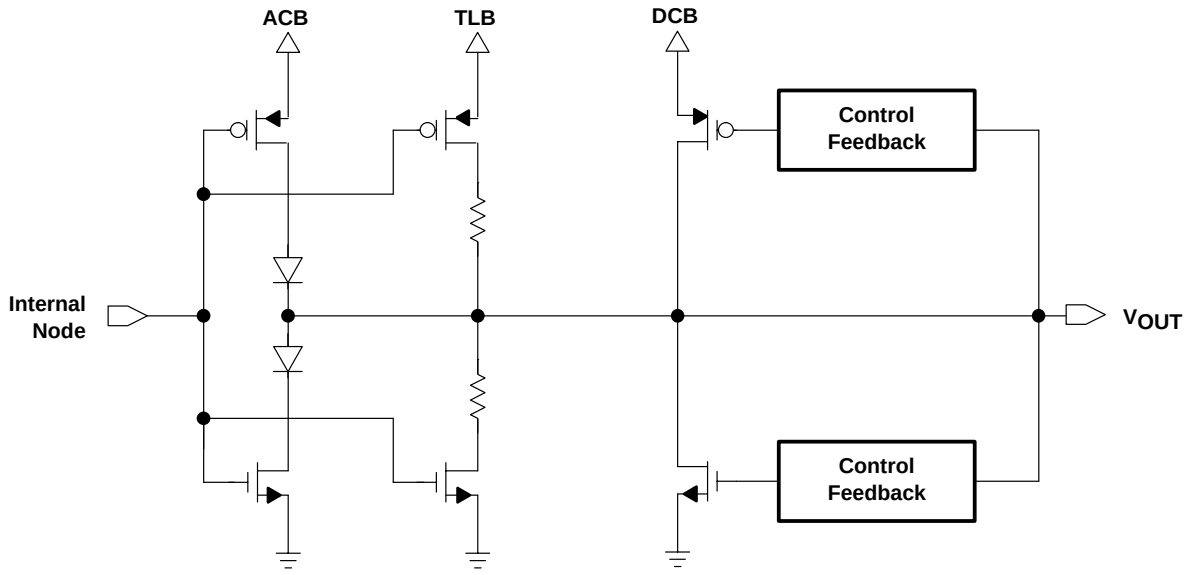


Figure 1. AUC Output Structure

2.2 Overvoltage Tolerance

The AUC logic family can handle up to a 3.6-V signal at the input, output, or I/O port with the operating V_{CC} range from 0.8 V to 2.7 V. The AUC output, or I/O port, can handle a signal with a magnitude greater than the V_{CC} when the output buffer of that port is in the high-impedance state. This overvoltage tolerance allows the AUC logic to interface with 3.3-V logic and leads to an easy migration path from 3.3-V logic to 2.5-V, or lower, voltage nodes.

NOTE: In the absolute maximum ratings and recommended operating conditions tables of the AUC data sheet, the maximum overvoltage specification is 3.6 V. In practice, the AUC safely can handle a 3.6-V dc level at the input, output, and I/O ports, while the output buffer is in the high-impedance state.

2.3 Power-Off Support

Rapid development of hand-held consumer electronics increases the demand for low power consumption. To achieve low-power goals, the off-state leakage current (I_{off}) feature has been added to the AUC device family. The I_{off} feature limits the current into or out of the device when the device V_{CC} = 0 V (see Figure 2). The AUC device can handle valid logic signals at both the input and the output ports when V_{CC} = 0. This feature is particularly helpful for partial-power-down systems.

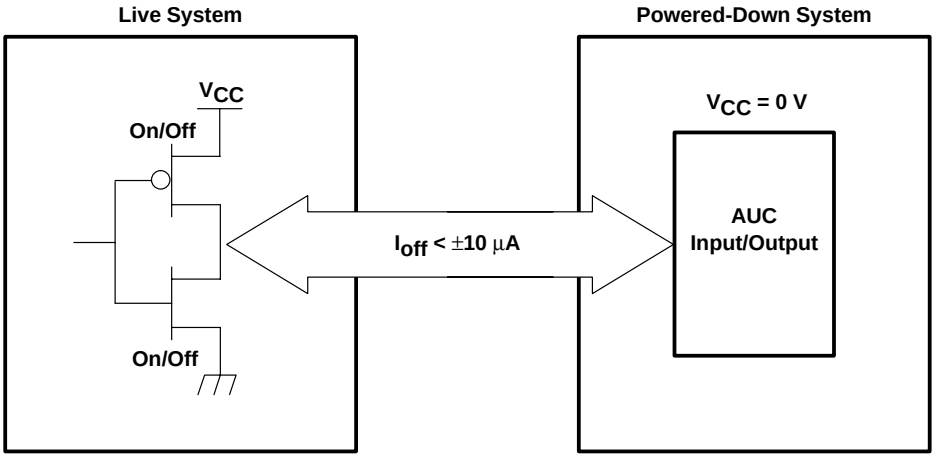


Figure 2. Simplified Partial-Power-Down System With AUC Logic

The output buffers of the AUC devices are designed with a blocking diode in the reversed-current path to V_{CC}. The input buffer, without the bus-hold circuit, does not provide any current path from the input to the V_{CC} rail. The bus-hold input has a blocking diode in the reverse-current path to V_{CC}. With these configurations, the maximum leakage current into or out of the input or output transistors, when forcing the input or output to 3.3 V and V_{CC} = 0 V, is negligible. This I_{off} is small enough to allow the device to remain electrically connected to a bus during partial-power-down conditions without loading the remaining live circuits. This feature also allows the use of this family in a mixed-voltage environment.

2.4 Bus-Hold Feature

The totem-pole structure of the CMOS input (see Figure 3c) requires that input voltage be close to GND or V_{CC} to reduce the I_{CC} current through the device. The bus-hold circuit at the CMOS input (see Figure 3b) helps to solve the problem of floating inputs and eliminates the need for pullup and pulldown resistors. The basic construction of a bus-hold circuit includes a weak inverter whose output is connected to the CMOS input (see Figure 3a). Selected AUC octals and Widebus devices are offered with the bus-hold option. The protection diode at the bus-hold circuit helps to maintain the overvoltage tolerance characteristics and the I_{off} specifications of the AUC inputs.

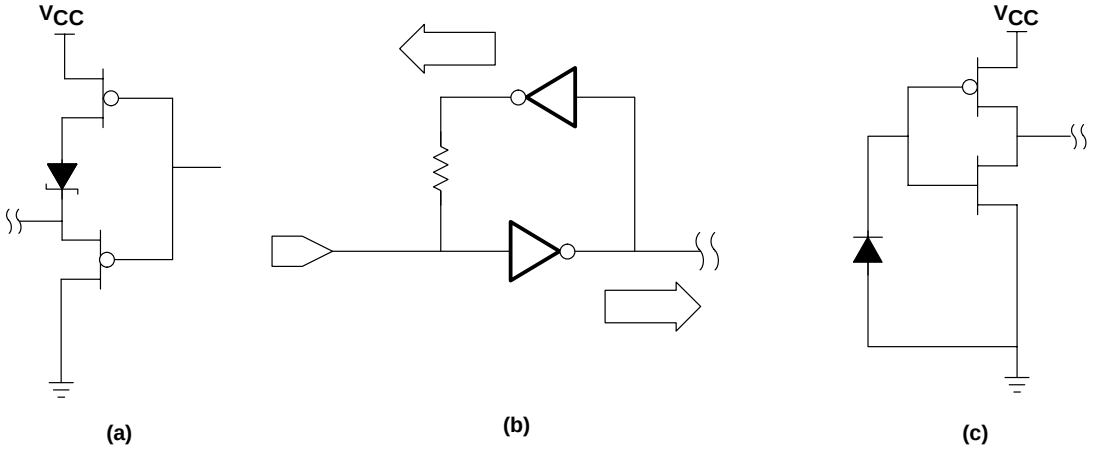


Figure 3. AUCH Input With Bus-Hold Circuit

3 AUC Logic-Device Characteristics

3.1 Input Characteristics

The input capacitance of logic devices can influence system performance in the following two ways:

- In terms of loading, CMOS inputs can be represented by the C_i or the C_{io} parameter, with some limitations. A device with low input capacitance allows a given driver to drive a large number of inputs.
- For a specific driver, if the load capacitance increases, the output slew rate decreases. The slower transitions at the CMOS input may increase the system power consumption because the signal stays in the high-current region longer (see Figure 5).

The AUC logic maintains a low input capacitance compared to other high-performance CMOS logic devices. (see Table 1)

Table 1. Input and Output Capacitance of AUC Octals and Widebus™ Devices

DEVICE	C_i (pF)		C_o or C_{io} (pF)	
	TYP	MAX	TYP	MAX
SN74AUC245	2.5	3	7.5	8
SN74AUCH245	2.5	3	8	8.5
SN74AUC16245	3	4	7	
SN74AUC16501	3.5	4.5	6	7.5
SN74AUC16240	3	4	5.5	6
SN74AUC16244	3.5	4.5	6	7.5
SN74AUCH16244	3	4.5	4	7
SN74AUC16374	3	4	5	

Figure 4 shows the input characteristics of an AUC device with the bus-hold feature. The data in Figure 4 has been taken from the SPICE simulation of the AUCH16244. In Figure 4, the typical data was taken at nominal process and temperature with V_{CC} = 1.8 V. The minimum and maximum values are the corners of process, voltage, and temperature at the 1.8-V V_{CC} node. The input voltage range from 0 V to 3.3 V is highlighted to show the bus-hold characteristics. For an input without bus hold (for example, AUC16244), the entire highlighted input-voltage range maintains a leakage current less than the data-sheet-specified I_I. The flat region of the V_I–I_I curve (V_{CC} to 3.6 V) indicates that input voltage can be raised above V_{CC} without increasing the leakage current.

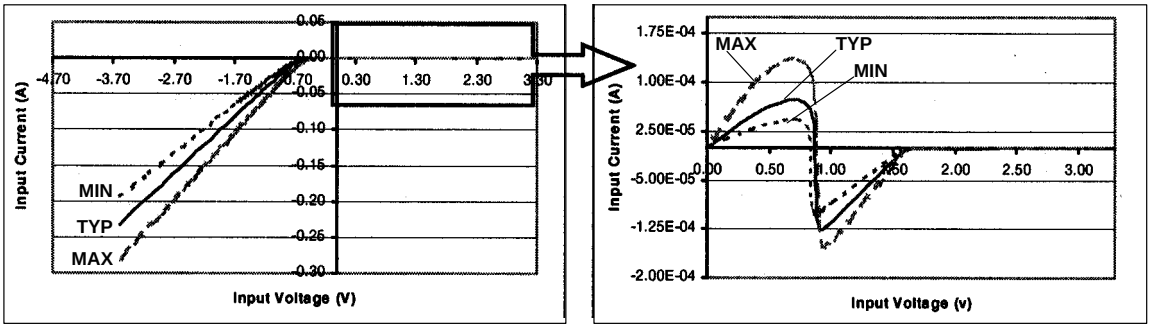


Figure 4. AUCH16244 Input V_I-I_I Characteristics

NOTE: In many applications, it is common to observe undershoot due to transmission-line mismatch. One way to estimate whether this undershoot is unsafe is to look at the V_I-I_I curve to see if the undershoot draws the transient input current above the data-sheet absolute-maximum ratings. However, to ensure device reliability, the best practice is to reduce the undershoot in the application. The V_I-I_I curve for the TI logic device can be found in the corresponding IBIS file.

Figure 5 shows the input voltage vs I_{CC} current of the AUC family. The data was taken from laboratory tests, with the nominal material of AUC16245 and AUC16244 at 1.8-V V_{CC} and T_A = 25°C. The input voltage vs I_{CC} curve of a CMOS input indicates the amount of excess supply current drawn if a CMOS input floats.

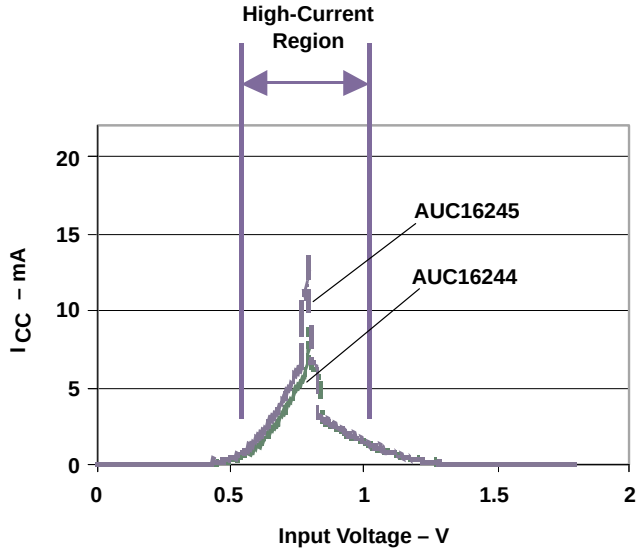


Figure 5. V_I vs I_{CC} Characteristics of AUC Devices

3.2 Electrical Characteristics

3.2.1 AC Performance: Faster Speed

The AUC family has been optimized for speed. With the help of special output circuitry, an AUC device can operate faster, while maintaining very good signal integrity. Figure 6 shows the performance comparison and the low-voltage migration path for different CMOS logic families offered by TI.

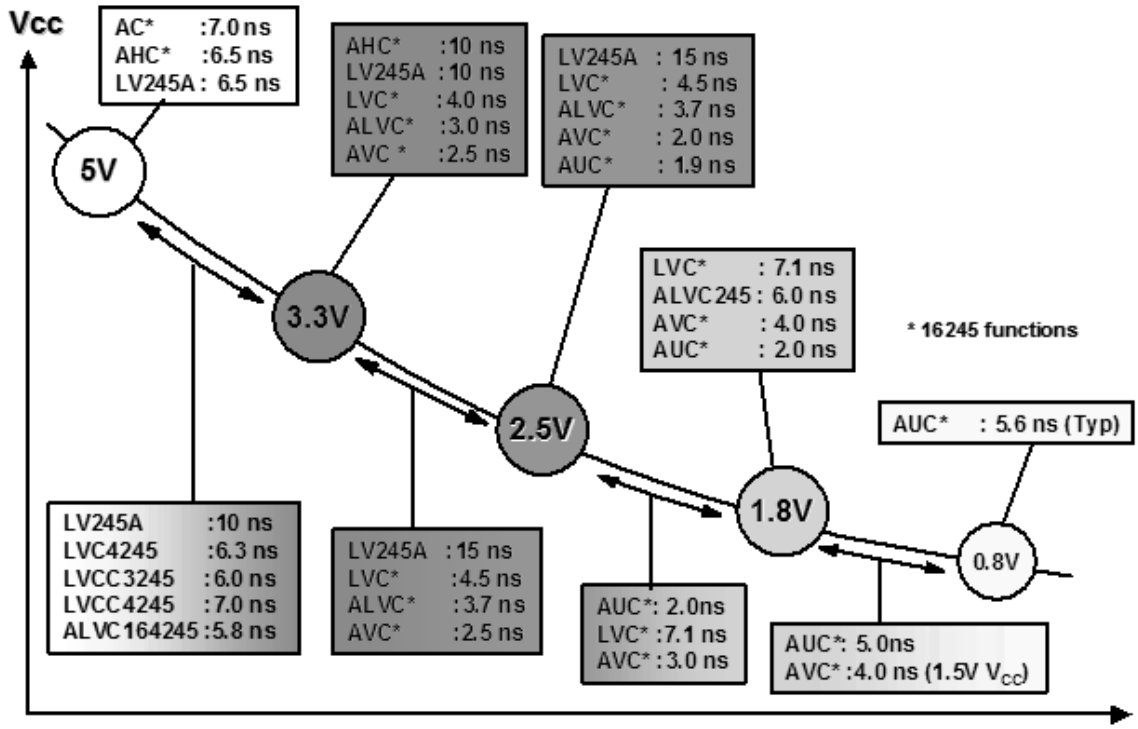


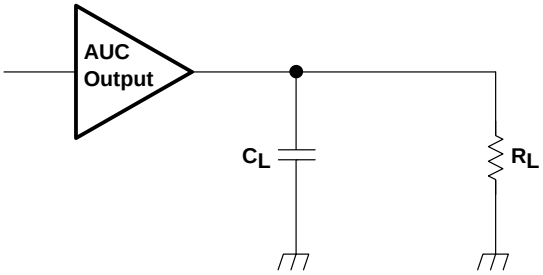
Figure 6. AUC vs Different CMOS Logic Families TI Offers as a Migration Path

In most electronic-system applications, it is important for the IC drivers to provide a balanced high and low drive during the ac transition. This ensures balanced output edge rates and improved signal integrity. Also, balanced high and low drive ensures that the difference between the low-to-high transition time (t_{PLH}) and the high-to-low transition time (t_{PHL}) is minimized. In general, as the supply voltage decreases, the p-channel transistor becomes weaker at a faster rate than the n-channel transistor due to their respective positive and negative carrier-mobility-degradation characteristics. For devices with active p-channel pullups, this causes t_{PLH} to increase at a faster rate than t_{PHL}; consequently, the $|t_{PLH} – t_{PHL}|$ increases, respectively. The three-branch AUC output minimizes this effect across V_{CC} by distributing the high drive across the r_{on} of the transistor with that of the resistor, i.e., the resistor in the TLB branch (see Figure 1). The resistance of the resistor does not vary with the supply voltage, thus reducing the effective variation in r_{on} of the high and low drives.

Table 2 shows the propagation delay for different AUC logic devices operating at different voltage nodes. These results are the output of laboratory tests using the standard load specifications in the parameter measurement information of the data sheet (see Figure 7).

Table 2. Timing Characteristics of AUC Logic Devices

DEVICE	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ±0.1 V		V_{CC} = 1.5 V ±0.1 V		V_{CC} = 1.8 V ±0.15 V			V_{CC} = 2.5 V ±0.2 V	
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX
SN74AUC245	A or B	B or A	5	1	3.2	0.6	2	0.6	1.3	2.2	0.5	1.8
SN74AUC16245	A or B	B or A	5.6	0.5	3.1	0.5	2	0.5	1.5	2	0.4	1.9
SN74AUC16501	A or B	B or A	8.5	0.9	4	1	2.8	0.3	2	2.8	0.1	2.3
SN74AUC16240	A	Y	5.8	0.9	2.6	0.7	1.8	0.6	1.4	2	0.4	1.6
SN74AUC16244	A	Y	5.4	0.8	2.8	0.6	1.9	0.7	1.3	1.8	0.5	1.8
SN74AUC16374	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2



t_{pd} TEST LOAD		
V_{CC}	C_L	R_L
0.8 V	15 pF	2 kΩ
1.2 V ± 0.1 V	15 pF	2 kΩ
1.5 V ± 0.1 V	15 pF	2 kΩ
1.8 V ± 0.15 V	30 pF	1 kΩ
2.5 V ± 0.2 V	30 pF	500 Ω

Figure 7. Test Loads for Propagation Delays at Different V_{CC} Nodes

AUC logic has been designed and optimized at V_{CC} = 1.8 V. But, it has good timing characteristics at the other V_{CC} nodes as well (see Table 2).

In an actual customer application, the load capacitance varies, depending on the number of receivers and the input characteristics of the receiver. Figures 8 and 9 show the variation of AUC propagation delays with the load capacitance at different V_{CC} nodes. The data was taken from the SPICE simulation of AUC16245 at the lumped capacitive loads, nominal process, and 25°C ambient temperature. Because the data was taken using the same reference loads, Figures 8 and 9 show a true comparison of the propagation delays at different voltage nodes.

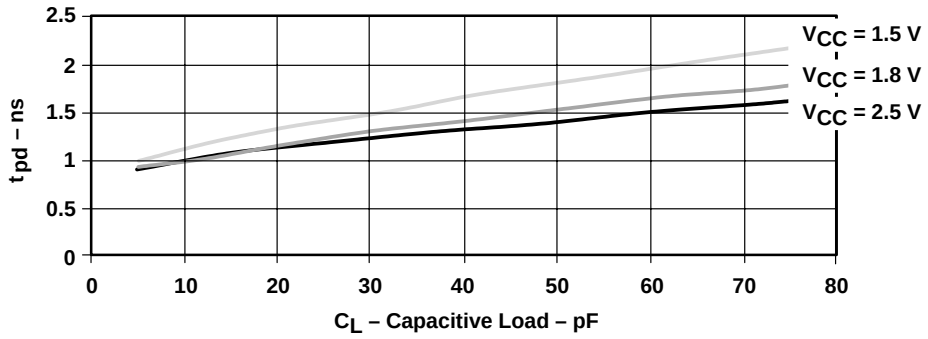


Figure 8. t_{pd} vs C_L at 2.5-V, 1.8-V, and 1.5-V V_{CC}

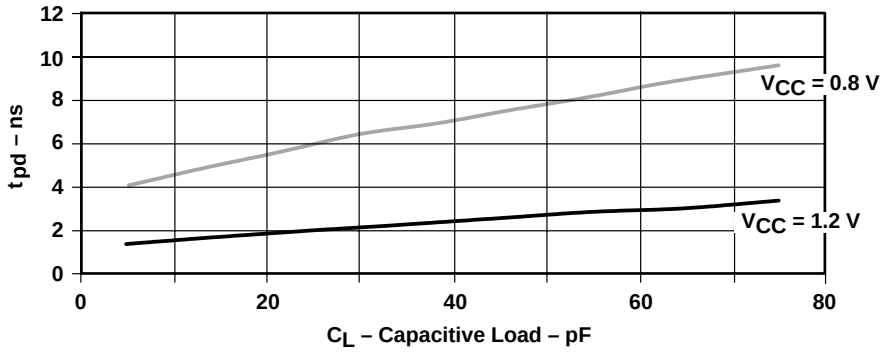


Figure 9. t_{pd} vs C_L at 1.2-V and 0.8-V V_{CC}

3.2.2 Dynamic vs DC Drive: Faster Speed, Low Transition Noise

For a typical CMOS logic device, the V_{OH}–I_{OH} and V_{OL}–I_{OL} characteristics represent the dc drive capability of the device. Because of the special output structure, the AUC V_{OH}–I_{OH} and V_{OL}–I_{OL} characteristics are unique. The V_O vs I_O performance demonstrates the dc drive performance of the output circuit, but does not relate directly to the ac performance. The output drive uses three impedance phases during the transition (see section 2.1). Figures 10 and 11 show the typical V_O vs I_O dc drive performance and dynamic (ac) drive performance. The dynamic-drive data was taken from the SPICE simulation with all three branches of the AUC output turned on. This situation represents the initial phase of the transition when all three legs are turned on. The parallel combination of r_{on} of all three legs provides very low impedance. The I_{OH} and I_{OL} values recommended in the AUC data sheet correspond to the dc curves in Figures 10 and 11. When the AUC device switches from one logic state to another, the initial drive strength corresponds to the dynamic drive curve, as shown in Figures 10 and 11. This high drive enables faster transition to the desired logic state. As the output approaches the desired logic level, the drive capability shrinks to the dc drive level to reduce the transition noise.

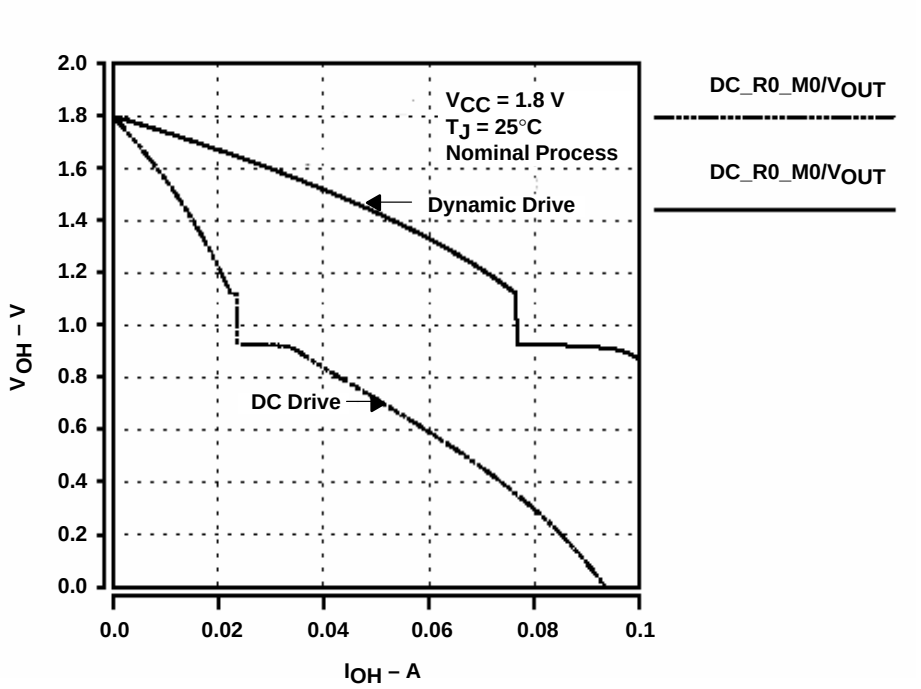


Figure 10. V_{OH} vs I_{OH}

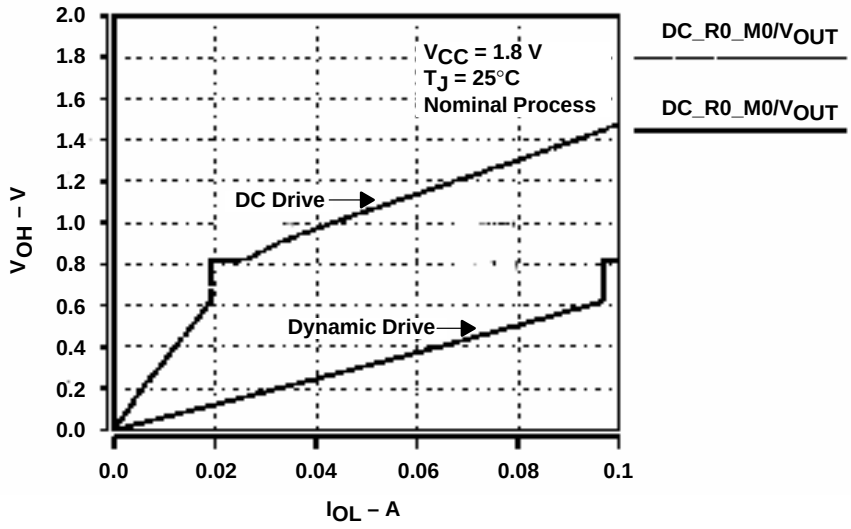


Figure 11. V_{OL} vs I_{OL}

On the V_{OH}–I_{OH} and V_{OL}–I_{OL} plots, a small step function is present outside the drive conditions of the data sheet. This step in the waveform should not cause any problems in device performance because it occurs at the point when both ACB and DCB are turned off and affects only the ac signal-integrity performance for which it is designed (see section 2.1).

3.3 Power Consumption

One of the major goals for a system designer is to reduce overall system power consumption. Table 3 shows a number of ways in which a logic device can contribute to the total system power consumption, along with solutions the AUC family offers.

Table 3. System Power-Consumption Modes

MODE OF OPERATION	DESCRIPTION OF THE OPERATING MODE	THE AUC SOLUTION
Standby mode	Device power is turned on, but it does not participate in active data transfer.	The AUC device is designed with I_{OZ}, I_{CC}, I_I specifications for this operating mode.
Power-down mode	Device power is turned off, but there are active signals at the input, output, and I/O ports.	The I_{off} specification of the AUC device allows live signals at the input, output, or I/O ports when V_{CC} is turned off.
Floating input	When the signal level is not at the V_{CC} or GND level at the CMOS input, excess through current might flow through the device (see Figure 5).	The AUC offers the bus-hold feature (see section 2.4)
Slow rise/fall rate at the output	If the output rise/fall time of a logic driver is too slow, the CMOS receiver consumes excess through current, causing an increase in system power consumption.	The AUC output delivers much of its drive at the beginning of the transition, resulting in faster transition. It takes away the excess drive at the end of the transition to reduce the transition noise.
Dynamic power	Device power consumption when driving a load at the operating frequency	The AUC family is optimized for faster speed, signal integrity, and low dynamic power, compared to the other high-performance CMOS families. Please refer to the data-sheet C_{pd} values.

Figure 12 shows the laboratory test results of supply current vs frequency for different AUC devices. For each of the devices, only one input was switching from 0 V to 1.8 V, with an input ramp rate of 1 V/ns. Note the increase in supply current as the operating frequency increases. The tests were performed at 25°C ambient temperature with V_{CC} = 1.8 V.

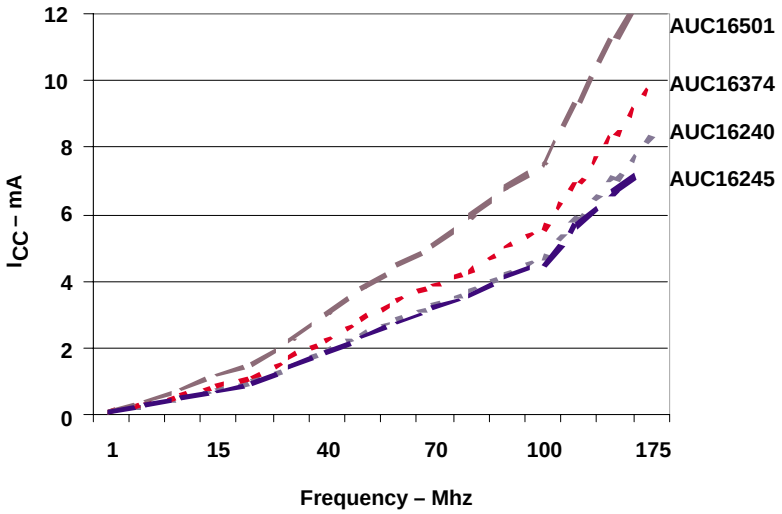


Figure 12. Typical Current Consumption of AUC Logic Devices

The bus-hold input is a weak inverter connected at the CMOS input (see section 2.4). One possible concern with bus hold is the excess drive current consumption to overdrive a bus-hold circuit. Figure 13 shows the AUC device I_{CC} current consumption between bus-hold and non-bus-hold inputs. For each device, the laboratory test was done with only one input switching from 0 V to 1.8 V, with an input ramp rate of 1 V/ns. There is no significant difference in power consumption between the two cases. This test also was performed with a 1.8-V power supply at 25°C.

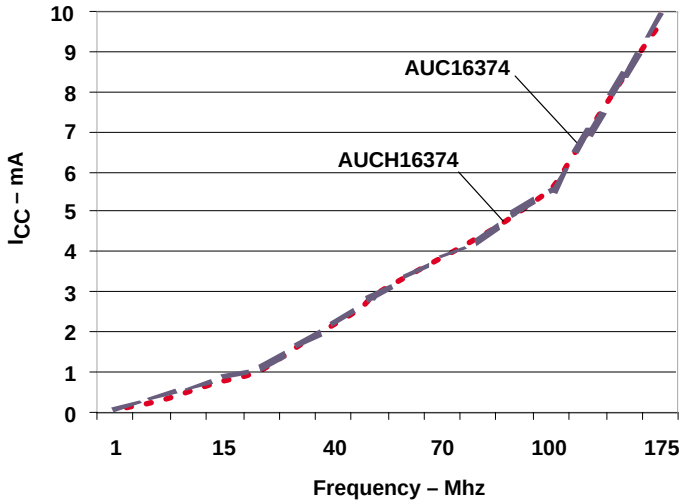


Figure 13. Power Consumption of the AUC16374 and AUCH16374

4 Design Issues and AUC Logic Solutions

4.1 Signal Integrity at Faster Speed

System designers continually pursue low-power high-speed solutions. The increase in system speed may conflict with the low-power requirement. For a given push-pull type CMOS output buffer, higher speed calls for higher drive strength, resulting in the increase of power dissipation, overshoot, and undershoot. As the system operating V_{CC} decreases, achieving the balance between speed and power consumption becomes easier. At low V_{CC}, the signal swing is smaller, resulting in lower transition time. But the low signal swing requires better signal integrity as the noise margin gets smaller with lower V_{CC}. TI AUC logic approaches the challenge of higher speed and improved signal integrity at lower V_{CC} nodes with the help of the unique output structure (see section 2.1). In addition to the requirement for better signal integrity and faster speed, system designers, especially for portable applications, need a solution that requires no external termination, i.e., damping resistors, clamping diodes, pullup resistors, etc. Additional components use valuable board space, where space also is at a premium in portable applications. AUC logic devices provide the best solution for systems with these design constraints.

Figure 14 shows a laboratory setup to compare the AUC logic with the competitor's high-end CMOS logic device. AUC16245 and the competitor's "x16245" were tested on a 10-cm, 50-Ω transmission line with a 5-pF capacitive load. The test was performed at room temperature with several samples of nominal material.

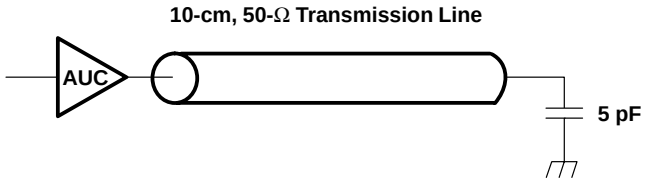


Figure 14. Laboratory Setup for Testing AUC Signal Integrity

Figures 15, 16, 17, and 18 show the laboratory data at 1.8-V V_{CC} and 2.5-V V_{CC}. The data was taken with all 16 bits of the AUC16245 and the "x16245" switching simultaneously. The AUC16245 operates at a faster speed, while maintaining good signal integrity. Note in Figures 15, 16, 17, and 18 that the AUC is optimized at 1.8 V, but performs equally well at the 2.5-V node. The dc drive specification of the AUC16245 at V_{CC} = 2.5 V is ±9 mA. The "x16245" drive at V_{CC} = 2.5 V is ±18 mA. The AUC transition rate is comparable to, or faster than, the competitor's part, which specifies double dc drive. (see section 3.2.2). The faster transition ensures that the CMOS receiver that the AUC is driving suffers less through current, resulting in overall system power savings.

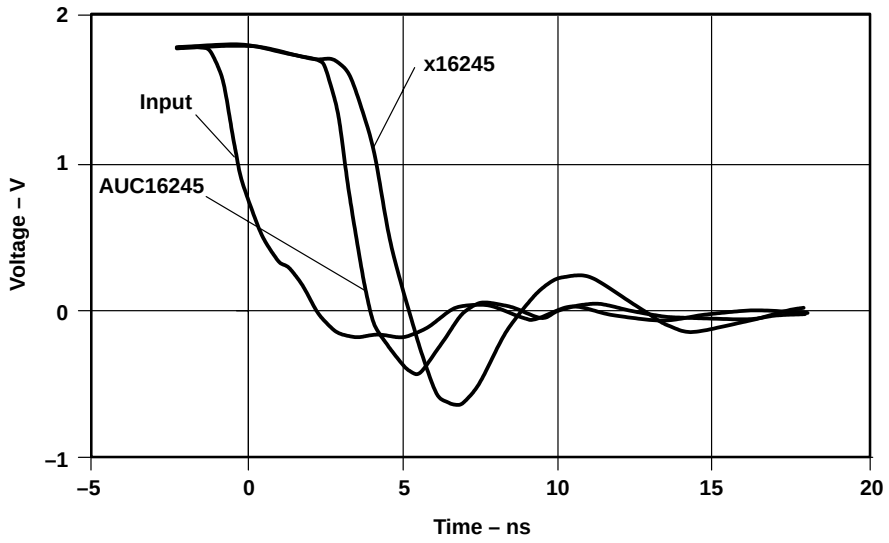


Figure 15. 1.8-V V_{CC} High-to-Low Transition, With All 16 Bits Switching

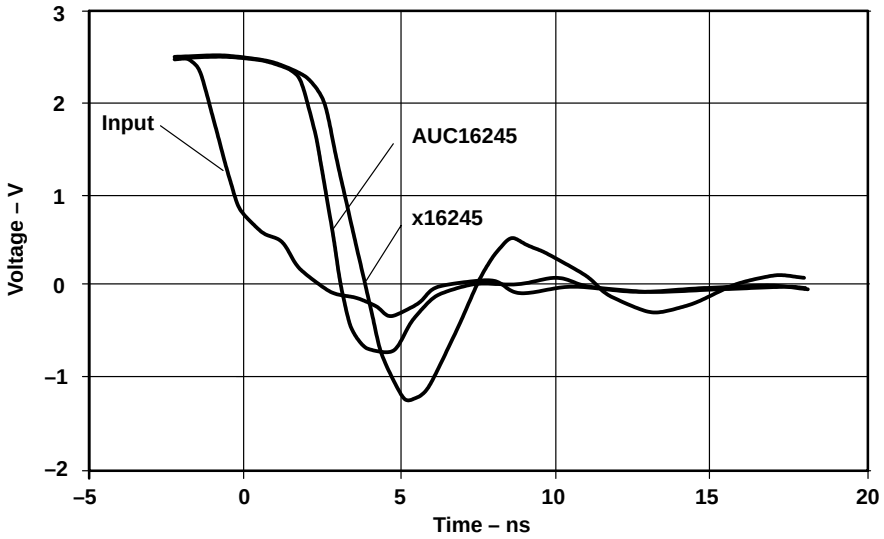


Figure 16. 2.5-V V_{CC} High-to-Low Transition, With All 16 Bits Switching

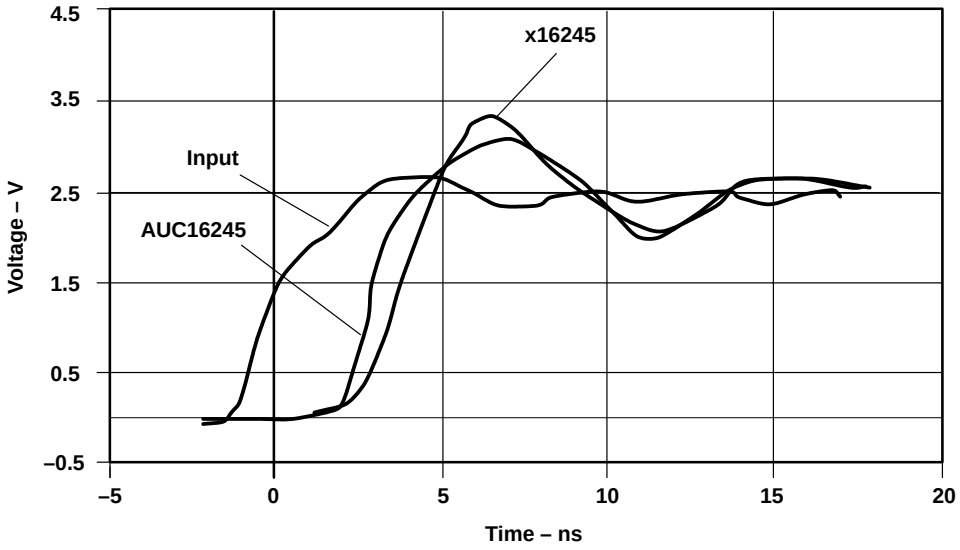


Figure 17. 2.5-V V_{CC} Low-to-High Transition, With All 16 Bits Switching

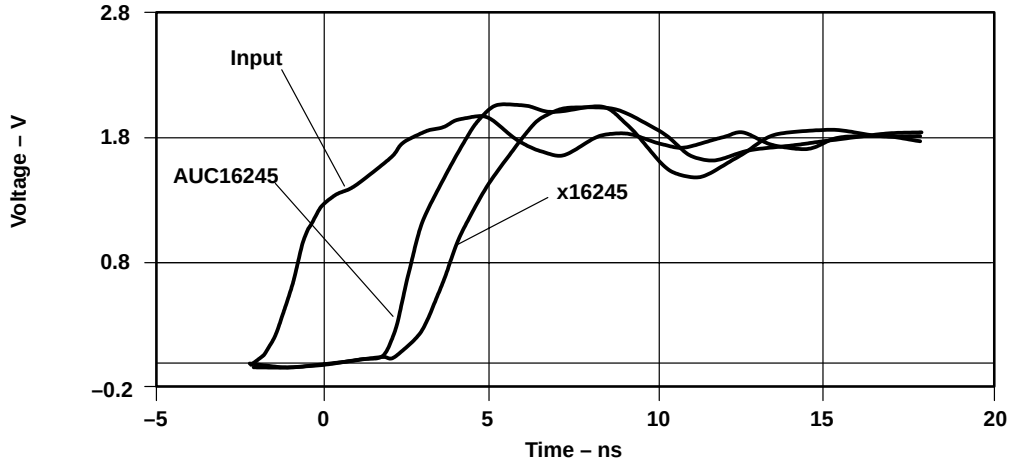


Figure 18. 1.8-V V_{CC} Low-to-High Transition, With All 16 Bits Switching

4.2 Simultaneous Switching

When multiple outputs of a logic device switch at the same time, the excessive current drawn from the power supply can produce significant noise in the power and ground rails. This noise is termed simultaneous-switching (SS) noise. Figure 19 demonstrates the mechanism of SS noise. When the input $V_I(2)$ switches between high and low logic levels, noise is injected into the V_{CC} and GND lines. The amount of noise depends on a number of factors, such as drive strength, driver edge rate, package parasitic, number of GND and V_{CC} pins, etc. The amount of noise increases as the number of switching drivers increases.

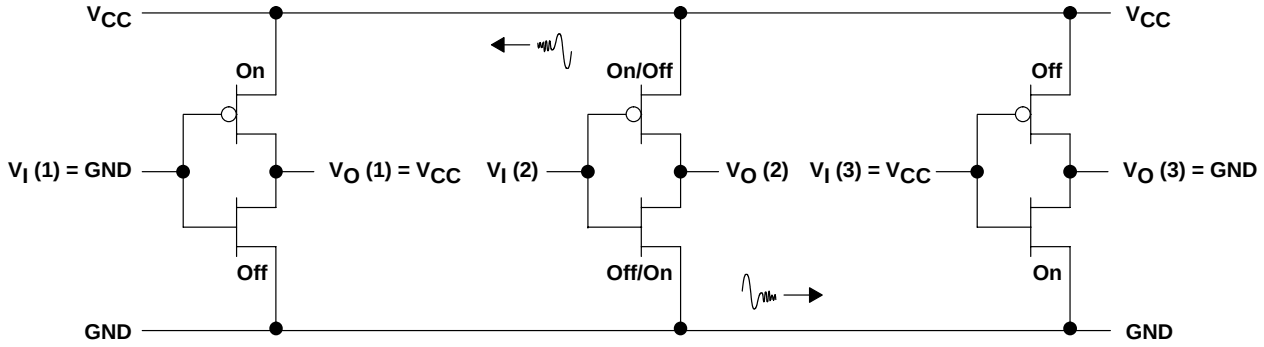


Figure 19. Noise Coupling at the V_{CC} and GND Rails

The output structure of the AUC device helps reduce simultaneous-switching noise. Because all three legs of the AUC output are turned on at the initial phase of the transition (see section 2.1), the output starts to switch with maximum drive strength. During the second phase of the transition, the ACB and the DCB are turned off, which helps reduce the noise injected at the V_{CC} and GND lines.

4.2.1 Simultaneous-Switching Noise of AUC Widebus™ Devices

Figure 20 shows the simultaneous-switching performance of AUC Widebus devices. The data was taken from a SPICE simulation of the AUC16245 with three different packages (TSSOP, TVSOP, and VFBGA). In the simulation, one of the 16 outputs was kept at dc high or low level, and the other 15 outputs were switching. Because AUC Widebus devices are offered in packages with multiple GND and V_{CC} pins, all package options show good signal-integrity performance.

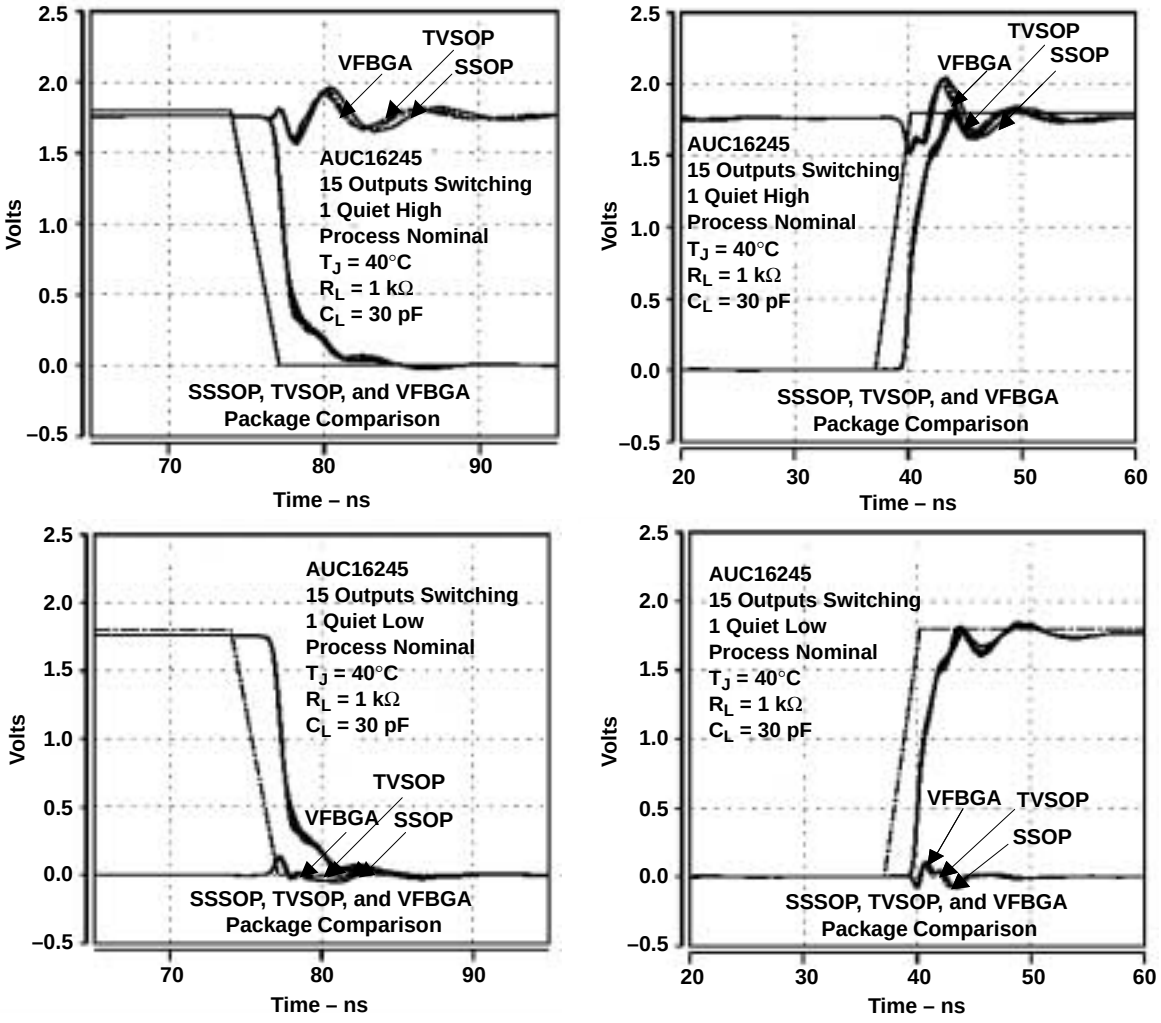


Figure 20. Simultaneous-Switching Noise of the AUC16245 in Different Packages

4.2.2 Simultaneous-Switching Noise of AUC Octals

The standard 20-pin package for octal logic devices accommodates only one V_{CC} and one GND pin. This makes the octal devices more susceptible to simultaneous-switching noise. TI offers the AUC245 in the advanced QFN package. The QFN package has several advantages over traditional SOIC, SSOP, TSSOP, and TVSOP packages. The QFN package physically is smaller, has a smaller routing area, improved thermal performance, and improved electrical parasitics, while giving customers a pinout scheme that is consistent with the four previously mentioned packages. Additionally, the absence of external leads eliminates bent-lead concerns and issues. Figure 21 shows the simultaneous-switching performance of the AUC245 with the QFN package.

NOTE: For a detailed description of the QFN package, please refer to the application report, *Quad Flatpack No-Lead Logic Packages*, literature number SCBA017.

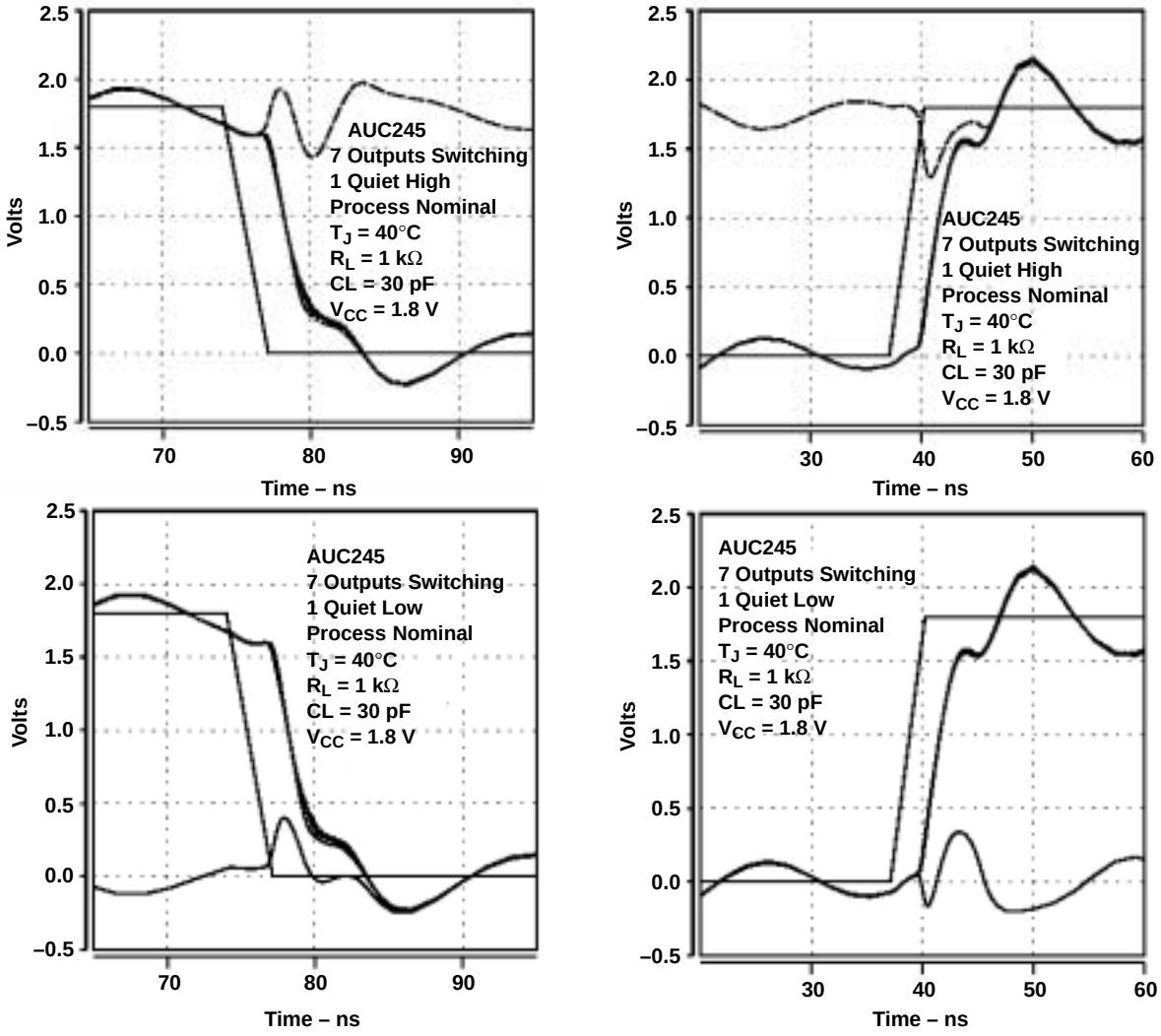


Figure 21. Simultaneous-Switching Noise of the AUC245

4.3 Voltage-Translation Support With the AUC Family

As the system designers convert core processors, ASICs, and memories of their designs to lower voltages, the AUC family presents excellent solutions for their interface needs. But, the migration toward lower-voltage nodes does not happen simultaneously in all segments of the design. The mix of different voltage nodes in the systems requires proper interfaces between the buses with incompatible logic levels. Voltage-level translation is necessary to allow interconnections, with the flexibility to provide a future migration path to lower-voltage I/O levels.

4.3.1 Bidirectional Data Transfer With Level Translation

Figure 22 shows bidirectional switching of AUC logic between 3.3-V LVTTL and 2.5-V LVCMOS interfaces. The inputs of the AUC device are 3.6-V tolerant and accept LVTTL switching levels. The outputs of the AUC device, powered at 2.5-V V_{CC} under worst-case conditions, are accepted as valid switching levels at the input of a 3.3-V LVTTL device, provided the dc output current is limited (refer to the data sheet V_{OH} specifications at I_{OH} = 100 μA). This kind of level translation with the AUC is possible, provided the following conditions are met:

- The I/O ports of the 3.3-V interface are CMOS type. The typical input leakage current for a CMOS buffer is within the 5-μA to10-μA range. The AUC V_{OH} level remains above the LVTTL V_{IH} level if the dc drive current is less than 100 μA.
- The input buffer of the 3.3-V interface does not have a bus-hold circuit. With the bus-hold circuit, the CMOS input leakage is considerably larger if the V_{OH} level of the driver is below the 3.3-V rail (see Figure 4). This excess leakage current may try to over drive the 2.5-V driver V_{OH} level to the 3.3-V rail. The presence of a bus-hold circuit at the 2.5-V AUC interface does not cause a problem.
- The increase in supply current at the 3.3-V interface, with the logic-high input signal not being at the V_{CC} rail, is not significant.

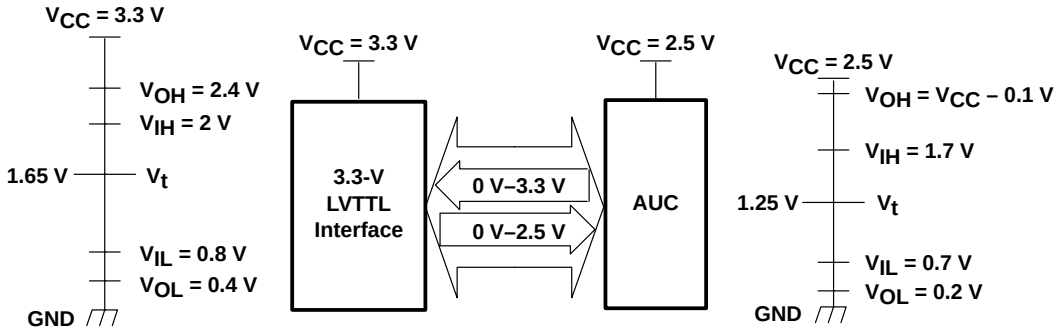


Figure 22. AUC Logic Operating at 2.5-V V_{CC} for Bidirectional Switching Between 3.3-V I/Os and 2.5-V I/Os

4.3.2 Unidirectional Data Transfer With Level Translation

Utilizing the 3.6-V-tolerance feature, the AUC driver, powered with 0.8-V, 1.2-V, 1.5-V, or 1.8-V V_{CC}, can be used to down translate from a higher voltage node to the voltage node of the supply voltage.

One potential drawback with down translation is the duty-cycle shift (see Figure 23) when the difference between input and output voltage is larger. At a lower operating V_{CC}, the input threshold voltage lowers proportionately. For example, if the operating V_{CC} = 1.2 V, the input threshold is close to 0.6 V. With very slowly rising or falling input waveforms, this lower input threshold may cause significant duty-cycle shift at the output waveforms. A faster transition at the input should eliminate this problem.

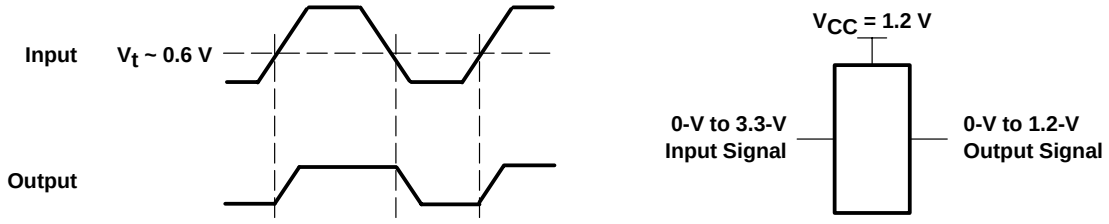


Figure 23. Unidirectional Data Transfer With CMOS Buffer

AUC logic has very low input capacitance, which helps a given driver switch at a faster transition rate. Use of the AUC buffer (instead of the AUC transceiver) is recommended in this situation. The input capacitance of the AUC buffer is ~3 pF, and the I/O capacitance of the AUC transceiver is ~6.5 pF (see Table 1).

5 Features and Benefits

Table 4 summarizes the features and benefits of AUC logic.

Table 4. Features and Benefits of AUC Logic

FEATURES	BENEFITS
Faster speed, better signal integrity	Use in very high-speed data transfer
Supports I_{off} at inputs	Use in applications that require partial-power-down modes
3.6-V I/O tolerant	Use in level-translation applications. Eases the migration to lower-voltage nodes. Enhances system safety.
Sub-1-V operable	Flexibility for future migration. Being operable at lower-voltage nodes means lower power consumption.
Bus hold	Eliminates the need for external pullup or pulldown resistors.

6 Conclusion

AUC logic devices provide the highest performance among the CMOS logic families across the industry. If a system solution requires faster speed and smoother transitions to low-voltage nodes, an AUC device is the right choice for the logic interface. The AUC family features 3.6-V I/O tolerance, bus-hold circuits, low power consumption, and partial-power-down support. The AUC product family offers a broad line of Widebus, Widebus+™, octal, single, and dual-gate solutions.

7 References

1. *Application of the Texas Instruments AUC Sub-1-V Little Logic Devices* application report, literature number SCEA027.
2. *Simultaneous-Switching Noise Analysis for Texas Instruments FIFO Products* application report, literature number SCAA008.
3. *AVC Logic Family Technology and Applications* application report, literature number SCEA006.
4. *Quad Flatpack No-Lead Logic Packages* application report, literature number SCBA017.

8 Glossary

ac	Alternating current
ACB	ac branch
AUC	Advanced ultra-low-voltage CMOS
CMOS	Complementary metal-oxide-silicon: a device technology that has balanced drive outputs and low power consumption
dc	Direct current
DCB	dc branch
EMI	Electromagnetic interference
IBIS	I/O Buffer Information Specification
I/O	Input or output
I_{OFF}	Maximum leakage current into or out of the input or output transistors when forcing the input or output to 2.7 V and V_{CC} = 0 V
I_{OH}	High-level output current. Output current with input conditions applied that, according to the product specification, establishes a high level at the output.
I_{OK}	Output clamp current. The absolute maximum current that can be sourced from an output pin when the voltage is taken below 0 V.
I_{OL}	Low-level output current. The current into an output with input conditions applied that, according to the product specification, establishes a low level at the output.
LOP	Lower output transistor
LVCMOS	Low-voltage complementary metal-oxide silicon
PDP	Power-delay product
r_{on}	On-state resistance

SPICE	Simulation program with integrated-circuit emphasis
TLB	Transmission-line branch
t_{pd}	Propagation delay time. The time between the specified reference points on the input and output voltage waveforms, with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH}).
t_{PHL}	Propagation delay time, high-to-low level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined high level to the defined low level.
t_{PLH}	Propagation delay time, low-to-high level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined low level to the defined high level.
TTL	Transistor-transistor logic
V_{OH}	High-level output voltage. The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output.
V_{OL}	Low-level output voltage. The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265