Flexible Voltage-Level Translation With CBT Family Devices

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TEXAS INSTRUMENTS

Abstract

Voltage translation between buses with incompatible logic levels can be accomplished using Texas Instruments (TI™) translation-voltage clamps (TVC) or standard crossbar technology (CBT) devices. CBT devices in this application offer flexibility in designs, protection of circuits that are sensitive to high-state voltage-level overshoots, and cost efficiency.

Introduction

In designing electronics systems, proper interfaces between buses with incompatible logic levels must be provided. Voltage-level translation is necessary to allow the interconnection with flexibility to provide a future migration path to lower-voltage input/output (I/O) levels (see Figure 1). TI offers I/O voltage translation solutions with two device families.

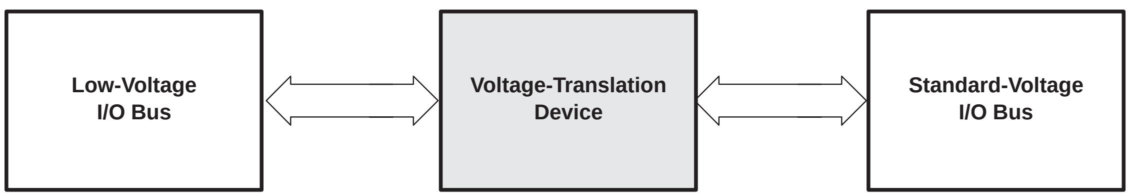

Figure 1. Flexible Voltage-Translation Application

One possible solution for flexible voltage translation is the TI translation-voltage clamp (TVC) family that has been designed specifically for protecting sensitive I/Os (see Figure 2). The information in the data sheet for each TVC-family device describes the I/O protection application of the TVC family and should enable the design engineer to successfully implement an I/O protection circuit utilizing the TI TVC solution.

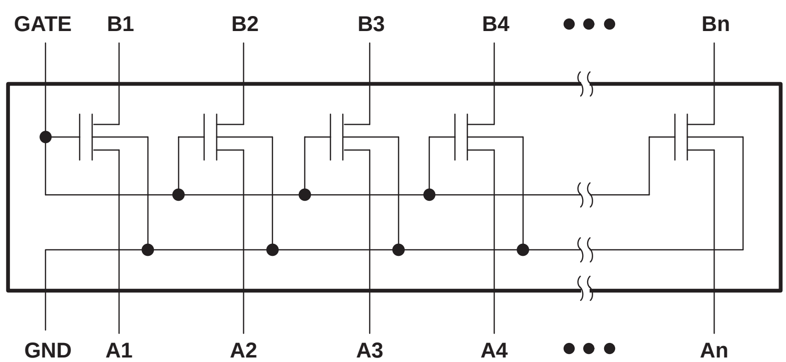

Figure 2. Simplified Schematic of a Typical TVC-Family Device

A comparable solution, allowing cost-effective and flexible voltage translation implemented with standard crossbar technology (CBT) family devices is described in this application report.

TI is a trademark of Texas Instruments Incorporated.

Device Description

The CBT family of devices provides an array of n-type metal-oxide semiconductor (NMOS) field-effect transistors (FETs) with the gates cascaded together to a control circuit (see Figure 3). Within a CBT device, all of the transistors are fabricated at the same time on one integrated die. This leads to a very small fabrication-process variation in the characteristics of the transistors. Because, within the device, the characteristics from transistor-to-transistor are the same, there is minimal deviation from one output to another. This is a large benefit of the CBT solution over discrete devices.

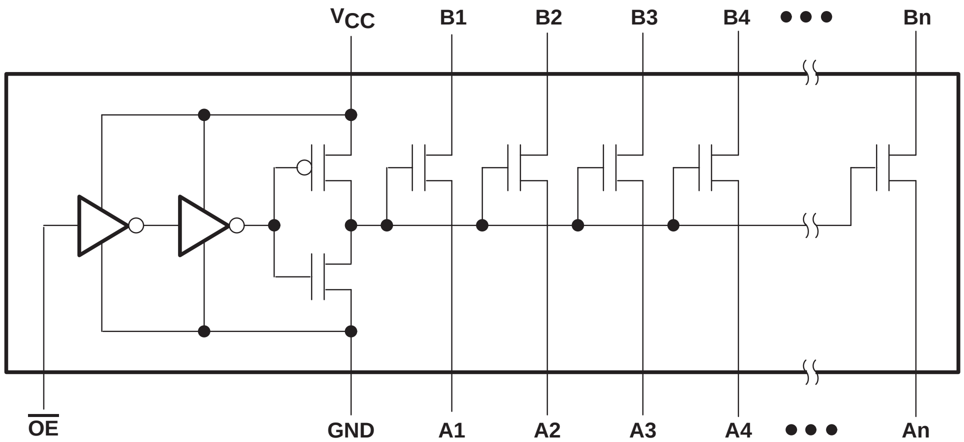

Figure 3. Simplified Schematic of a Typical CBT-Family Device

A CBT device can be used as a voltage limiter or voltage translator by connecting one of the FETs as a reference transistor, and the remainder as pass transistors. The most positive voltage on the low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. All of the transistors in the array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Because the transistors are fabricated symmetrically and the I/O signals are bidirectional through each FET, either port connection of each bit can be used as the low-voltage side.

Application

When the active-low, output-enable ($\overline{OE}$) input is connected directly to ground, the gate of the p-channel FET in the final inverter of the control circuitry is grounded. This saturates the p-channel, turning the FET on hard, and effectively connects the V_{CC} input directly to the gates of the n-channel pass transistors, thus providing external control of the gate voltage.

For the example in Figure 4, the ASIC has an open-drain interface that is sensitive to high-state voltages. For the voltage-limiting configuration, the CBT $\overline{OE}$ input must be grounded. The V_{CC} input must be connected to one side (A or B) of any one of the transistors. This connection determines the V_{BIAS} input of the reference transistor. The V_{BIAS} input is connected through a pullup resistor (typically 200 kΩ) to the V_{DD} supply. A filter capacitor on V_{BIAS} is recommended. The opposite side is used as the reference voltage (V_{REF}) connection. The V_{REF} input must be less than V_{BIAS} – 1 V to bias the reference transistor into conduction. The reference transistor regulates the V_{BIAS}, thus gate voltage (V_G) of all the pass transistors. The gate voltage is determined by the characteristic gate-to-source voltage difference (V_{GS}) because $V_G = V_{REF} + V_{GS}$. The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of $V_G – V_{GS}$, or V_{REF}. A weak pulldown resistor on open-drain outputs ensures that when the output switches off (logic high), overshoots do not cause the voltage to exceed the maximum voltage rating.

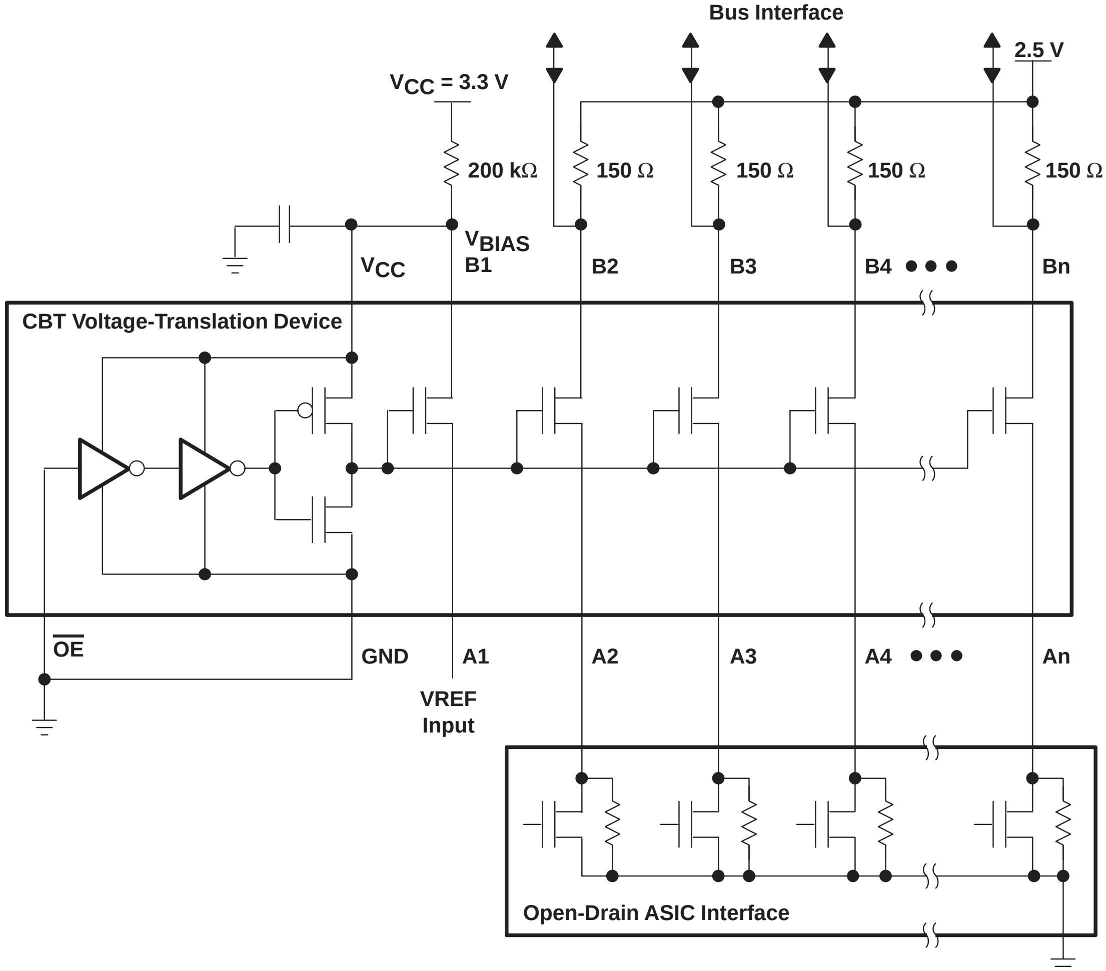

Figure 4. Typical Application of CBT as a Voltage-Translation Device

Conclusion

TI offers a line of CBT devices, including standard, Widebus™, dual-bit, and single-bit functions. The flexibility of CBT enables a low-voltage migration path for advanced designs to align with existing industry standards. The TI CBT family provides the designer with a solution for voltage-level translation and protection of circuits with I/Os that are sensitive to high-state-voltage-level overshoots.

Acknowledgment

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