Achieving Maximum Speed on Parallel Buses With Gunning Transceiver Logic (GTLP)

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ABSTRACT

This application report compares two approaches for synchronous bus-system designs. The focus of the report is the comparison of a system using central-synchronous system clock (CSSC) with a system operated with a source-synchronous system clock (SSSC).

The basic characteristics of lines, key factors that influence the bus line delay, and the impedance of bus lines are described.

The theoretical advantages of an SSSC system over a CSSC system are based on a comparison of timing budget calculations. Theoretical results are confirmed by measurements, using the GTLP demonstration backplane.

In the SSSC mode, the system-clock frequency is, with a clock frequency of 120 MHz, about 2.4 times higher than in the CSSC mode.

Contents

List of Figures

List of Tables

1 Introduction

Driver modules that are set up for a modern-wiring backplane have many complex requirements. The drivers must switch fast, with the smallest possible propagation time and the greatest possible number of bits in one driver, to provide the necessary data throughput over the bus.

In addition, the driver should have a sufficiently high driver capacity to generate the required logic levels, even in the case of a full backplane with many interconnected receive and transmit modules. Also, the drivers should have a small noise potential and a large noise margin. The optimum driver should use little power and have the live-insertion with precharge property, which allows exchanging modules during operation without impairing the function of the overall system.

In many electronic systems, shutdown to change a defective system part is not possible without severe adverse consequences for the complete application. Examples are electronic telecommunications systems, the control center in an electrical power-supply company, or computers used by air-traffic controllers.

The GTLP bus drivers address all the above points: minimum propagation time, high-drive capability, and the capability of being inserted into, or removed from, the system during operation, and have been developed especially for this type of application.

This application report emphasizes system speed, which is achieved by the appropriate architecture, using GTLP devices.

Section 2 describes physical basics of backplanes. Influences of the number of modules and the distance between modules on the properties of transfer speed and line impedance are explained.

Section 3 discusses two setups, both of which are based on a synchronous system design using GTLP devices:

- Central-synchronous system clock (CSSC) – All system cards use the same clock as base for the data.
- Source-synchronous system clock (SSSC) – The transmitter also sends the clock signal, via an additional line, along with the data.

The theoretical considerations are confirmed by measurements using the GTLP demonstration board.

In principle, both systems can be set up using technologies other than GTLP. However, the combination of the advantages of high-driver capability, live-insertion capability, and flexible edge steepness that can be modified during operation, is found only with the GTLP bus-driver solution.

2 Physical Properties and Limitations of Bus Lines

The basic composition of a line consisting of capacitive and inductive replacement components is shown in Figure 1. In the case of static conditions, line impedance primarily is determined by the ohmic resistance and/or the parallel conductance of C′ of the line. These are not of any consequence at a frequency of just a few kilohertz, because the frequency is in the term $\omega = 2 \times \pi \times f$.

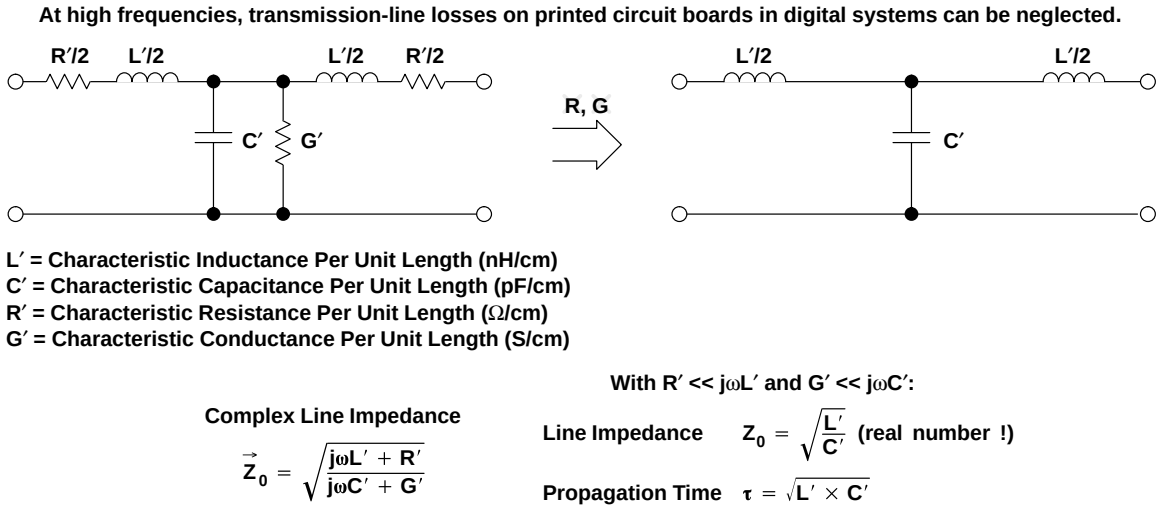


Figure 1. Ideal Transmission Line With Negligible Conductance and Resistance

Comparing the apparent impedance for a specified frequency (e.g., 1 MHz) with the parallel conductance G′ and the series resistance R′ shows that G′ and R′ are negligible compared with the line impedance Z_O.

The simplified formulae for line impedance and the propagation delay time per unit length are dependent only on the inductive and capacitive layer of the line. In practice, calculations are easy to handle. In the case of a homogeneous line, which represents a connection between a transmitter and a receiver, its capacitive and inductive layers determine the line property.

However, if we look at bus lines, such as the one in Figure 2, the line impedance no longer is constant and is dependent on the number of inserted modules.

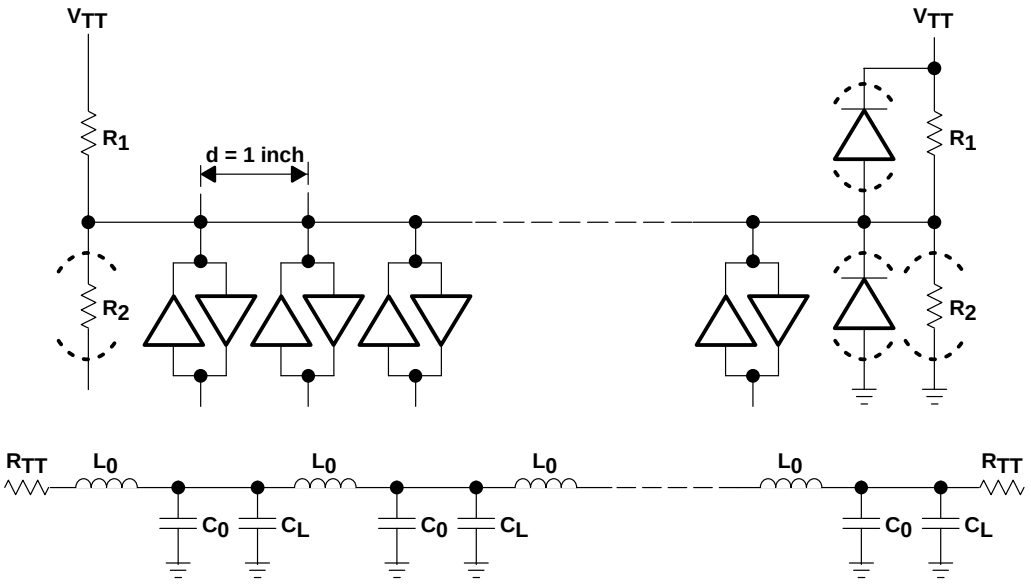


Figure 2. Additional Capacitive Load of Line by Modules

If the distances between the inserted modules remain electrically short, i.e., twice the propagation delay time between two inserted modules is shorter than the rise/fall time of the signal, it is possible to add the capacitive load to the capacitive layer. The influence on the inductive layer is negligible.

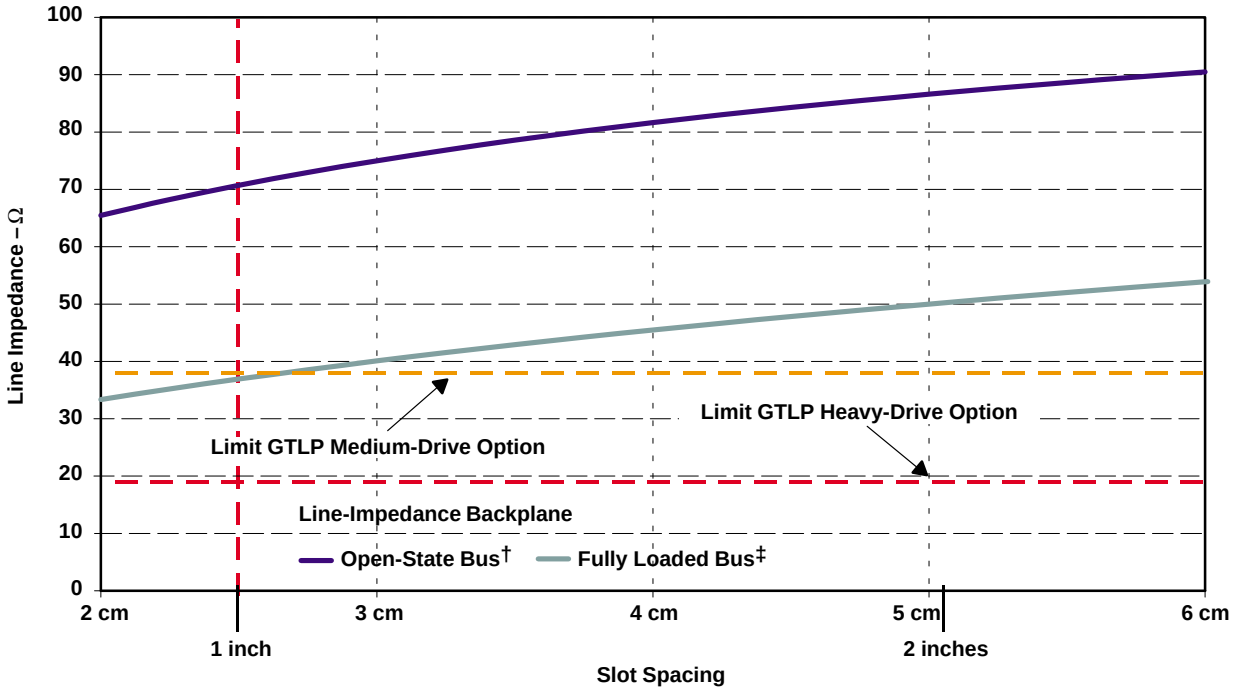
Table 1 shows the comparison between a point-to-point connection on a PCB, an unloaded bus line with the bus connectors only, and a fully loaded bus. The distance between the slots is 1 inch.

Table 1. Comparison of PCB Line and Bus Line (Slot Distance = 1 Inch)

LINE PARAMETER	OPEN LINE		LOADED LINE (BUS)
	PCB	BUS	
Inductive layer, L_0	6.5 nH/cm	6.5 nH/cm	6.5 nH/cm
Capacitive layer, C_0	0.4 pF/cm	0.4 pF/cm	0.4 pF/cm
Connector	Not applicable	2 pF per slide-in module	2 pF per slide-in module
Feed line to backplane side of connector	Not applicable	<<1 pF	<<1 pF
Feed line to module side of connector	Not applicable	Not applicable	~1 pF
Input capacity of receiver	Not applicable	Not applicable	9 pF
Additional capacity load, C_L	Not applicable	2 pF/2.54 cm	10 pF/2.54 cm
Capacitive load per cm	0.4 pF	1.2 pF	4.73 pF
Line impedance, Z_O	127 Ω	74 Ω	37 Ω
Propagation delay time of signal, τ	5.1 ns/m	8.8 ns/m	17.5 ns/m

While the inductive layer remains almost constant in all three cases, the connectors, stub lines to the connector, and driver input and output, as well as the input capacity of the receiver, represent an additional capacitive load for the line. The increased capacitive load reduces the line impedance and starts the demand for higher driver capability for bus-interface logic. However, the signal propagation delay time via the bus increases significantly (by a factor of more than three in the example above)

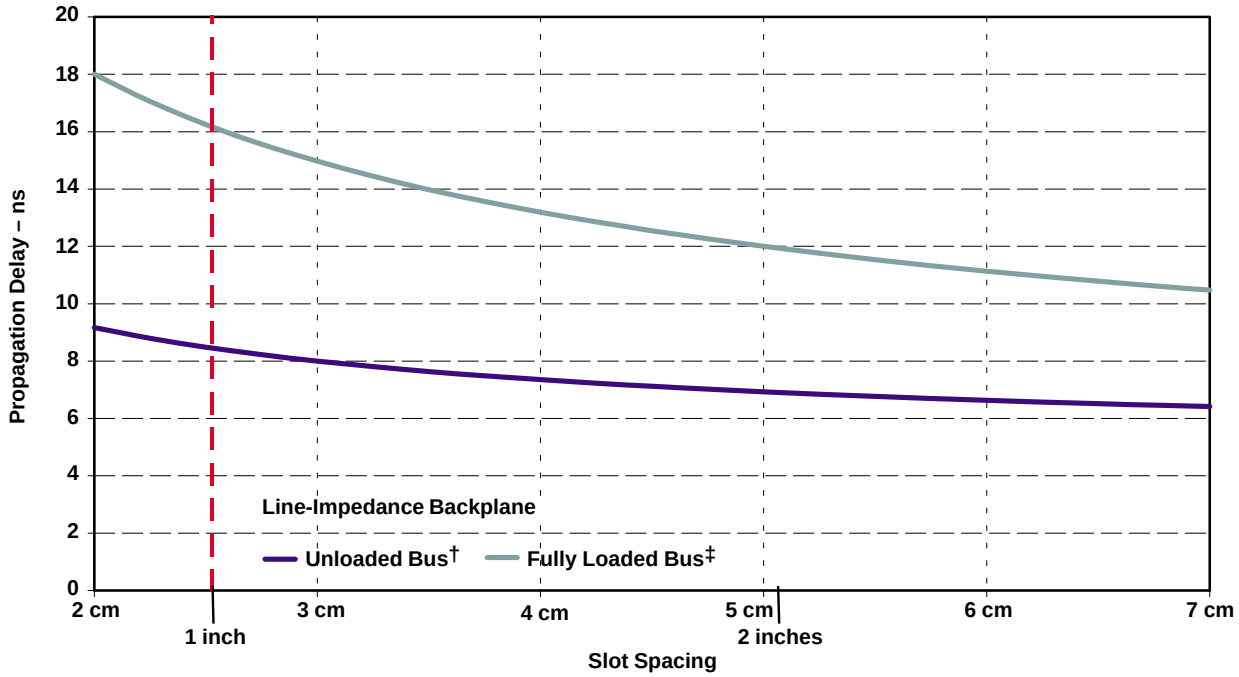
Changing the distances between the modules affects the capacitive layer of the line as shown in Figure 3.



† Assuming a capacitive load of 2 pF per slot (connector only)
‡ Assuming a capacitive load of 10 pF per slot (complete module)

Figure 3. Effect of Slot Spacing on Line Impedance

One curve represents a bus line in the unloaded state, for which the bus-side connectors are the only loads on the line. The other curve represents a fully loaded bus line. The same correlation also is produced with regard to the propagation time of the line, and is shown in Figure 4.



† Assuming a capacitive load of 2 pF per slot (connector only)
‡ Assuming a capacitive load of 10 pF per slot (complete module)

Figure 4. Effect of Slot Spacing on Flight Time

The values from Table 1 for the slot distance of 1 inch in Figures 3 and 4 can be found at intersections with the dashed lines.

The homogeneity of the line impedance cannot be ensured in every case. For a backplane, the modules can be inserted into different positions on the backplane, and some positions can be left empty, so the different bus-line sections have different impedance values.

However, this fact does not significantly affect the quality of the signal.

3 Transfer Modes

For a synchronous system, as the name suggests, it is important for the transferred data to refer to a common system-clock signal. Every participant in the system then gets the active edge of system clock as a reference and a data signal, which refers to the system clock.

In this section, two synchronous transfer modes are described:

- Central-synchronous system clock (CSSC) mode
- Source-synchronous system clock (SSSC) mode

System parameters that have an important role in affecting the maximum clock speed, in conjunction with the calculation of the time budget, are discussed in the following subsections.

3.1 Parameters for the Time Budget

Parameters for the time budget are assigned to different sources (see Figure 5). The transmitter and clock-distribution devices have skew values and additional propagation time as a result of simultaneous switching. Flight time represents the propagation delay time of the signal via the bus. Finally, the setup and hold times of the receiver must be taken into account.

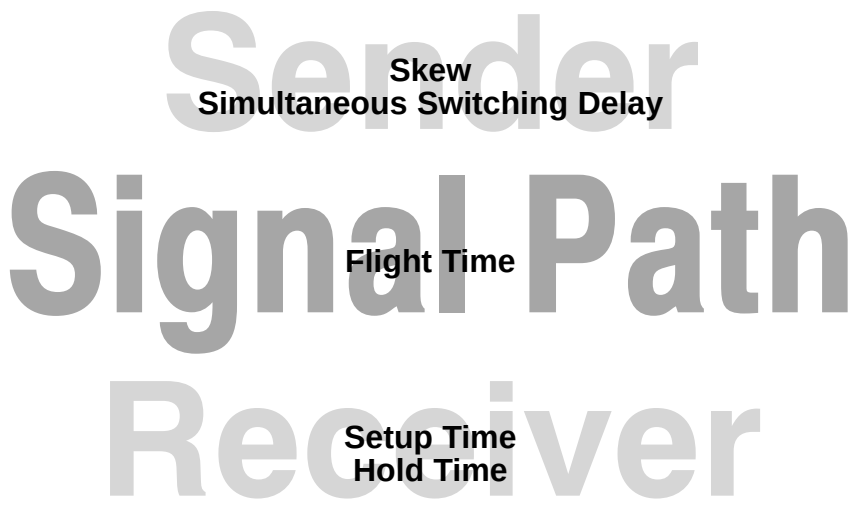


Figure 5. Important Parameters for the Time Budget

3.1.1 Skew

Skew is the small difference that arises from different propagation delays between output stages within a device. These differences, which cannot be prevented, are defined in the EIA/JEDEC standard, *Definition of Skew Specification for Standard Logic Devices* (EIA/JESD 65) (see Figure 6).

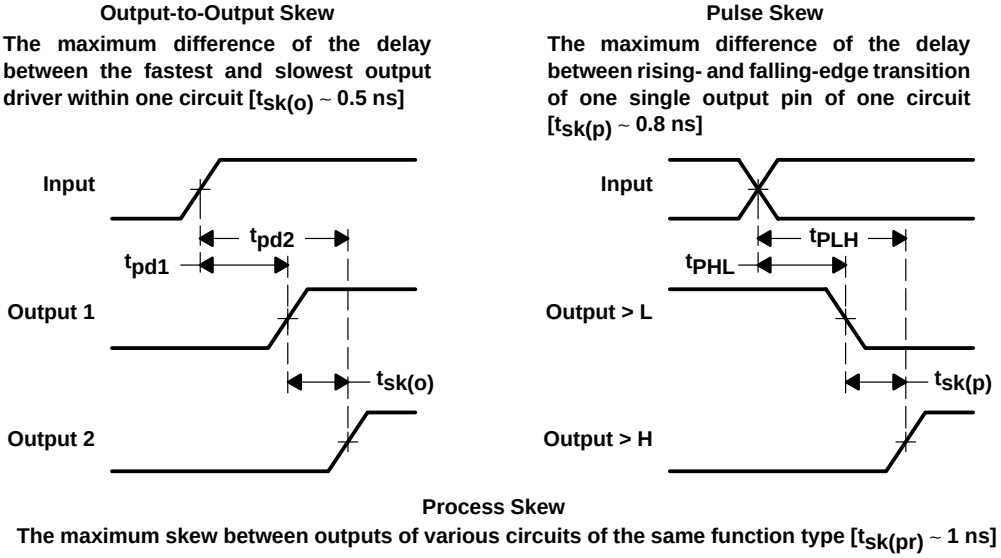


Figure 6. Skew Definitions

Output-to-output skew, $t_{sk(o)}$, is the maximum difference between the slowest and the fastest of the drivers within a package. For clock distribution drivers, $t_{sk(o)}$ is approximately 500 ps. For interface devices, this parameter is not always given, but is typically less than 1 ns.

Pulse skew, $t_{sk(p)}$, describes the difference in propagation delay time between the positive and negative edge, and it is an important definition, if there is a specific duty cycle required.

Should more than one device participate in the clock distribution, process skew (which is the maximum difference in propagation time between drivers of the same function) is defined. Process skew is added to the output-to-output skew.

3.1.2 Propagation Time Due to Simultaneous Switching

The simultaneous switching parameter, Δt_{pd}, is the difference in propagation time that arises from the simultaneous switching of several outputs of the same device.

Data sheets show only the maximum propagation time of one output when it is the only one to be switched. An additional propagation time must be taken into account when multiple outputs are switched simultaneously. The reason for the increase in propagation time is the internal package inductance, which works as a current brake. The more outputs that are switched on, the greater the current and, therefore, the braking effect is greater. Figure 7 shows this correlation for different package options.

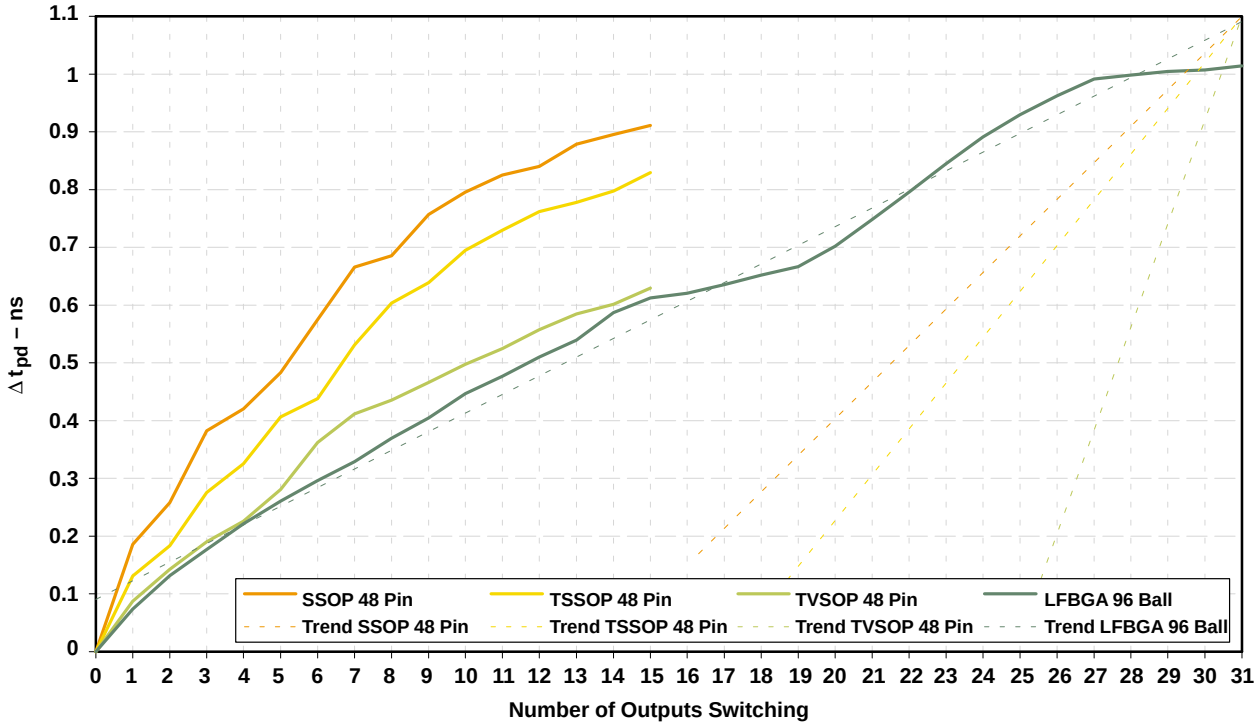
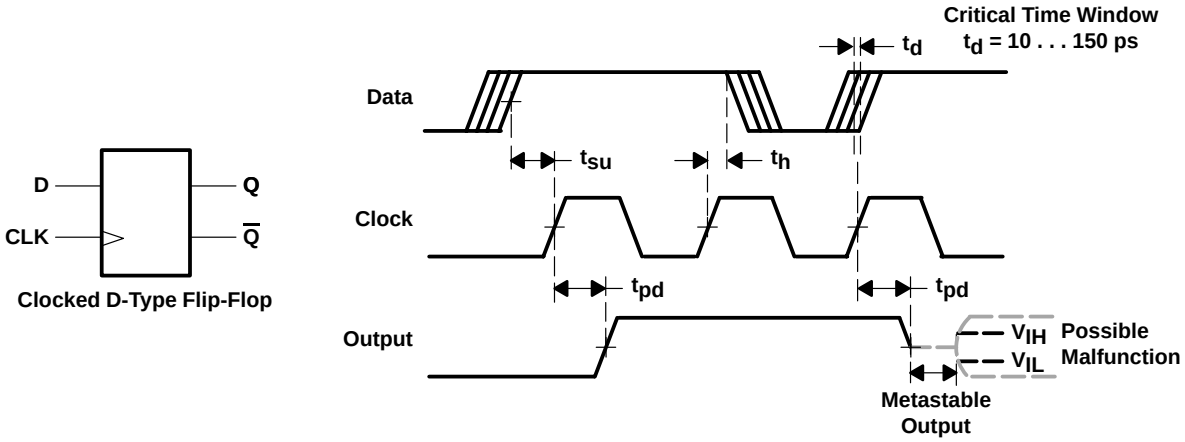


Figure 7. Effect of Simultaneous Switching on Propagation Time

The low-profile fine-pitch BGA (LFBGA) package shows the best skew behavior, when forced by simultaneous switching, in this comparison. Despite having double the number of outputs switched at the same time, the absolute difference of the propagation delay in Figure 7 is not significantly greater than that of other modern 16-bit dual-inline packages.

3.1.3 Setup and Hold Times at Receiver Input

In a synchronous system, a common clock signal, which is synchronous for all the interface devices (e.g., registers or flip-flops) exists. Figure 8 shows the definitions for setup and hold time based on a D flip-flop. Both times are defined around the active edge of the clock signal.



NOTE: The setup and hold times are given in the data sheets. For GTLPH1655, t_{su} is 2.6 ns and t_h is 0.5 ns.

Figure 8. Setup and Hold Times

The setup time is the time during which a data signal must be stable before the active edge of the clock input occurs. The hold time is the time during which a data signal must be stable after the active edge of the clock input occurs. Should either of the two times be violated, it is possible that the output can be in a metastable state in the critical time window. The result can be a state in undefined range or even in the threshold region, that represents neither a logical 1 nor a logical 0. The consequence can be that the subsequent stage can interpret the value as either high or low. Therefore, the probability of malfunctions increases dramatically.

3.2 Central Synchronous Clock Distribution

A basic prerequisite for a synchronous system is that the transferred signals refer to a common clock signal that is transmitted from a central clock distribution circuit. In the layout shown in Figure 9, the active clock edge reaches all parts of the system as simultaneously as possible. For skew adjustment, the line lengths have been chosen to be as close as possible.

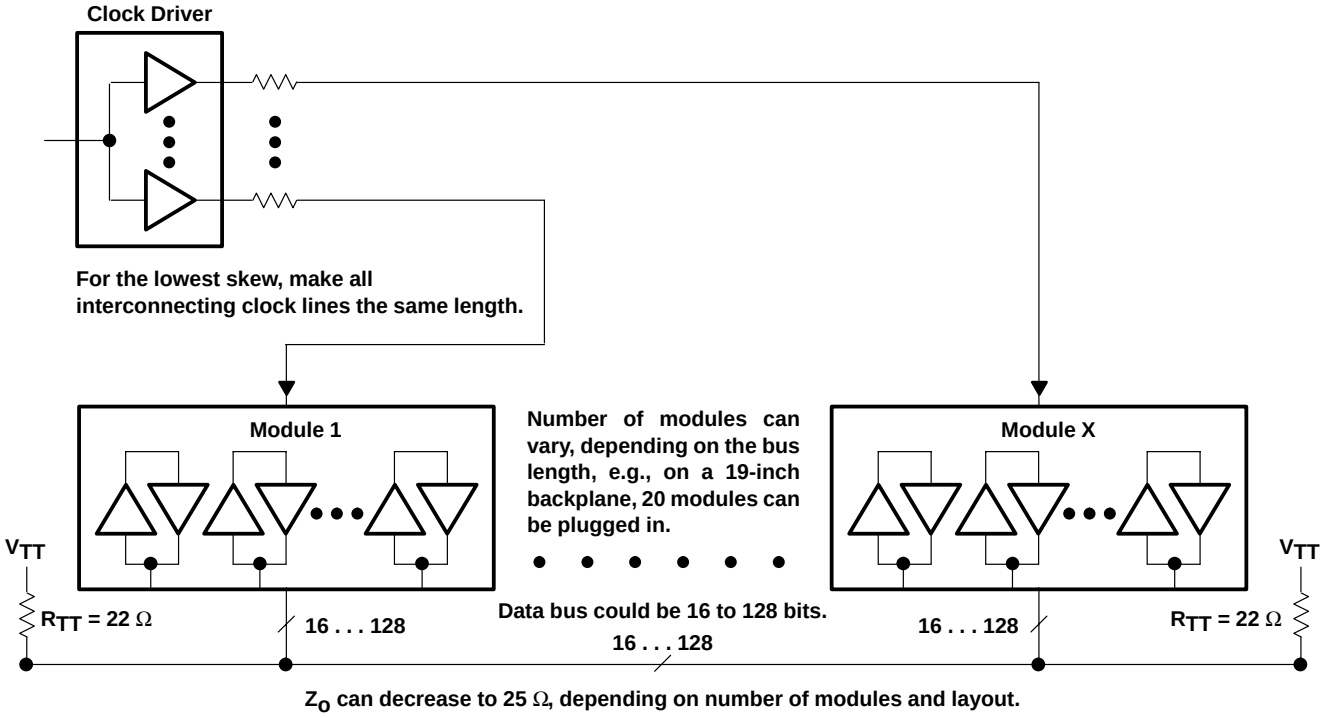
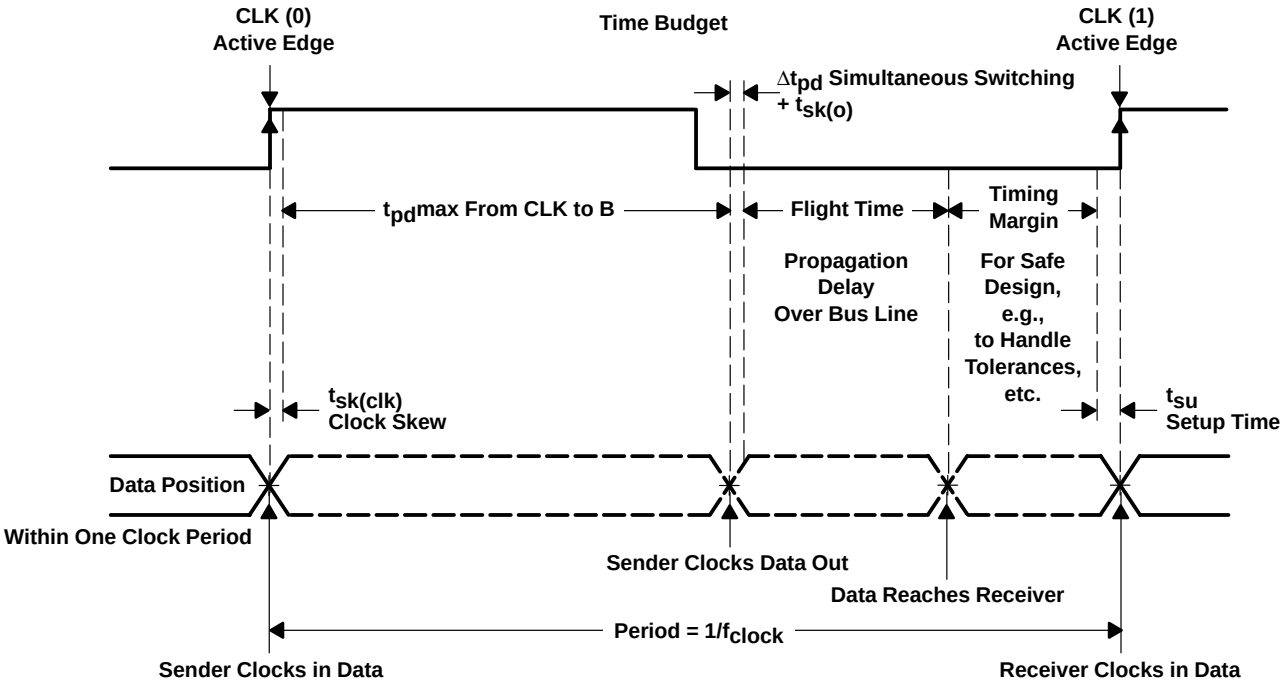


Figure 9. Principle of Central Synchronous Clock Distribution

Figure 10 shows the time budget for the central-clock distribution. All times that must be taken into account are shown. The main contributors of time in the timing budget are the propagation delay time of the device and the propagation delay time over the bus.



NOTE: No additional clock signal line is required because all receivers refer to system clock.

Figure 10. Time Budget for Central Synchronous System Clock Distribution Environment

The need for all system parts to receive the clock at the same time is a disadvantage because the propagation delay time of the data signals via the bus must be taken into account when determining the maximum frequency of the system.

The transmitted data must propagate over the distance from the transmitter to the receiver within a single clock cycle, because the transmitter and the receiver work with exactly the same active edge of the clock signal.

Should the data fail to reach the receiver input within a clock period, the synchronicity of the system no longer can be ensured. In this case, the signal reaches one part of the bus system at the right time (within the same clock period), while another part does not receive the signal until one clock period later. This effect is shown as case 2 of Figure 11.

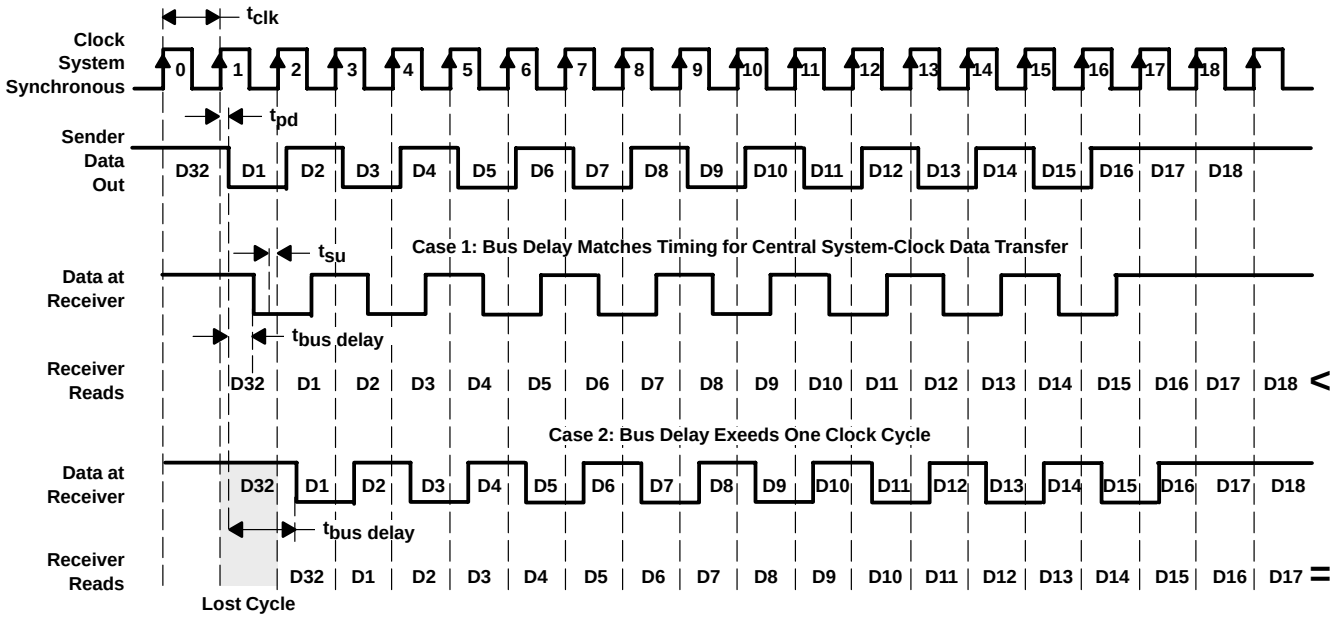


Figure 11. Two Examples for Data Transmission in a Central Synchronous System Clock Distribution Environment

The maximum frequency is calculated from the skew of the clock-distribution circuit [t_{sk}(clk)], the device propagation (t_{pd}), the skew of the driving device, the additional propagation delay time (Δt_{pd}) due to simultaneous switching of several outputs, the transit time via the bus [t_{flight}(bus)], as well as the setup time of the connected receiver [t_{setup}(rec)]. The formula for calculating the maximum frequency is:

$$f_{max}(clk) = \frac{1}{t_{sk}(clk) + t_{pd}(clk\ to\ B) + \Delta t_{pd}(sim.sw.transm.) + t_{sk(o)} + t_{flight}(bus) + t_{setup}(rec)} \quad (1)$$

With:

$t_{sk(o)}$(clk)	= 0.5 ns
t_{pd}(GTLPH1655)	= 5.8 ns
Δt_{pd}	= 1 ns
$t_{sk(o)}$	= ns
Transit time via the bus t_{flight}(bus)	= 10 ns
Setup time for the receiver t_{setup}(rec)	= 2.6 ns
f_{max}	= 47.8 MHz

Central-synchronous clock distribution propagation delay time via the bus takes a large part of the available clock period. The propagation delay over the bus can be lower if the capacitive load is lower. For example, if only the transmitter and one receiver card are plugged into the bus and no additional modules are inserted, the maximum f_{max}(clk) must be put in the formula for a safe circuit design, i.e., assume that all slots are filled with cards.

3.3 Source-Synchronous Clock Distribution

To eliminate the signal propagation delay time on the bus, the solution illustrated in Figure 12 can be used. An additional line for the source-synchronous clock signal and other lines for the arbitration or transmission of the send/receive status are required. However, propagation delay time over the bus (t_{flight}) is eliminated from the calculation of the maximum clock frequency. Therefore, a significantly higher system speed is possible.

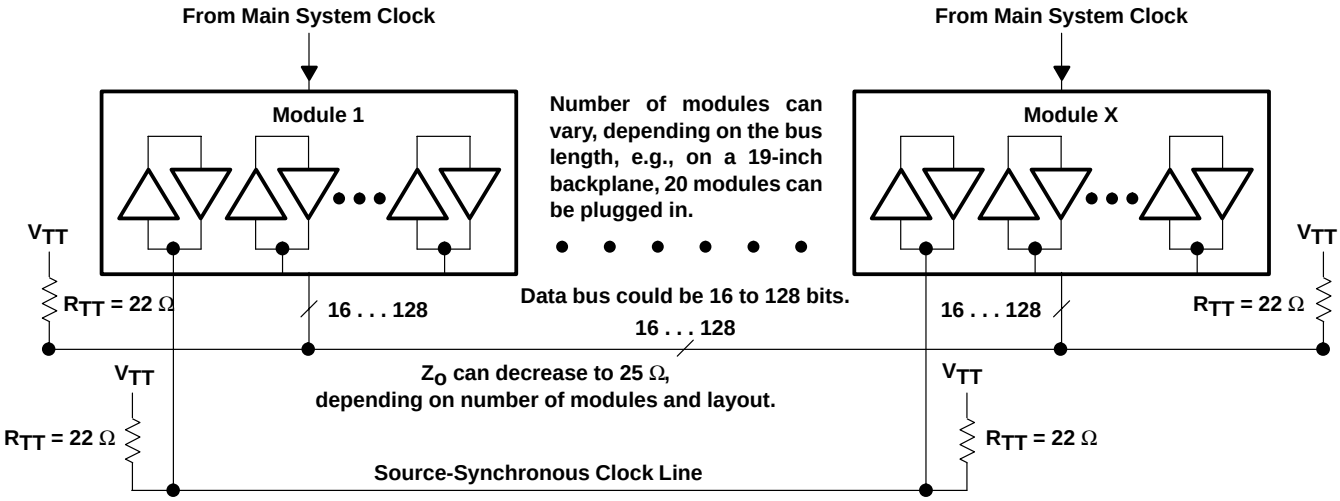


Figure 12. Principle of Source-Synchronous Clock Distribution

The times to be observed refer to two successive clock periods. The first clock period includes times that must be taken into account relative to the transmitter, while the second clock period includes critical times for the receiver. There are two requirements for the maximum clock speed:

$$f_{max}(clk) \leq \frac{1}{t_{sk}(clk) + t_{pd}(clk\ to\ B) + t_{sk(o)} + \Delta t_{pd}(sim.sw.transm.)} \quad (2)$$

$$f_{max}(clk) \leq \frac{1}{t_{hold}(rec) + t_{setup}(rec)} \quad (3)$$

The smaller value for f_{max} from equations 2 and 3 represents the highest possible frequency. Figure 13 shows this correlation graphically.

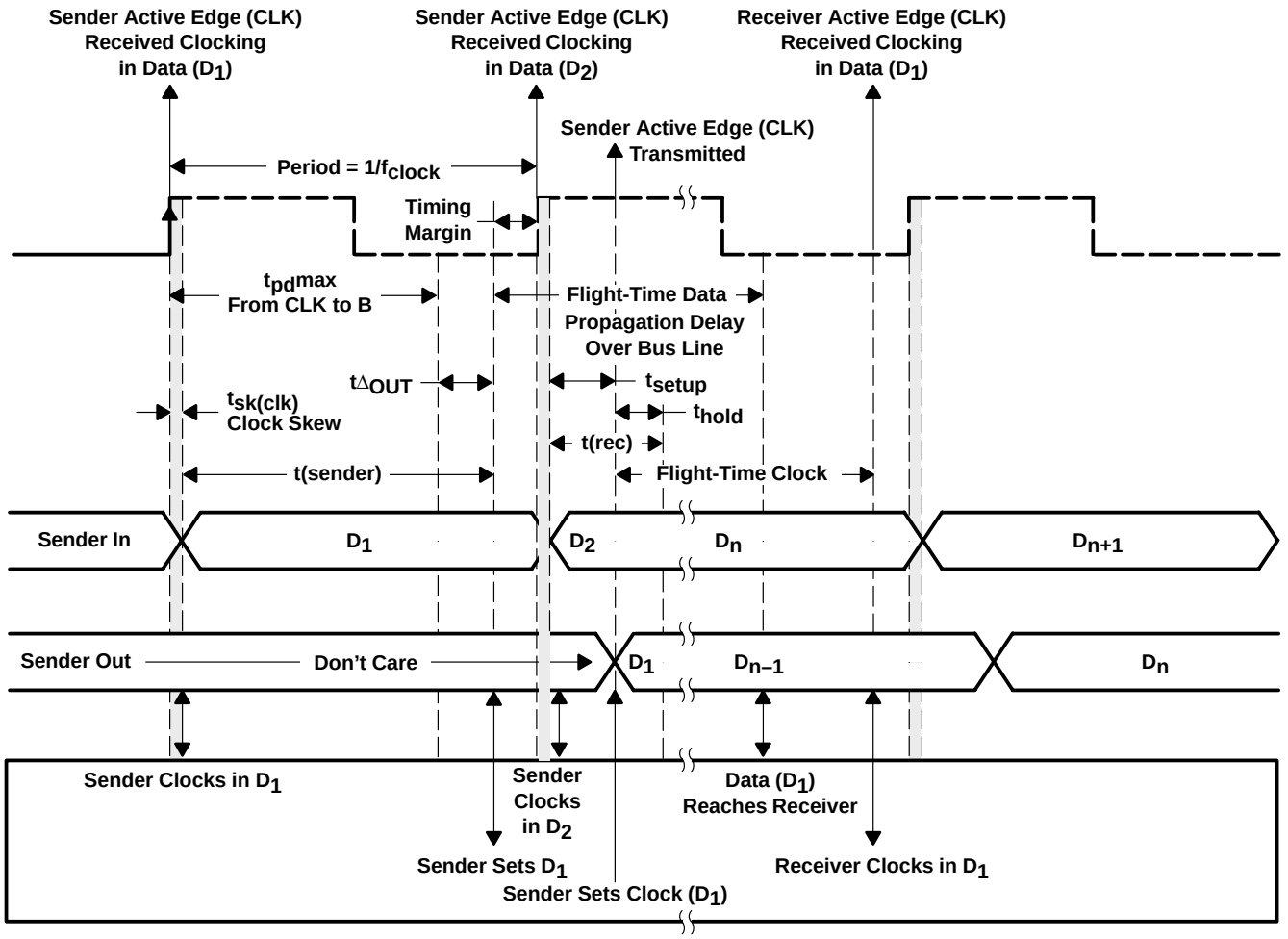


Figure 13. Time Budget for Source-Synchronous Clock Distribution

In this case, error-free synchronous data transfer that is independent of the propagation delay time over the line is possible (see Figure 14). The clock signal – with certain propagation to the data signal – is transferred via a separate clock line.

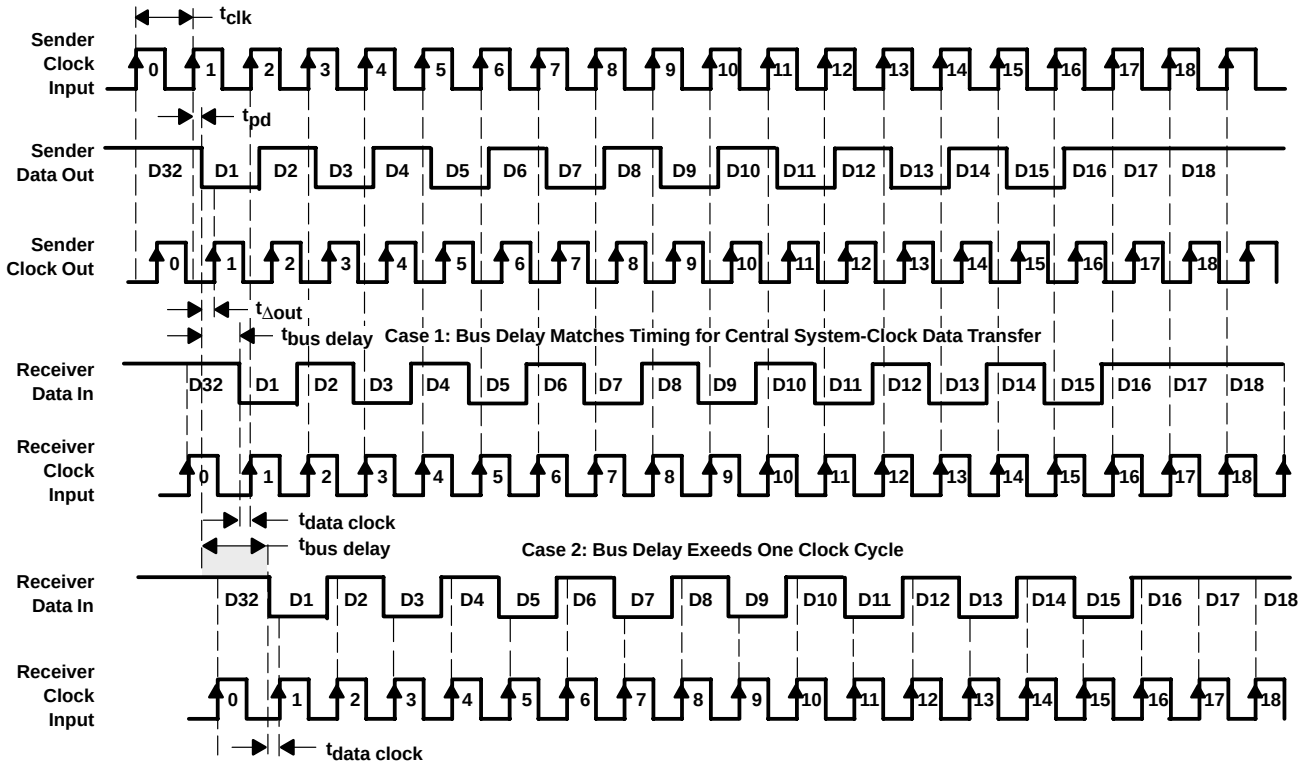


Figure 14. Two Examples of Source-Synchronous Clock Distribution

4 Measurements Using Texas Instruments GTLP Evaluation Module

Theoretical considerations concerning the two transmission modes discussed in the previous sections can be confirmed by measurements, using the GTLP demonstration backplane.

The evaluation module (EVM) (see Figure 15) is a good model for a typical parallel-backplane system as found, for example, in telecom applications.

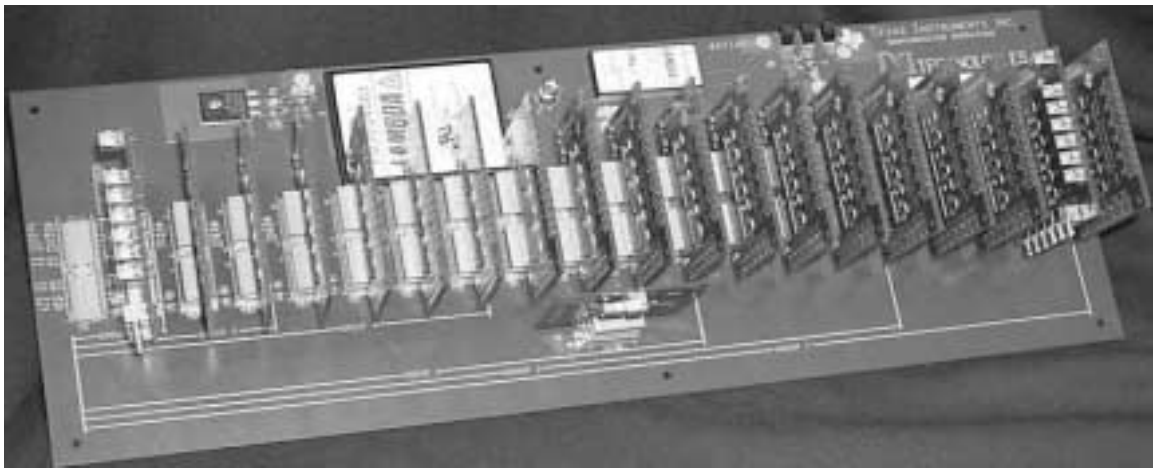


Figure 15. GTLP Demonstration Backplane

Altogether, 48 bits run in parallel over the 19-inch backplane, which has 20 slots, each 1 inch apart. The connectors are fully integrated onto the backplane, while the number of modules can vary. GTLPH1655 devices are used as the interface.

Different bus characteristics can be realized and shown using this EVM.

By using the EVM, it is possible to show the effect of termination resistances on signal quality, as well as different load conditions, due to a different number of modules on the bus. Also, the clock frequency is variable.

Figure 16 shows the layout of the driver card. Using a jumper, the transmitter can be switched from the system-synchronous clock mode to the source-synchronous clock mode.

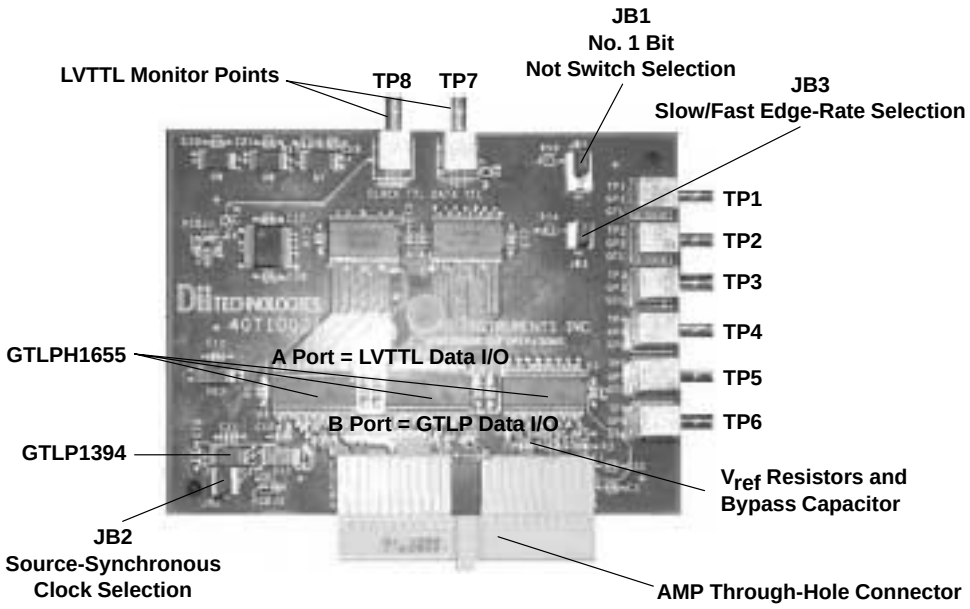


Figure 16. Layout of Driver Card With Monitor Points and Jumpers

Figure 17 shows a receiver card. The receiver card contains GTLPH1655 transceivers that receive data from the GTLP bus and translate it into LVTTL signals.

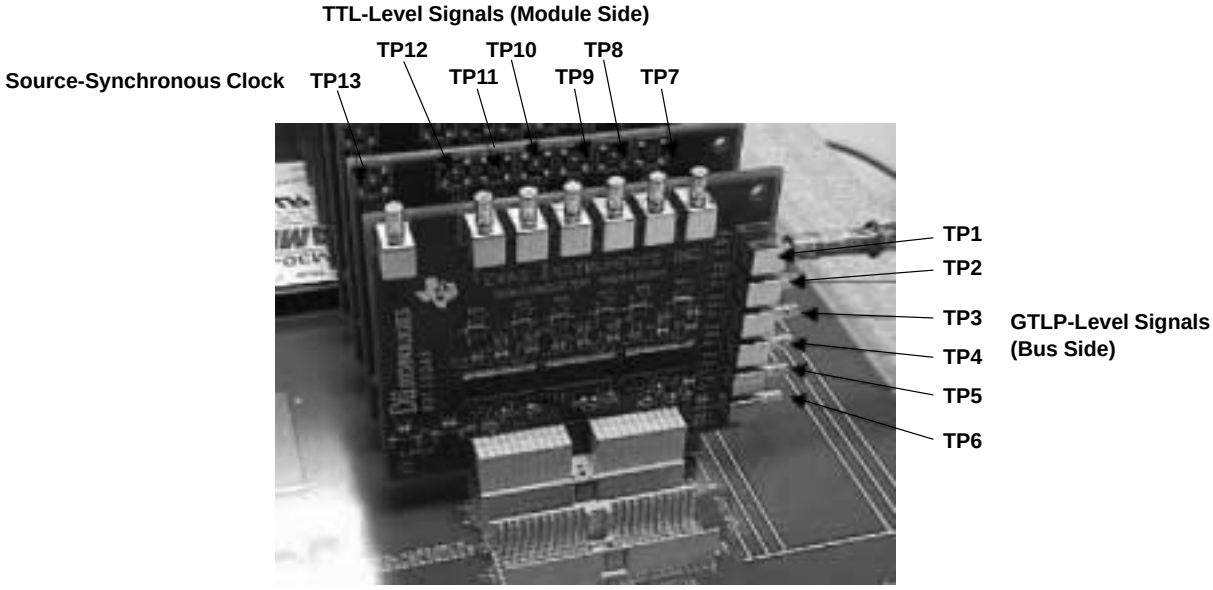


Figure 17. Receiver Card With Monitor Points

Using the receiver card, GTLP bus measurements (GTLP level) and module measurements (LVTTL level) are possible.

The EVM is used to illustrate the difference between system-synchronous data transfer and source-synchronous data transfer. The transmitter is at the beginning of the bus line, and the receiver is at the end of the bus. In both cases, 66 MHz is the clock speed, and gives a clock period of 15.15 ns.

4.1 Data Transfer With System-Synchronous Clock

The propagation time of the signal via the bus amounts to about 4 ns, if all other slots are empty. If the characteristics of the interface modules using GTLPH1655 devices are included, the worst-case scenario for the maximum clock speed is:

$$f_{max}(clk) = \frac{1}{0.5\ ns + 5.8\ ns + 1.1\ ns + 1\ ns + 4\ ns + 2.6\ ns} = \frac{1}{15\ ns} = 66.7\ MHz \quad (4)$$

With no load on the bus, timing already is critical at 66-MHz clock frequency because the timing margin is only 150 ps.

However, GTLPH1655 devices typically have less propagation time (about 3.5 ns compared with data-sheet value of 5.8 ns), thus, the critical frequency increases to about 78.7 Hz (see Figure 18).

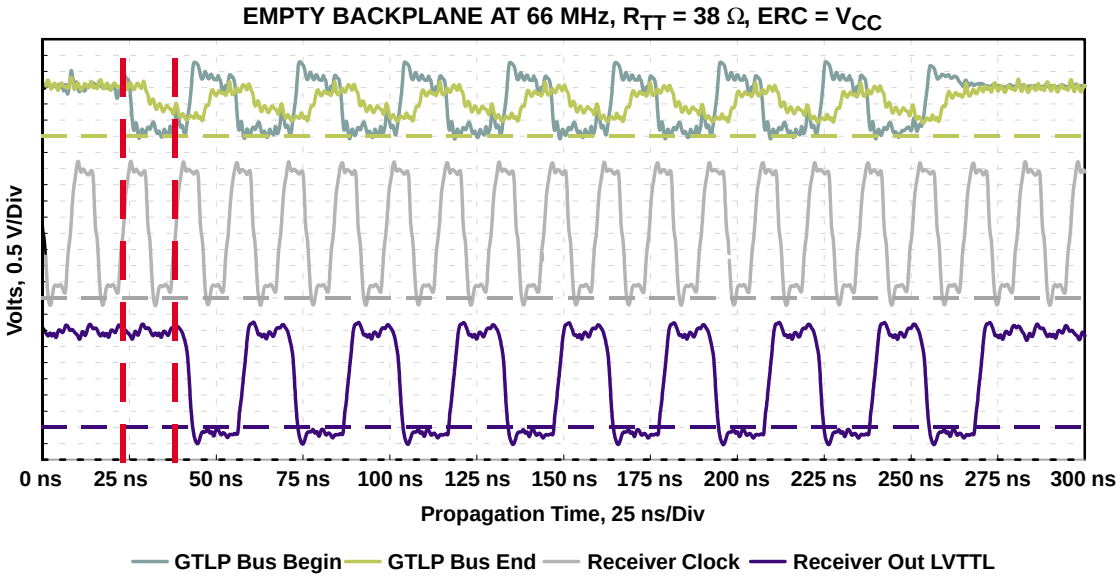


Figure 18. Empty Backplane Transmitter, CSSC in Slot 1, Receiver in Slot 20

However, if additional modules are inserted into the backplane, the capacitive load and, thus, the propagation delay time via the bus, increases significantly. In this case, the propagation delay time via the bus increases to about 10 ns. As a result, the maximum clock speed is significantly lower:

$$f_{max}(clk) = \frac{1}{0.5\ ns + 5.8\ ns + 1.1\ ns + 1\ ns + 10\ ns + 2.6\ ns} = \frac{1}{21\ ns} = 47.6\ MHz \quad (5)$$

Therefore, the required period in this case is 21 ns, increasing the chosen clock period from 66 MHz by 6 ns. The consequence is that not all modules receive the same data with the same clock edge. Some modules receive the data with the active edge of consecutive clock periods, as shown in Figure 19. With an empty backplane (see Figure 18), the data was transmitted with the next active edge of the clock signal at the receiver output. In this case, it takes one more clock period (see Figure 19).

In other words, the system no longer is working synchronously, and errors due to missing synchronicity can result.

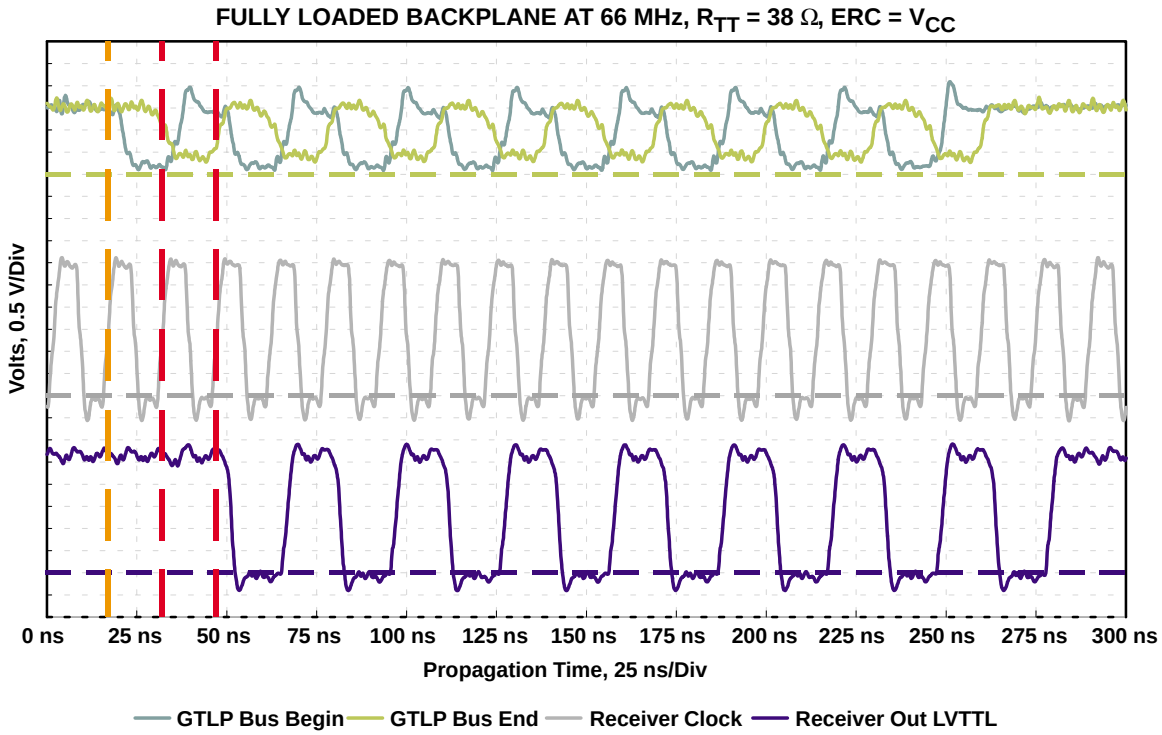


Figure 19. Empty Backplane Transmitter, CSSC in Slot 1, Receiver in Slot 20

4.2 Data Transfer With Source-Synchronous Clock

The sender is switched to source-synchronous clock mode by moving a jumper on the driver card. Comparing the signals on the empty backplane, there is little difference, as similar results are seen in the oscilloscope pictures (see Figure 16).

In the source-synchronous mode, the signal is within the same clock period (see Figure 20). The clock pulse no longer has any relation to the signal on the bus, because the clock pulse is measured at the receiver and, therefore, has a proper relation only to the TTL output signal.

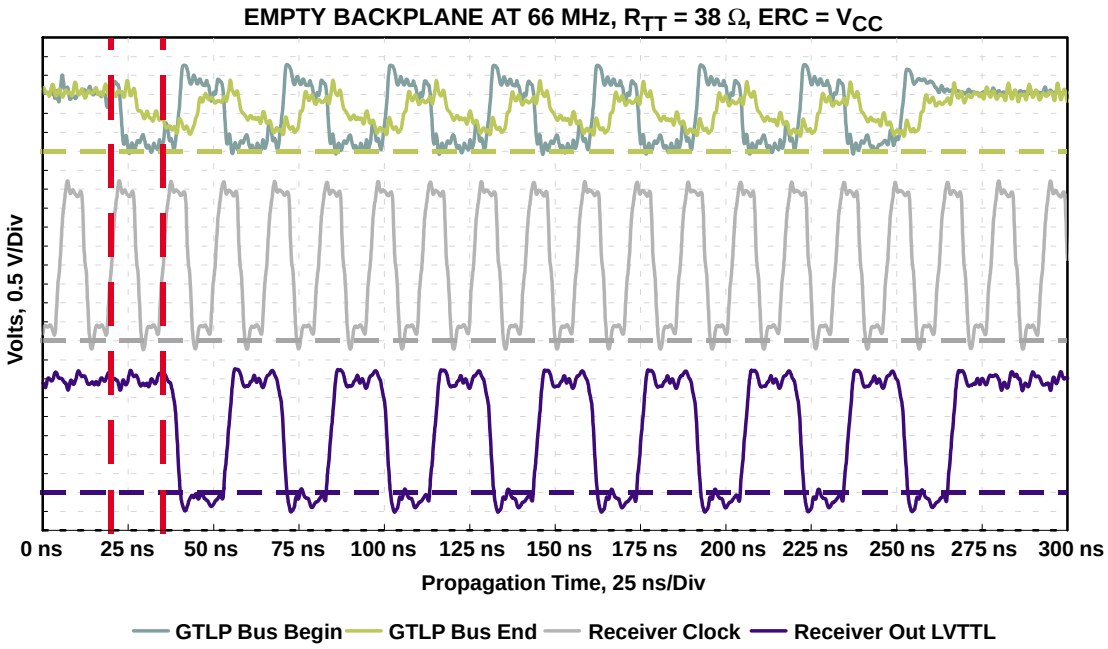


Figure 20. Signals on Empty Backplane, SSSC, Transmitter in Slot 1, Receiver in Slot 20

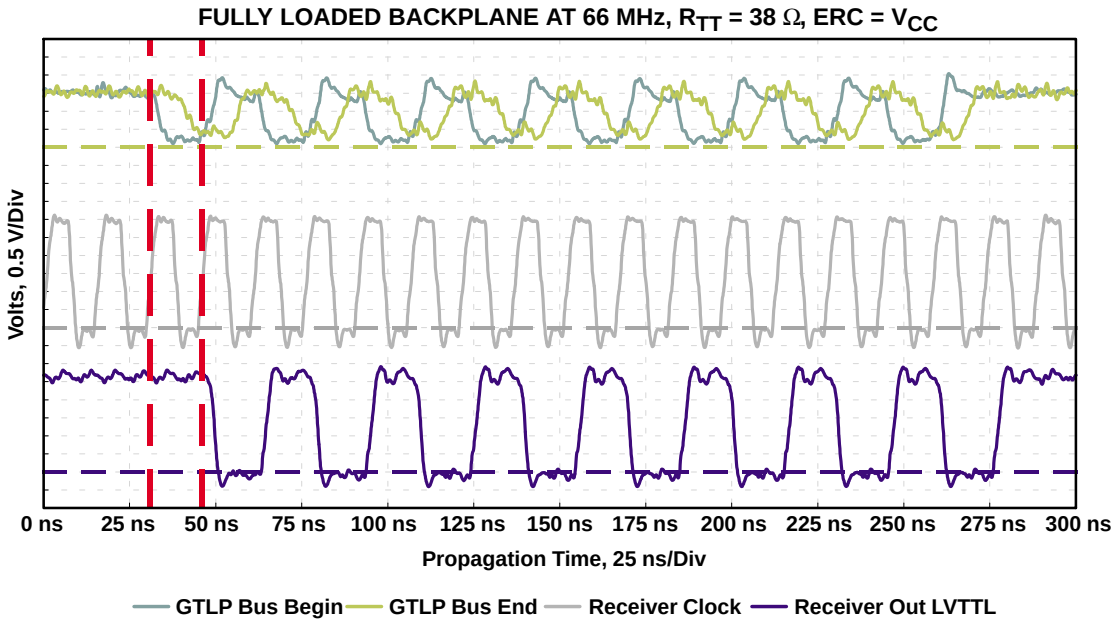


Figure 21. Fully Loaded Backplane, SSSC, Transmitter in Slot 1, Receiver in Slot 20

Even if the bus is fully loaded, a correct signal transfer can be observed. The only drawback is the need for an additional line in the bus layout. The clock signal always is transferred, with a small delay, to the present datum. The increase in propagation delay time via the bus, as a result of the additional input capacitance of the inserted modules, no longer is relevant.

The maximum frequency is calculated using data-sheet values, realistic approximations, and equation 2:

$$f_{max}(CLK) = \frac{1}{0.5\ ns + 5.8\ ns + 1.0 + 1\ ns} = \frac{1}{8.3\ ns} = 120.4\ MHz \quad (6)$$

5 Summary

With the central-clock-distribution system, the highest possible system pulse rate is about 50 MHz (assuming a 19-inch backplane). With the source-synchronous system, the clock frequency can be increased by a factor of 2.4, to 120 MHz.

Table 2 lists three system solutions, along with relevant parameters that must be taken into account during system design.

Table 2. Comparison of Parallel Bus Systems With Different Pulse Supplies

PARAMETER	SYNCHRONOUS SYSTEM		ASYNCHRONOUS SYSTEM
	CENTRAL-CLOCK DISTRIBUTION	SOURCE-SYNCHRONOUS CLOCK DISTRIBUTION	NO SYSTEM CLOCK PULSE
Pulse skew	Output-to-output pulse driver (to be taken into account)	Output-to-output pulse driver (to be taken into account)	Not applicable
t_{pd} CLKAB	Device dependent (to be taken into account)	Device dependent (to be taken into account)	Not applicable
Δ Data – pulse	–/–	To be fixed	Not applicable
t_{pd} (sim.switch)	Package dependent (to be taken into account)	Package dependent (to be taken into account)	Package dependent (to be taken into account)
$t_{sk(o)}$	Device dependent (to be taken into account)	Device dependent (to be taken into account)	Device dependent (to be taken into account)
Bus propagation delay time	Bus dependent (to be taken into account)	0 ns Not applicable	Bus dependent (to be taken into account)
Setup time	Package dependent (to be taken into account)	0 ns Not applicable	Not applicable

For the central-system-clock solution, a central clock exists for all bus attendees. The maximum clock speed is about 50 MHz and provides a 32-bit data width and a data throughput rate of up to 1.6 Gbit/s. A significant limiting factor for the time budget is the transit time via the bus.

For a system with a source-synchronous system clock, the clock signal, with a slight shift in time to the data, is sent together with the data signal on the bus. The delay between data and clock is constant for all bus members. The maximum clock speed is about 120 MHz. The 32-bit data width results in 3.8 Gbit/s as the maximum data throughput. A significant limiting factor for the time budget in this setup is the propagation time, compared with the clock period.

A further option is asynchronous data transfer, in which an integrated system clock does not exist. All the bus drivers are in transparent mode, and switch the outputs according to their propagation time. Therefore, there is no common clock speed.

The asynchronous data frequencies can be 160 MHz, or more, depending on the technology. However, the effective maximum frequency is reduced significantly by additional requirements, such as the introduction of a bus protocol, which is indispensable in this system. The maximum frequencies that produce the theoretical data rate, which is based on 32 bits of up to 5.12 Gbit/s (at160 MHz), can be reached only for a short time, not continuously.

6 Glossary

BTL	Backplane transceiver logic
CMOS	Complementary symmetry metal-oxide semiconductor
CSSC	Central-synchronous system clock
DUT	Device under test
FB	FutureBus (device identifier for backplane transceiver logic devices)
GND	Ground
GTLP	Gunning transceiver logic plus
I/O	Input/output
LVTTL	Low-voltage transistor-transistor logic with 3.3-V supply, compatible with TTL
PCB	Printed circuit board
Slew rate	Slew rate, which is derived using the following equation: slew rate = $\Delta V/\Delta t = (0.8\ V_{OH} - V_{OL})/t_{r,f}$
SSSC	Source-synchronous system clock
TTL	Transistor-transistor logic
t_{pd}	Propagation delay time
t_f	Time to transit from logical high to logical low, measured between the 90% and 10% values of the steady logical-high level
t_r	Time to transit from logical low to logical high, measured between the 10% and 90% values of the steady logical-high level
Transceiver	Trans(mitter) (re)ceiver, bidirectional device
V_{CC}	Supply voltage

7 Bibliography

Electronic Industries Alliance

Definition of Skew Specifications for Standard Logic Devices, EIA/JESD65, September 1998.

Interference Control Technologies, Inc.

Donald R. J. White, *EMI Control in the Design of Printed Circuit Boards and Backplanes*.

Texas Instruments Incorporated

G. Becke, E. Haseloff, *Das TTL-Kochbuch (The TTL Cookbook)*, SDYZG17.

PCB Design Guidelines for Reduced EMI, Application Report, November 1999, SZZA009.

AVC Logic Family Technology and Applications, August 1998, SCEA006A.

Comparison of Electrical and Thermal Parameters of Widebus™ SMD SSOP, TSSOP, TVSOP, and LFBGA Packages, October 1999, SCYA007.

Metastable Response in Digital Circuits, April 1995, SCBD002C.

Logic Selection Guide and Databook, CD-ROM, April 1998, SCBC001B.

Design Considerations for Logic Products, Application Book, [Volume 1], 1997, SDYA002.

Design Considerations for Logic Products, Application Book, Volume 2, September 1999, SDYA018.

Design Considerations for Logic Products, Application Book, Volume 3, December 2000, SDYA019.

Digital Design Seminar Reference Manual, 1998, SDYDE01B.

What a Designer Should Know, November 1994, SDZAE03.

The Bergeron Method, Application Report, October 1996, SDYA014.

Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs, Application Report, August 1997, SCBA012A.

Live Insertion, Application Report, October 1996, SDYA012.

Thin Very Small-Outline Package (*TVSOP)*, Application Report, May 2001, SCBA009.

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