

# SN74LV4T125 Single Power Supply Quadruple Buffer Translator GATE With 3-State Output CMOS Logic Level Shifter

## 1 Features

- Single-Supply Voltage Translator at 5.0-V, 3.3-V, 2.5-V, and 1.8-V  $V_{CC}$
- Operating Range of 1.8 V to 5.5 V
- Up Translation
  - 1.2 V<sup>(1)</sup> to 1.8 V at 1.8-V  $V_{CC}$
  - 1.5 V<sup>(1)</sup> to 2.5 V at 2.5-V  $V_{CC}$
  - 1.8 V<sup>(1)</sup> to 3.3 V at 3.3-V  $V_{CC}$
  - 3.3 V to 5.0 V at 5.0-V  $V_{CC}$
- Down Translation
  - 3.3 V to 1.8 V at 1.8-V  $V_{CC}$
  - 3.3 V to 2.5 V at 2.5-V  $V_{CC}$
  - 5.0 V to 3.3 V at 3.3-V  $V_{CC}$
- Logic Output is Referenced to  $V_{CC}$
- Characterized up to 50 MHz at 3.3-V  $V_{CC}$
- 5.5 V Tolerance on Input Pins
- –40°C to 125°C Operating Temperature Range
- Pb-Free Packages Available: SC-70 (RGY)
  - 3.5 × 3.5 × 1 mm
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Supports Standard Logic Pinouts
- $I_{off}$  Support Partial-Power-Down Mode Operation
- CMOS Output B Compatible with AUP125, LVC125 <sup>1</sup>

## 2 Applications

- Tablet
- Smartphone
- Personal Computer
- Industrial Automotive

## 3 Description

SN74LV4T125 is a low-voltage CMOS buffer gate that operates at a wider voltage range for portable, telecom, industrial, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to match 1.8-V input logic at  $V_{CC} = 3.3$  V and can be used in 1.8 V to 3.3 V level-up translation. In addition, the 5-V tolerant input pins enable down translation (for example, 3.3 V to 2.5 V output at  $V_{CC} = 2.5$  V). The wide  $V_{CC}$  range of 1.8 V to 5.5 V allows the generation of desired output levels to connect to controllers or processors.

The SN74LV4T125 device is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

### Device Information

| PART NUMBER <sup>(1)</sup> | PACKAGE        | BODY SIZE (NOM)   |
|----------------------------|----------------|-------------------|
| SN74LV4T125                | PW (TSSOP, 14) | 5.00 mm x 4.40 mm |
|                            | RGY (VQFN, 14) | 3.50 mm x 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

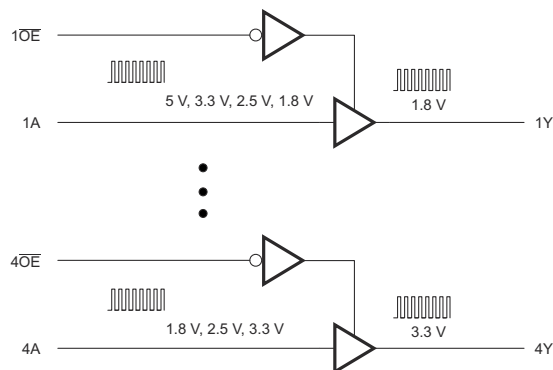


Figure 3-1. Simplified Application Diagram

<sup>1</sup> Refer the  $V_{IH}/V_{IL}$  and output drive for lower  $V_{CC}$  condition.



## Table of Contents

|  |    |  |    |
|--|----|--|----|
| <b>1 Features</b> .....                          | 1  | 8.2 Functional Block Diagram.....                                | 10 |
| <b>2 Applications</b> .....                      | 1  | 8.3 Feature Description.....                                     | 10 |
| <b>3 Description</b> .....                       | 1  | 8.4 Device Functional Modes.....                                 | 11 |
| <b>4 Revision History</b> .....                  | 2  | <b>9 Applications and Implementation</b> .....                   | 12 |
| <b>5 Pin Configuration and Functions</b> .....   | 3  | 9.1 Application Information.....                                 | 12 |
| Pin Functions.....                               | 3  | 9.2 Typical Application.....                                     | 12 |
| <b>6 Specifications</b> .....                    | 4  | <b>10 Power Supply Recommendations</b> .....                     | 13 |
| 6.1 Absolute Maximum Ratings.....                | 4  | <b>11 Layout</b> .....   | 14 |
| 6.2 ESD Ratings.....                             | 4  | 11.1 Layout Guidelines.....                                      | 14 |
| 6.3 Recommended Operating Conditions.....        | 5  | 11.2 Layout Example.....   | 14 |
| 6.4 Thermal Information.....                     | 5  | <b>12 Device and Documentation Support</b> .....                 | 15 |
| 6.5 Electrical Characteristics.....              | 6  | 12.1 Documentation Support.....                                  | 15 |
| 6.6 Switching Characteristics.....               | 7  | 12.2 Receiving Notification of Documentation Updates..           | 15 |
| 6.7 Noise Characteristics.....                   | 8  | 12.3 Support Resources.....                                      | 15 |
| 6.8 Operating Characteristics.....               | 8  | 12.4 Trademarks.....   | 15 |
| 6.9 Typical Characteristics.....                 | 8  | 12.5 Electrostatic Discharge Caution.....                        | 15 |
| <b>7 Parameter Measurement Information</b> ..... | 9  | 12.6 Glossary.....   | 15 |
| <b>8 Detailed Description</b> .....              | 10 | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | 15 |
| 8.1 Overview.....                                | 10 |  |    |

## 4 Revision History

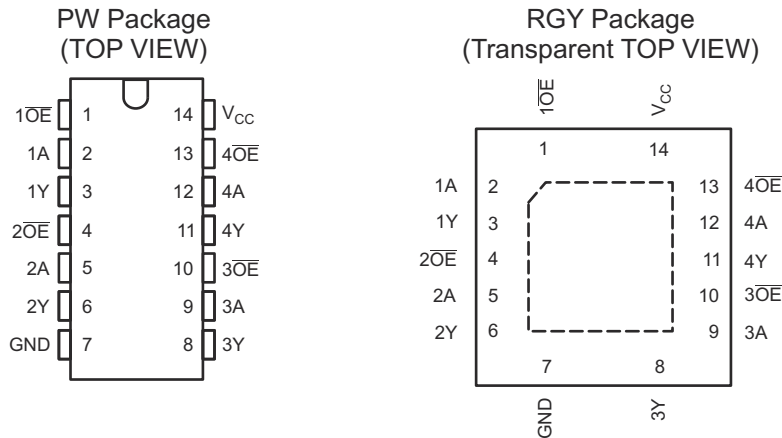
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision B (March 2014) to Revision C (June 2022)</b>  | <b>Page</b> |
|--|-------------|
| • I <sub>off</sub> Support Partial-Power-Down Mode Operation to Features.....  | 1           |
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....                  | 1           |
| • Added ESD Ratings table, Receiving Notification of Documentation Updates section, and Support Resources section..... | 1           |

| <b>Changes from Revision A (March 2014) to Revision B (September 2014)</b>  | <b>Page</b> |
|---|-------------|
| • Updated Features. ....  | 1           |
| • Updated Pin Functions table. ....   | 3           |
| • Added ESD Ratings table, Thermal Information table, Typical Characteristics section, Pin Configuration and Functions section, Detailed Description section, Power Supply Recommendations section, Layout section, Receiving Notification of Documentation Updates section, and Community Resources section..... | 4           |
| • Updated Detailed Design Procedure section. ....   | 13          |

| <b>Changes from Revision * (February 2014) to Revision A (March 2014)</b> | <b>Page</b> |
|---|-------------|
| • Updated 1 page preview document to full version. ....                   | 1           |

## 5 Pin Configuration and Functions



## Pin Functions

| PIN |                   | TYPE (1) | DESCRIPTION |
|-----|-------------------|----------|-------------|
| NO. | NAME              |          |             |
| 1   | 1 $\overline{OE}$ | I        | Enable 1    |
| 2   | 1A                | I        | Input 1     |
| 3   | 1Y                | O        | Output 1    |
| 4   | 2 $\overline{OE}$ | I        | Enable 2    |
| 5   | 2A                | I        | Input 2     |
| 6   | 2Y                | O        | Output 2    |
| 7   | GND               | —        | Ground Pin  |
| 8   | 3Y                | O        | Output 3    |
| 9   | 3A                | I        | Input 3     |
| 10  | 3 $\overline{OE}$ | I        | Enable 3    |
| 11  | 4Y                | O        | Output 4    |
| 12  | 4A                | I        | Input 4     |
| 13  | 4 $\overline{OE}$ | I        | Enable 4    |
| 14  | V <sub>CC</sub>   | —        | Power Pin   |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN  | MAX                   | UNIT |    |
|------------------|---|--|-----------------------|------|----|
| V <sub>CC</sub>  | Supply voltage range  | -0.5   | 7.0                   | V    |    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>  | -0.5   | 7.0                   | V    |    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5   | 4.6                   | V    |    |
|                  | Voltage range applied to any output in the high or low state <sup>(2)</sup>                 | -0.5   | V <sub>CC</sub> + 0.5 |      |    |
| I <sub>IK</sub>  | Input clamp current   | V <sub>I</sub> < 0                                     | -20                   | mA   |    |
| I <sub>OK</sub>  | Output clamp current  | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> | ±50                   | mA   |    |
| I <sub>O</sub>   | Continuous output current   |  | ±35                   | mA   |    |
|                  | Continuous current through V <sub>CC</sub> or GND   |  | ±70                   | mA   |    |
| T <sub>J</sub>   | Junction temperature  |  | 150                   | °C   |    |
| T <sub>stg</sub> | Storage temperature   |  | -65                   | 150  | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

|                    |                         | VALUE   | UNIT |
|--------------------|-------------------------|---|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | V    |
|                    |                         | Machine Model (MM), per JEDEC specification                           |      |
|                    |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | MIN                              | MAX | UNIT            |      |
|-----------------|------------------------------------|----------------------------------|-----|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     | 1.6                              | 5.5 | V               |      |
| V <sub>I</sub>  | Input voltage                      | 0                                | 5.5 | V               |      |
| V <sub>O</sub>  | Output voltage                     | High or Low State                | 0   | V <sub>CC</sub> | V    |
|                 |                                    | H-Z                              | 0   | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.8 V          |     | -3              | mA   |
|                 |                                    | V <sub>CC</sub> = 2.5 V          |     | -5              |      |
|                 |                                    | V <sub>CC</sub> = 3.3 V          |     | -8              |      |
|                 |                                    | V <sub>CC</sub> = 5.0 V          |     | -16             |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.8 V          |     | 3               | mA   |
|                 |                                    | V <sub>CC</sub> = 2.5 V          |     | 5               |      |
|                 |                                    | V <sub>CC</sub> = 3.3 V          |     | 8               |      |
|                 |                                    | V <sub>CC</sub> = 5.0 V          |     | 16              |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.6 V to 2.0 V |     | 20              | ns/V |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |     | 20              |      |
|                 |                                    | V <sub>CC</sub> = 3 V or 3.6 V   |     | 20              |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.0 V |     | 20              |      |
| T <sub>A</sub>  | Operating free-air temperature     | -40                              | 125 | °C              |      |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | SN74LV4T125                                  |         | UNIT |      |
|-------------------------------|--|---------|------|------|
|                               | PW   | RGY     |      |      |
|                               | 14 PINS                                      | 14 PINS |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 126.9   | 52.9 | °C/W |
| R <sub>θJctop</sub>           | Junction-to-case (top) thermal resistance    | 54.2    | 67.8 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 68.6    | 29.0 |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 7.5     | 2.6  |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 68.0    | 29.1 |      |
| R <sub>θJcbot</sub>           | Junction-to-case (bottom) thermal resistance | —       | 9.3  |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                 | V <sub>CC</sub>   | T <sub>A</sub> = 25°C                             |                       |      | T <sub>A</sub> = -40°C to 125°C |                       | UNIT |    |
|-------------------------|---|---|---|-----------------------|------|---------------------------------|-----------------------|------|----|
|                         |   |   | MIN   | TYP                   | MAX  | MIN                             | MAX                   |      |    |
| V <sub>IH</sub>         | High-level input voltage                        | V <sub>CC</sub> = 1.65 V to 1.9 V   | 0.95  |                       |      | 1                               |                       | V    |    |
|                         |   | V <sub>CC</sub> = 2.3 V to 2.7 V  | 1.1   |                       |      | 1.2                             |                       |      |    |
|                         |   | V <sub>CC</sub> = 3 V to 3.6 V  | 1.3   |                       |      | 1.35                            |                       |      |    |
|                         |   | V <sub>CC</sub> = 4.5 V to 5.0 V  | 2   |                       |      | 2                               |                       |      |    |
| V <sub>IL</sub>         | Low-level input voltage                         | V <sub>CC</sub> = 1.65 V to 1.9 V   |   |                       |      | 0.55                            |                       | V    |    |
|                         |   | V <sub>CC</sub> = 2.3 V to 2.77 V   |   |                       |      | 0.7                             |                       |      |    |
|                         |   | V <sub>CC</sub> = 3 V to 3.6 V  |   |                       |      | 0.85                            |                       |      |    |
|                         |   | V <sub>CC</sub> = 4.5 V to 5.5 V  |   |                       |      | 0.9                             |                       |      |    |
| V <sub>OH</sub>         | High-level output voltage                       | I <sub>OH</sub> = -50 μA  | V <sub>CC</sub> = 1.65 V to 5.5 V                 | V <sub>CC</sub> - 0.1 |      |                                 | V <sub>CC</sub> - 0.1 |      | V  |
|                         |   | I <sub>OH</sub> = -2 mA   | V <sub>CC</sub> = 1.65 V                          | 1.4                   |      |                                 | 1.35                  |      | V  |
|                         |   | I <sub>OH</sub> = -3 mA   | V <sub>CC</sub> = 2.3 V                           | 2.05                  |      |                                 | 2.0                   |      | V  |
|                         |   | I <sub>OH</sub> = -5 mA   | V <sub>CC</sub> = 3.0 V                           | 2.7                   |      |                                 | 2.6                   |      | V  |
|                         |   | I <sub>OH</sub> = -8 mA   |   | 2.6                   |      |                                 | 2.5                   |      |    |
|                         |   | I <sub>OH</sub> = -8 mA   | V <sub>CC</sub> = 4.5 V                           | 3.7                   |      |                                 | 3.6                   |      | V  |
|                         |   | I <sub>OH</sub> = -16 mA  |   | 3.8                   |      |                                 | 3.7                   |      |    |
|                         |   | I <sub>OH</sub> = -16 mA  | V <sub>CC</sub> = 5.0 V                           | 4.4                   |      |                                 | 4.3                   |      | V  |
| V <sub>OL</sub>         | Low-level output voltage                        | I <sub>OL</sub> = 50 μA   | V <sub>CC</sub> = 1.65 V to 5.5 V                 |                       |      |                                 | 0.1                   |      | V  |
|                         |   | I <sub>OH</sub> = 2 mA  | V <sub>CC</sub> = 1.65 V                          |                       |      |                                 | 0.1                   |      | V  |
|                         |   |   | V <sub>CC</sub> = 1.8 V                           |                       |      |                                 | 0.3                   |      |    |
|                         |   | I <sub>OH</sub> = 3 mA  | V <sub>CC</sub> = 2.3 V                           |                       |      |                                 | 0.2                   |      | V  |
|                         |   |   | V <sub>CC</sub> = 2.5 V                           |                       |      |                                 | 0.25                  |      |    |
|                         |   | I <sub>OH</sub> = 5 mA  | V <sub>CC</sub> = 3.0 V                           |                       |      |                                 | 0.35                  |      | V  |
|                         |   |   |   |                       |      |                                 | 0.4                   |      |    |
|                         |   | I <sub>OH</sub> = 8 mA  | V <sub>CC</sub> = 3.3 V                           |                       |      |                                 | 0.45                  |      | V  |
|                         |   |   |   |                       |      |                                 | 0.5                   |      |    |
|                         |   | I <sub>OH</sub> = 8 mA  | V <sub>CC</sub> = 4.5 V                           |                       |      |                                 | 0.50                  |      | V  |
|                         |   |   |   | 0.55                  |      |                                 |                       |      |    |
| I <sub>OH</sub> = 16 mA | V <sub>CC</sub> = 5.0 V                         |   |   |                       | 0.55 |                                 | V                     |      |    |
|                         |   |   |   |                       | 0.55 |                                 |                       |      |    |
| I <sub>I</sub>          | Input leakage current                           | V <sub>I</sub> = 0 V or V <sub>CC</sub>   | V <sub>CC</sub> = 0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V | ±0.1                  |      |                                 | ±1                    |      | μA |
| I <sub>CC</sub>         | Static supply current                           | V <sub>I</sub> = 0 V or V <sub>CC</sub> ,<br>I <sub>O</sub> = 0; open on loading            | V <sub>CC</sub> = 5.0 V                           | 2                     |      |                                 | 20                    |      | μA |
|                         |   |   | V <sub>CC</sub> = 3.3 V                           | 2                     |      |                                 | 20                    |      |    |
|                         |   |   | V <sub>CC</sub> = 2.5 V                           | 2                     |      |                                 | 20                    |      |    |
|                         |   |   | V <sub>CC</sub> = 1.8 V                           | 2                     |      |                                 | 20                    |      |    |
| ΔI <sub>CC</sub>        | Additional static supply current                | One input at 0.3 V or 3.4 V<br>Other inputs at 0 or V <sub>CC</sub> ,<br>I <sub>O</sub> = 0 | V <sub>CC</sub> = 5.5 V                           |                       |      |                                 | 1.35                  |      | μA |
|                         |   | One input at 0.3 V or 1.1 V<br>Other inputs at 0 or V <sub>CC</sub> ,<br>I <sub>O</sub> = 0 | V <sub>CC</sub> = 1.8 V                           |                       |      |                                 | 1.5                   |      |    |
| I <sub>OZ</sub>         | Off-state (High Impedance State) Output Current | V <sub>O</sub> = V <sub>CC</sub> or GND   | V <sub>CC</sub> = 5.5 V                           | ±0.25                 |      |                                 | ±2.5                  |      | μA |
| I <sub>off</sub>        | Partial power down current                      | V <sub>O</sub> or V <sub>I</sub> = 0 to 5.5 V   | V <sub>CC</sub> = 0 V                             | 0.5                   |      |                                 | 5                     |      | μA |
| C <sub>i</sub>          | Input capacitance                               | V <sub>I</sub> = V <sub>CC</sub> or GND   | V <sub>CC</sub> = 3.3 V                           | 1.6                   |      |                                 | 1.6                   |      | pF |
| C <sub>o</sub>          | Output capacitance                              | V <sub>O</sub> = V <sub>CC</sub> or GND   | V <sub>CC</sub> = 3.3 V                           | 4.8                   |      |                                 | 4.8                   |      | pF |

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | FREQUENCY (TYP) | V <sub>CC</sub> | C <sub>L</sub> | T <sub>A</sub> = 25°C |     |      | T <sub>A</sub> = -65°C to 125°C |     |     | UNIT |
|------------------|-----------------|-------------|-----------------|-----------------|----------------|-----------------------|-----|------|---------------------------------|-----|-----|------|
|                  |                 |             |                 |                 |                | MIN                   | TYP | MAX  | MIN                             | TYP | MAX |      |
| t <sub>pd</sub>  | Any In          | Y           | DC to 50 MHz    | 5.0 V           | 15 pF          | 2.8                   | 3.2 | 3    | 3.5                             | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 3                     | 3.5 | 3    | 4.5                             |     |     |      |
|                  |                 |             |                 | 3.3 V           | 15 pF          | 4                     | 4.5 | 5    | 5.5                             |     |     |      |
|                  |                 |             |                 |                 | 30 pF          | 5                     | 5.5 | 5.5  | 6.5                             |     |     |      |
|                  |                 |             | DC to 50 MHz    | 2.5 V           | 15 pF          | 5.5                   | 6.5 | 7    | 7.5                             | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 6.5                   | 7   | 7.5  | 8.5                             |     |     |      |
| DC to 30 MHz     | 1.8 V           | 15 pF       | 10              | 11              | 11             | 12                    | ns  |      |                                 |     |     |      |
|                  |                 | 30 pF       | 11              | 12              | 12.5           | 13                    |     |      |                                 |     |     |      |
| t <sub>pZH</sub> | $\overline{OE}$ | Y           | DC to 50 MHz    | 5.0 V           | 15 pF          | 3.5                   | 4   | 3.5  | 4                               | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 3.8                   | 4.2 | 4    | 4.5                             |     |     |      |
|                  |                 |             |                 | 3.3 V           | 15 pF          | 5                     | 5.8 | 5.8  | 6.1                             |     |     |      |
|                  |                 |             |                 |                 | 30 pF          | 5.5                   | 6   | 5.7  | 6.5                             |     |     |      |
|                  |                 |             | DC to 50 MHz    | 2.5 V           | 15 pF          | 7.5                   | 8   | 8.5  | 9                               | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 8                     | 8.5 | 9    | 9.5                             |     |     |      |
| DC to 30 MHz     | 1.8 V           | 15 pF       | 14.5            | 15              | 15.5           | 16.5                  | ns  |      |                                 |     |     |      |
|                  |                 | 30 pF       | 15.5            | 16              | 16             | 17                    |     |      |                                 |     |     |      |
| t <sub>pZL</sub> | $\overline{OE}$ | Y           | DC to 50 MHz    | 5.0 V           | 15 pF          | 3                     | 3.5 | 3.5  | 4                               | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 3.5                   | 4   | 4    | 4.5                             |     |     |      |
|                  |                 |             |                 | 3.3 V           | 15 pF          | 5.3                   | 5.6 | 6    | 6.2                             |     |     |      |
|                  |                 |             |                 |                 | 30 pF          | 5.8                   | 6.2 | 7    | 7.5                             |     |     |      |
|                  |                 |             | DC to 50 MHz    | 2.5 V           | 15 pF          | 8                     | 8.5 | 9    | 9.5                             | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 9                     | 9.5 | 10.5 | 11                              |     |     |      |
| DC to 30 MHz     | 1.8 V           | 15 pF       | 17              | 17.5            | 18             | 18.5                  | ns  |      |                                 |     |     |      |
|                  |                 | 30 pF       | 18              | 18.5            | 19             | 20                    |     |      |                                 |     |     |      |
| t <sub>pHZ</sub> | $\overline{OE}$ | Y           | DC to 50 MHz    | 5.0 V           | 15 pF          | 3                     | 3.5 | 3.5  | 4                               | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 3.5                   | 4   | 4    | 4.5                             |     |     |      |
|                  |                 |             |                 | 3.3 V           | 15 pF          | 3.5                   | 4   | 4.5  | 5                               |     |     |      |
|                  |                 |             |                 |                 | 30 pF          | 5                     | 6   | 6.5  | 7                               |     |     |      |
|                  |                 |             | DC to 50 MHz    | 2.5 V           | 15 pF          | 5.5                   | 6   | 6    | 6.5                             | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 7.5                   | 8   | 8    | 9                               |     |     |      |
| DC to 30 MHz     | 1.8 V           | 15 pF       | 7.5             | 8               | 8              | 8.5                   | ns  |      |                                 |     |     |      |
|                  |                 | 30 pF       | 11              | 12              | 12             | 13                    |     |      |                                 |     |     |      |
| t <sub>PLZ</sub> | $\overline{OE}$ | Y           | DC to 50 MHz    | 5.0 V           | 15 pF          | 2                     | 2.5 | 2    | 2.7                             | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 2                     | 3   | 2    | 3.2                             |     |     |      |
|                  |                 |             |                 | 3.3 V           | 15 pF          | 2.3                   | 2.8 | 2.5  | 3.2                             |     |     |      |
|                  |                 |             |                 |                 | 30 pF          | 2.8                   | 3.2 | 3.3  | 4                               |     |     |      |
|                  |                 |             | DC to 50 MHz    | 2.5 V           | 15 pF          | 3.3                   | 3.8 | 3.8  | 4.2                             | ns  |     |      |
|                  |                 |             |                 |                 | 30 pF          | 4                     | 4.3 | 4.2  | 5                               |     |     |      |
| DC to 30 MHz     | 1.8 V           | 15 pF       | 5               | 5.5             | 5              | 5.7                   | ns  |      |                                 |     |     |      |
|                  |                 | 30 pF       | 6.5             | 7               | 7              | 8.5                   |     |      |                                 |     |     |      |
| t <sub>sk</sub>  | Any In          | Y           | DC to 50 MHz    | 5.0 V to 2.5 V  | 15 pF          |                       |     | 1    | 1                               | ns  |     |      |
|                  |                 |             | DC to 30 MHz    | 1.8 V           | 15 pF          |                       |     |      |                                 |     |     |      |

## 6.7 Noise Characteristics

 $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}^{(1)}$ 

| PARAMETER   |  | MIN  | TYP  | MAX  | UNIT |
|-------------|--|------|------|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |      | 0.4  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |      | -0.3 | -0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |      | 3    |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31 |      |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |      |      | 0.99 | V    |

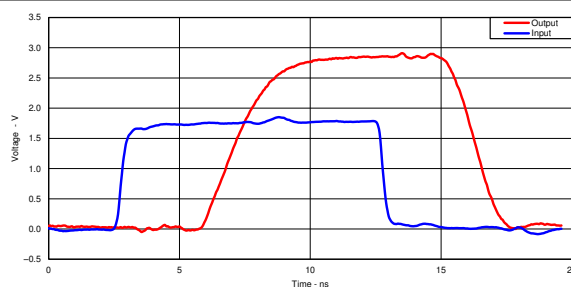
(1) Characteristics are for surface-mount packages only.

## 6.8 Operating Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

| PARAMETER |                               | TEST CONDITIONS                            | TYP | UNIT |
|-----------|-------------------------------|--|-----|------|
| $C_{pd}$  | Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 16  | pF   |

## 6.9 Typical Characteristics

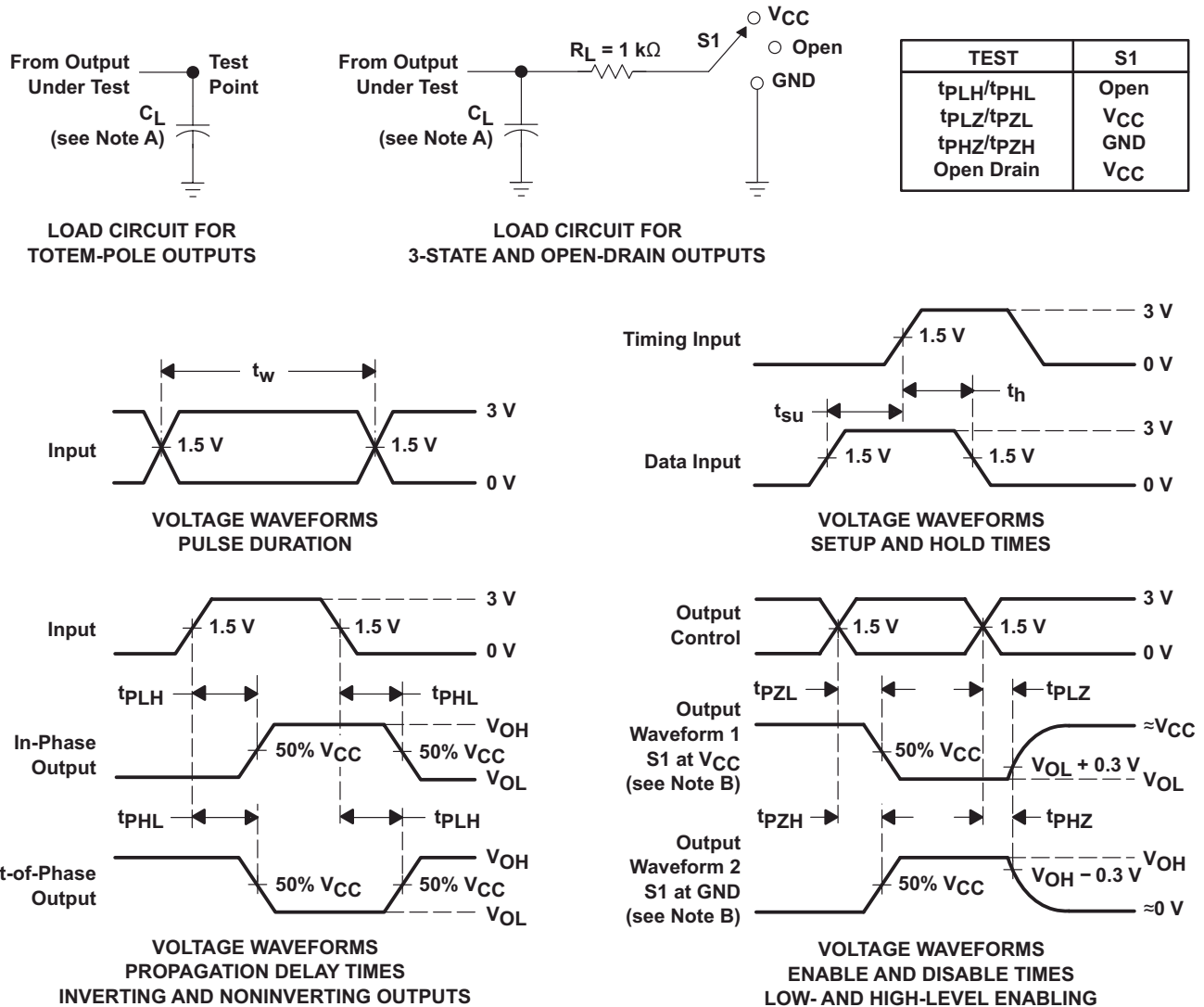


**Figure 6-1. Switching Characteristics at 50 MHz**  
Excellent Signal Integrity (1.8 V to 3.3 V at 3.3-V  $V_{CC}$ )



## 7 Parameter Measurement Information

### 7.1



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - The outputs are measured one at a time, with one input transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74LVxTxx family was created to allow up- or down-voltage translation with only one power rail. The family has over-voltage tolerant inputs that allow down translation from up to 5.5 V to the  $V_{CC}$  level that can be as low as 1.8 V. The family SN74LVxTxx also has a lowered switching threshold that allows it to translate up to the  $V_{CC}$  level that can be as high as 5.5 V.

#### 8.1.1 Translating Down

Using these parts to translate down is very simple. Because the inputs are tolerant to 5.5 V at any valid  $V_{CC}$ , they can be used to down translate. The input can be any level above  $V_{CC}$  up to 5.5 V and the output will equal the  $V_{CC}$  level, which can be as low as 1.8 V. One important advantage to down translating using this part is that the  $I_{CC}$  current will remain less than or equal to the specified value.

Down translation possibilities with SN74LVxTxx:

- With 1.8-V  $V_{CC}$  from 2.5 V, 3.3 V, or 5 V down to 1.8 V.
- With 2.5-V  $V_{CC}$  from 3.3 V or 5 V down to 2.5 V.
- With 3.3-V  $V_{CC}$  from 5 V down to 3.3 V.

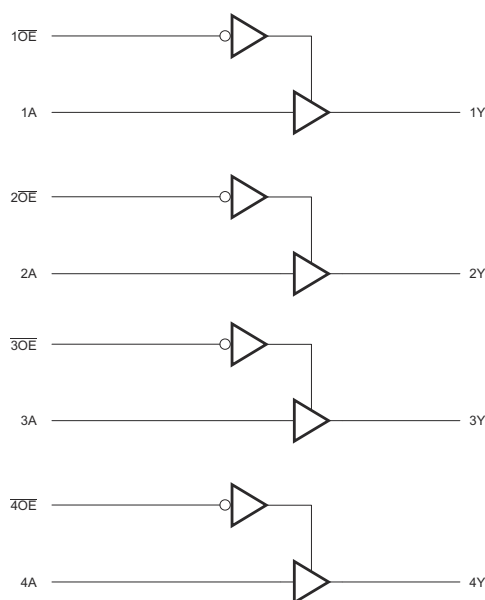
#### 8.1.2 Translating Up

Using the SN74LVxTxx family to translate up is very simple. The input switching threshold is lowered so the high level of the input voltage can be much lower than a typical CMOS  $V_{IH}$ . For instance, If the  $V_{CC}$  is 3.3 V then the typical CMOS switching threshold would be  $V_{CC} / 2$  or 1.65 V. This means the input high level must be at least  $V_{CC} \times 0.7$  or 2.31 V. On the LVxT devices the input threshold for 3.3-V  $V_{CC}$  is approximately 1 V. This allows a signal with a 1.8-V  $V_{IH}$  to be translated up to the  $V_{CC}$  level of 3.3 V.

Up translation possibilities with SN74LVxTxx:

- With 2.5-V  $V_{CC}$  from 1.8 V to 2.5 V.
- With 3.3-V  $V_{CC}$  from 1.8 V or 2.5 V to 3.3 V.
- With 5-V  $V_{CC}$  From 2.5 V or 3.3 V to 5 V.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

This part is a single supply buffer that is capable up or down translation. The output will equal  $V_{CC}$  while the input can vary from 1.2 V to 5.5 V.

**Up Translation Mode:**

- 1.2 V to 1.8 V at 1.8-V  $V_{CC}$
- 1.5 V to 2.5 V at 2.5-V  $V_{CC}$
- 1.8 V to 3.3 V at 3.3-V  $V_{CC}$
- 3.3 V to 5.0 V at 5.0-V  $V_{CC}$

**Down Translation Mode:**

- 3.3 V to 1.8 V at 1.8-V  $V_{CC}$
- 3.3 V to 2.5 V at 2.5-V  $V_{CC}$
- 5.0 V to 3.3 V at 3.3-V  $V_{CC}$

## 8.4 Device Functional Modes

This device performs the function of a buffer where input logic level equals the output logic level, while providing buffering and drive to the output. The SN74LV4T125 device will also translate voltages up or down while performing this function.

**Table 8-1. Function Table  
(Each Buffer)**

| INPUTS <sup>(1)</sup> |   | OUTPUT <sup>(2)</sup> |
|-----------------------|---|-----------------------|
| $\overline{OE}$       | A | Y                     |
| L                     | H | H                     |
| L                     | L | L                     |
| H                     | X | Z                     |

**Table 8-2. Supply  $V_{CC} = 3.3$  V**

| INPUT b<br>(Lower Level Input) |   | OUTPUT<br>( $V_{CC}$ CMOS) |
|--------------------------------|---|----------------------------|
| A                              | B | Y                          |
| $V_{IH}(\min) = 1.35$ V        |   | $V_{OH}(\min) = 2.9$ V     |
| $V_{IL}(\max) = 0.8$ V         |   | $V_{OL}(\max) = 0.2$ V     |

- (1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance  
(2) H = Driving High, L = Driving Low, Z = High Impedance State

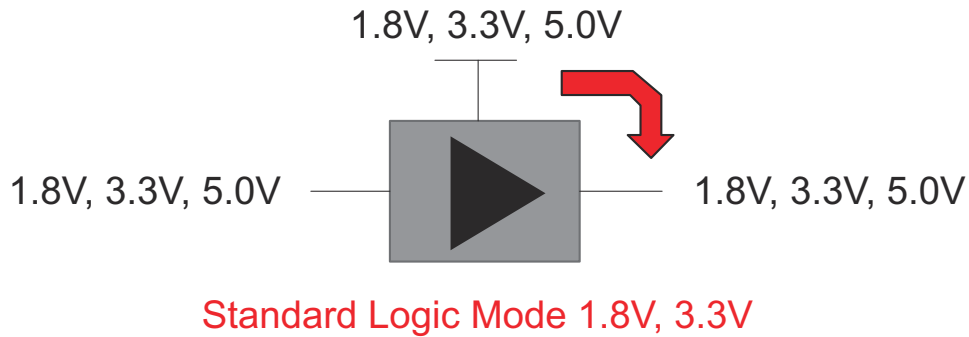
## 9 Applications and Implementation

### Note

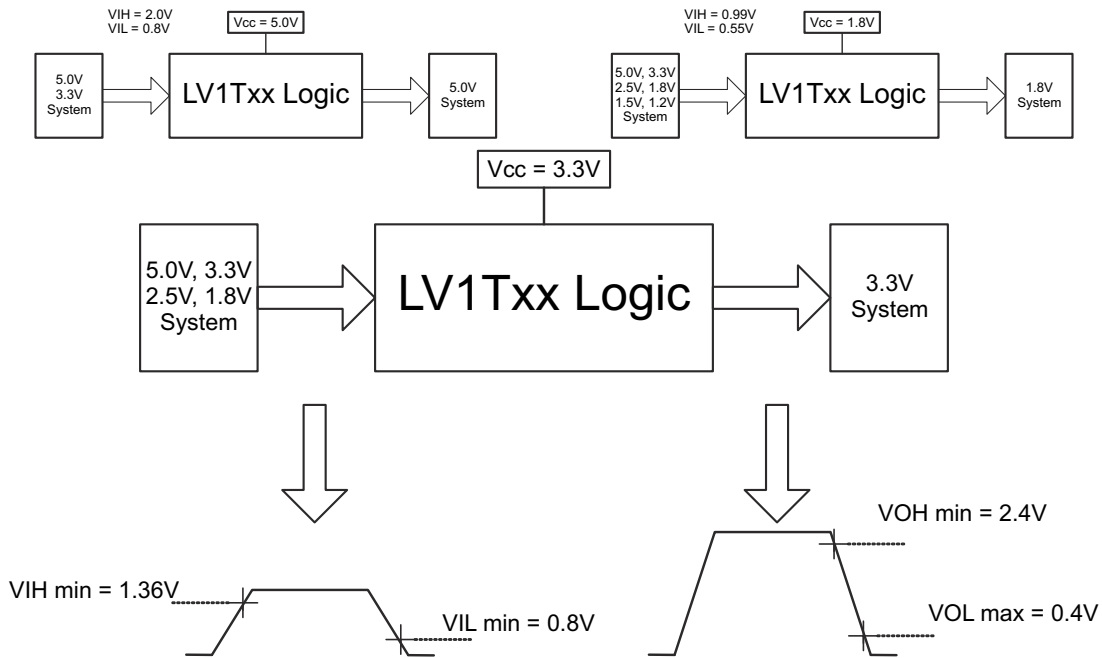
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

Based upon the lower-threshold circuit design of the LVxT family, the LVxT family also supports level translation. For level translation up and down, the LVxT family requires only a single power supply.



### 9.2 Typical Application



**Figure 9-1. Switching Thresholds for 1.8 V to 3.3 V Translation**

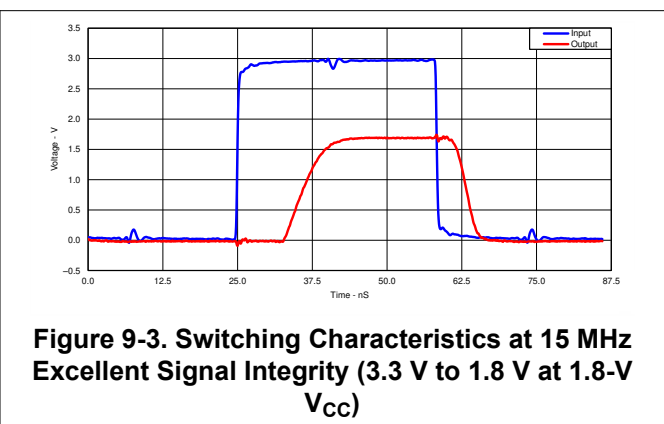
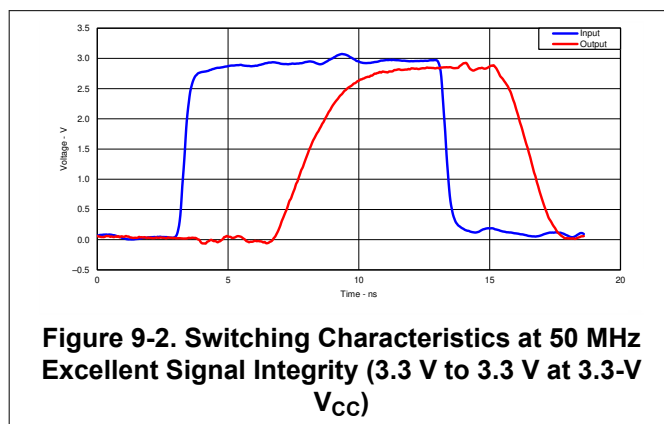
### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. The input threshold levels are lowered to allow for up translation. At 5 V the device has equivalent TTL input levels.

### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - Rise time and fall time specifications. See  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend output conditions:
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#).

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

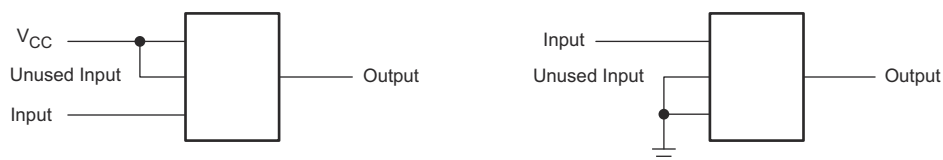
When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 11-1](#) are the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient.

It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

### 11.2 Layout Example



**Figure 11-1. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Additional Product Selection

| DEVICE      | PACKAGE       | DESCRIPTION                                    |
|-------------|---------------|--|
| SN74LV1T00  | DCK, DBV      | 2-Input Positive-NAND Gate                     |
| SN74LV1T02  | DCK, DBV      | 2-Input Positive-NOR Gate                      |
| SN74LV1T04  | DCK, DBV      | Inverter Gate                                  |
| SN74LV1T08  | DCK, DBV      | 2-Input Positive-AND Gate                      |
| SN74LV1T34  | DCK, DBV, DRL | Single Buffer Gate                             |
| SN74LV1T14  | DCK, DBV      | Single Schmitt-Trigger Inverter Gate           |
| SN74LV1T32  | DCK, DBV      | 2-Input Positive-OR Gate                       |
| SN74LV1T86  | DCK, DBV      | Single 2-Input Exclusive-Or Gate               |
| SN74LV1T125 | DCK, DBV, DRL | Single Buffer Gate with 3-state Output         |
| SN74LV1T126 | DCK, DBV, DRL | Single Buffer Gate with 3-state Output         |
| SN74LV4T125 | RGY, PW       | Quadruple Bus Buffer Gate With 3-State Outputs |

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV4T125PWR   | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | LV4T125                 | <a href="#">Samples</a> |
| SN74LV4T125RGYR  | ACTIVE        | VQFN         | RGY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | LVT125                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV4T125PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV4T125RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV4T125PWR  | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LV4T125RGYR | VQFN         | RGY             | 14   | 3000 | 356.0       | 356.0      | 35.0        |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - $\triangle F$  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

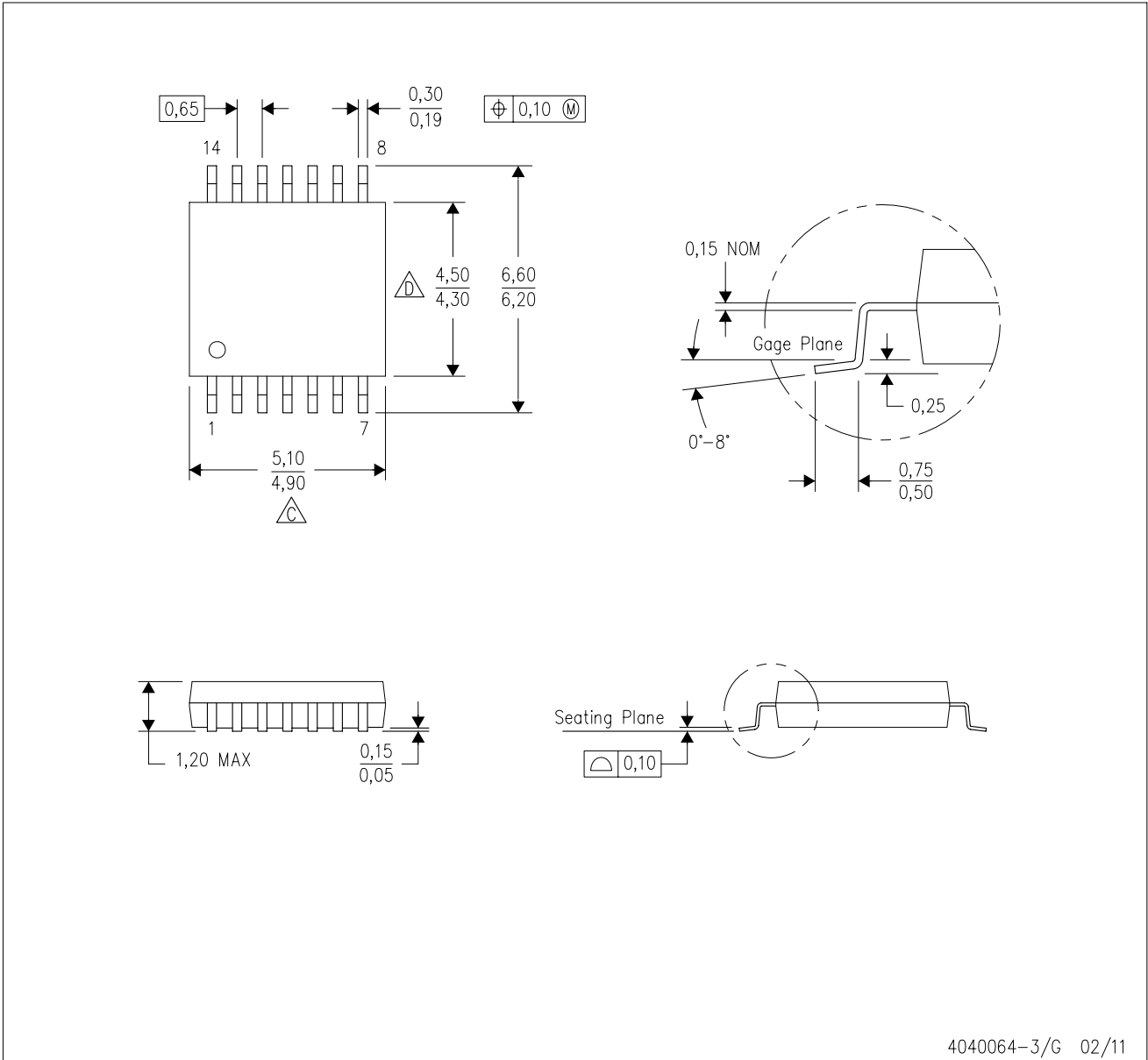


4208122-2/P 03/14



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated