SNx4LV594A 8-Bit Shift Registers With Output Registers

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Maximum tpd of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, TA = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Latch-up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- ECG Electrocardiograms
- Storage Servers
- EPOS, ECR, and Cash Drawers
- Servers and High-Performance Computing

3 Description

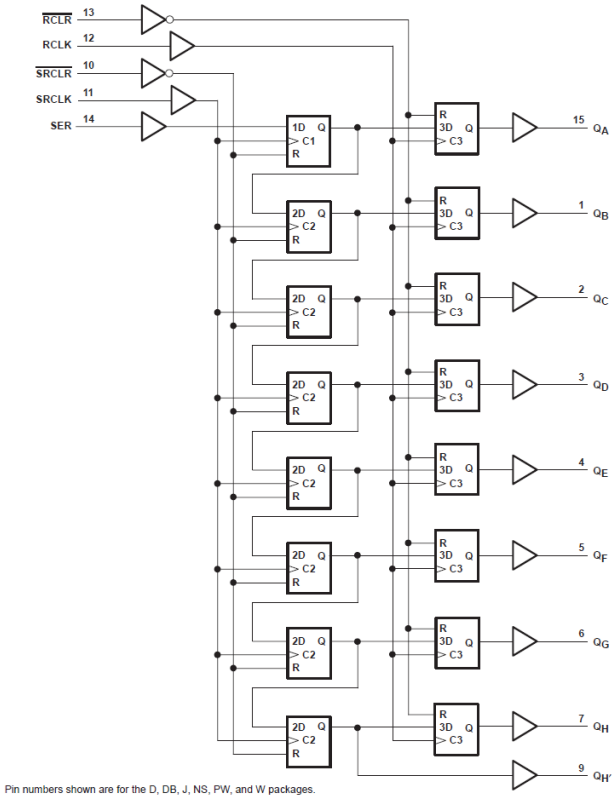
The SN74LV594A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV594A	SSOP (16)	6.20 mm × 5.30 mm
	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DB, J, NS, PW, and W packages.

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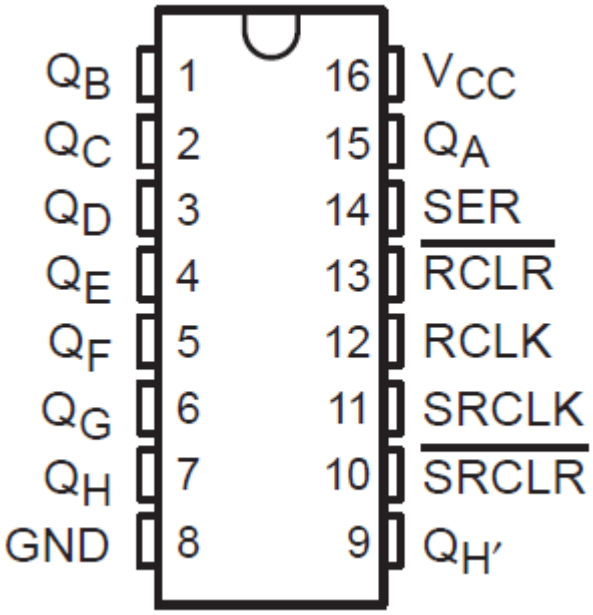
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2005) to Revision J	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D, DB, or PW Package
16-Pin SOIC, SSOP, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Q_B	O	Output B
2	Q_C	O	Output C
3	Q_D	O	Output D
4	Q_E	O	Output E
5	Q_F	O	Output F
6	Q_G	O	Output G
7	Q_H	O	Output H
8	GND	–	Ground pin
9	$Q_{H'}$	O	Q_H inverted
10	$\overline{SRCLR}$	I	Serial clear
11	SRCLK	I	Serial clock
12	RCLK	I	Storage clock
13	$\overline{RCLR}$	I	Storage clear
14	SER	I	Serial input
15	Q_A	O	Output A
16	Vcc	–	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
V_I	Input voltage (2)		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state (2)		−0.5	7	V
V_O	Output voltage (2) (3)		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0	−20		mA
I_{OK}	Output clamp current	V_O< 0	−50		mA
I_O	Continuous output current	V_O = 0 to V_{CC}	−25	25	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54LV594A(2)		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level input current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate V_{CC} = 2.3 V to 2.7 V V_{CC} = 3 V to 3.6 V V_{CC} = 4.5 V to 5.5 V			200		200	ns/V
				100		100	
				20		20	
T_A	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) Product Preview

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV594A			UNIT
		D (SOIC)	DB (SSOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	97.8	106.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	48.1	40.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	38	48.5	51.1	
ψ_{JT}	Junction-to-top characterization parameter	9	10	3.8	
ψ_{JB}	Junction-to-board characterization parameter	37.7	47.9	50.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	SN54LV594A			SN74LV594A –40°C TO 85°C			SN74LV594A –40°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH} = –2 µA	2.3 V	2			2			2			
	I_{OH} = –6 µA	3 V	2.48			2.48			2.48			
	I_{OH} = –12 µA	4.5 V	3.8			3.8			3.8			
V_{OL}	I_{OH} = –50 µA	2 V to 5.5 V			0.1			0.1			0.1	V
	I_{OH} = –2 µA	2.3 V			0.4			0.4			0.4	
	I_{OH} = –6 µA	3 V			0.44			0.44			0.44	
	I_{OH} = –12 µA	4.5 V			0.55			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1			±1	µA
I_{CC}	V_I = V_{CC} of GND, I_O = 0	5.5 V			20			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		3.5			3.5					pF

6.6 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted). See Figure 1.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54lv594A		SN74LV594A –40°C TO 85°C		SN74LV594A –40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	65(1)	80(1)		45(1)		45		35		MHz
			C_L = 50 pF	60	70		40		40		30		
t_{PLH}	SRCLK	Q_A – Q_H	C_L = 15 pF		6.4(1)	10.6(1)	1(1)	11.1(1)	1	11.1	1	12.5	ns
t_{PHL}					6.3(1)	10.4(1)	1(1)	11.1(1)	1	11.1	1	12.5	
t_{PLH}		$Q_{H'}$			7.4(1)	12.1(1)	1(1)	12.8(1)	1	12.8	1	15	
t_{PHL}	RCLK				7.2(1)	11.6(1)	1(1)	12.8(1)	1	12.8	1	15	
t_{PHL}		Q_A – Q_H			7.9(1)	12.7(1)	1(1)	13.6(1)	1	13.6	1	15.5	
		$Q_{H'}$			7.4(1)	11.9(1)	1(1)	13.1(1)	1	13.1	1	15.5	
t_{PLH}	$\overline{SRCLR}$	Q_A – Q_H	C_L = 50 pF		9.5	14.1	1	14.6	1	14.6	1	17	ns
t_{PHL}					10.8	15.5	1	17.2	1	17.2	1	19.5	
t_{PLH}		$Q_{H'}$			10.6	15.7	1	16.5	1	16.5	1	18.5	
t_{PHL}	$\overline{RCLR}$				11.3	16.1	1	18.6	1	18.6	1	20.5	
t_{PHL}		Q_A – Q_H			12.1	17.4	1	19	1	19	1	21	
		$Q_{H'}$			11.6	16.5	1	18.6	1	18.6	1	20.6	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted). See Figure 1.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV594A		SN74LV594A –40°C TO 85°C		SN74LV594A –40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80(1)	120(1)		70(1)		70		60		MHz
			C_L = 50 pF	55	105		50		50		40		
t_{PLH}	SRCLK	Q_A – Q_H	C_L = 15 pF		4.6(1)	8(1)	1(1)	8.5(1)	1	8.5	1	10.5	ns
t_{PHL}					4.9(1)	8.2(1)	1(1)	8.8(1)	1	8.8	1	10.5	
t_{PLH}		$Q_{H'}$			5.4(1)	9.1(1)	1(1)	9.7(1)	1	9.7	1	11.5	
t_{PHL}	RCLK				5.5(1)	9.2(1)	1(1)	9.9(1)	1	9.9	1	11.6	
t_{PHL}		Q_A – Q_H			6(1)	9.8(1)	1(1)	10.6(1)	1	10.6	1	12.1	
		$Q_{H'}$			5.6(1)	9.2(1)	1(1)	10(1)	1	10	1	12	
t_{PLH}	$\overline{SRCLR}$	Q_A – Q_H	C_L = 50 pF				1	11.1	1	11.1	1	12.5	ns
t_{PHL}							1	13.1	1	13.1	1	15	
t_{PLH}		$Q_{H'}$					1	12.4	1	12.4	1	14	
t_{PHL}	$\overline{RCLR}$						1	13.9	1	13.9	1	15.5	
t_{PHL}		Q_A – Q_H					1	14.4	1	14.4	1	16.1	
		$Q_{H'}$					1	14	1	14	1	16	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted). See Figure 1.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV594A		SN74LV594A –40°C TO 85°C		SN74LV594A –40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f_{max}			C_L = 15 pF	135(1)	170(1)		115(1)		115		105		MHz
			C_L = 50 pF	120	140		95		95		85		
t_{PLH}	SRCLK	Q_A – Q_H	C_L = 15 pF		3.3(1)	6.2(1)	1(1)	6.5(1)	1	6.5	1	8	ns
t_{PHL}					3.7(1)	6.5(1)	1(1)	6.9(1)	1	6.9	1	8.5	
t_{PLH}		$Q_{H'}$			3.7(1)	6.8(1)	1(1)	7.2(1)	1	7.2	1	8.5	
t_{PHL}	RCLK				4.1(1)	7.2(1)	1(1)	7.6(1)	1	7.6	1	9	
t_{PHL}		Q_A – Q_H			4.5(1)	7.6(1)	1(1)	8.2(1)	1	8.2	1	9.5	
		$Q_{H'}$			4.1(1)	7.1(1)	1(1)	7.6(1)	1	7.6	1	9	
t_{PLH}	$\overline{SRCLR}$	Q_A – Q_H	C_L = 50 pF		4.9	7.8	1	8.3	1	8.3	1	9.6	ns
t_{PHL}					5.8	8.9	1	9.7	1	9.7	1	11	
t_{PLH}		$Q_{H'}$			5.5	8.6	1	9.1	1	9.1	1	10.5	
t_{PHL}	$\overline{RCLR}$				6	9.2	1	10.1	1	10.1	1	11.5	
t_{PHL}		Q_A – Q_H			6.6	10	1	10.7	1	10.7	1	12	
		$Q_{H'}$			6	9.2	1	10.1	1	10.1	1	11.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Timing Requirements: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V. See Figure 1.

			T_A = 25°C		SN54LV594A		SN74LV594A –40°C TO 85°C		SN74LV594A –40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	7		7.5		7.5		8.5		ns
		$\overline{RCKR}$ or $\overline{SCRCLR}$ low	6		6.5		6.5		7.5		
t_{su}	Setup time	SER before SRCLK↑	5.5		5.5		5.5		6		ns
		SRCLK↑ before RCLK↑	8		9		9		10		
		$\overline{SCRCLR}$ low before RCLK↑ (1)	8.5		9.5		9.5		10.5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	6		6.8		6.8		7.5		
		$\overline{RCLK}$ high (inactive) before RCLK↑	6.7		7.6		7.6		8.5		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		1.5		2		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.10 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V. See Figure 1.

			T_A = 25°C		SN54LV594A		SN74LV594A –40°C TO 85°C		SN74LV594A –40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5.5		5.5		5.5		6.5		ns
		$\overline{RCKR}$ or $\overline{SCRCLR}$ low	5		5		5		6		
t_{su}	Setup time	SER before SRCLK↑	3.5		3.5		3.5		4		ns
		SRCLK↑ before RCLK↑	8		8.5		8.5		9.5		
		$\overline{SCRCLR}$ low before RCLK↑ (1)	8		9		9		10		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	4.2		4.8		4.8		5.5		
		$\overline{RCLK}$ high (inactive) before RCLK↑	4.6		5.3		5.3		6		
t_h	Hold time	SER after SRCLK↑	1.5		1.5		1.5		2		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.11 Timing Requirements: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V. See Figure 1.

			T_A = 25°C		SN54LV594A		SN74LV594A –40°C TO 85°C		SN74LV594A –40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5		5		5		6		ns
		$\overline{RCKR}$ or $\overline{SCRCLR}$ low	5.2		5.2		5.2		6.2		
t_{su}	Setup time	SER before SRCLK↑	3		3		3		3.5		ns
		SRCLK↑ before RCLK↑	5		5		5		6		
		$\overline{SCRCLR}$ low before RCLK↑(1)	5		5		5		5.5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2.9		3.3		3.3		4		
		$\overline{RCLK}$ high (inactive) before RCLK↑	3.2		3.7		3.7		4.5		
t_h	Hold time	SER after SRCLK↑	2		2		2		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.12 Noise Characteristics(1)

over operating free-air temperature range (unless otherwise noted), V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(V)}$	High-level dynamic input voltage	2.31			V
$V_{IL(V)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	3.3 V	93	pF
			5 V	112	

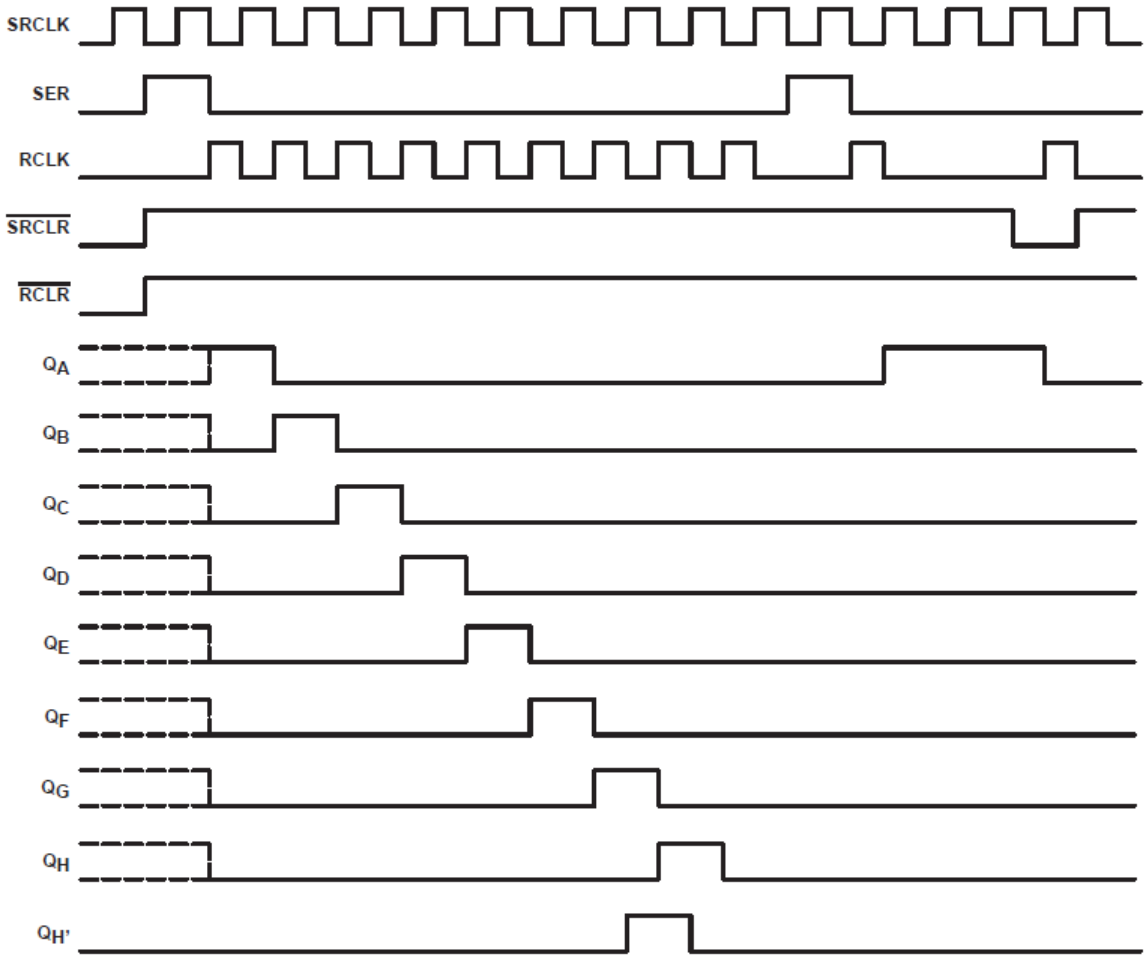


Figure 1. Timing Diagram

6.14 Typical Characteristics

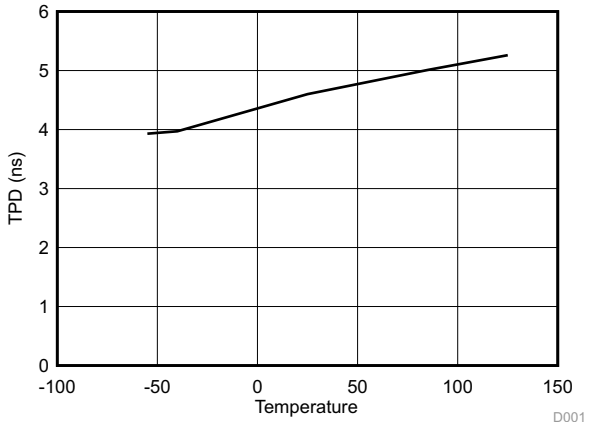


Figure 2. TPD vs. Temperature at 3.3 V

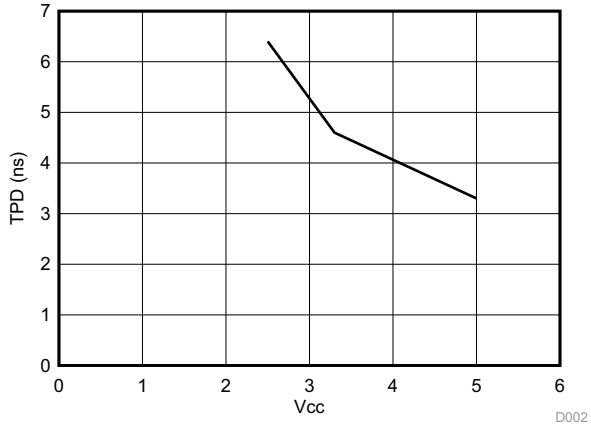
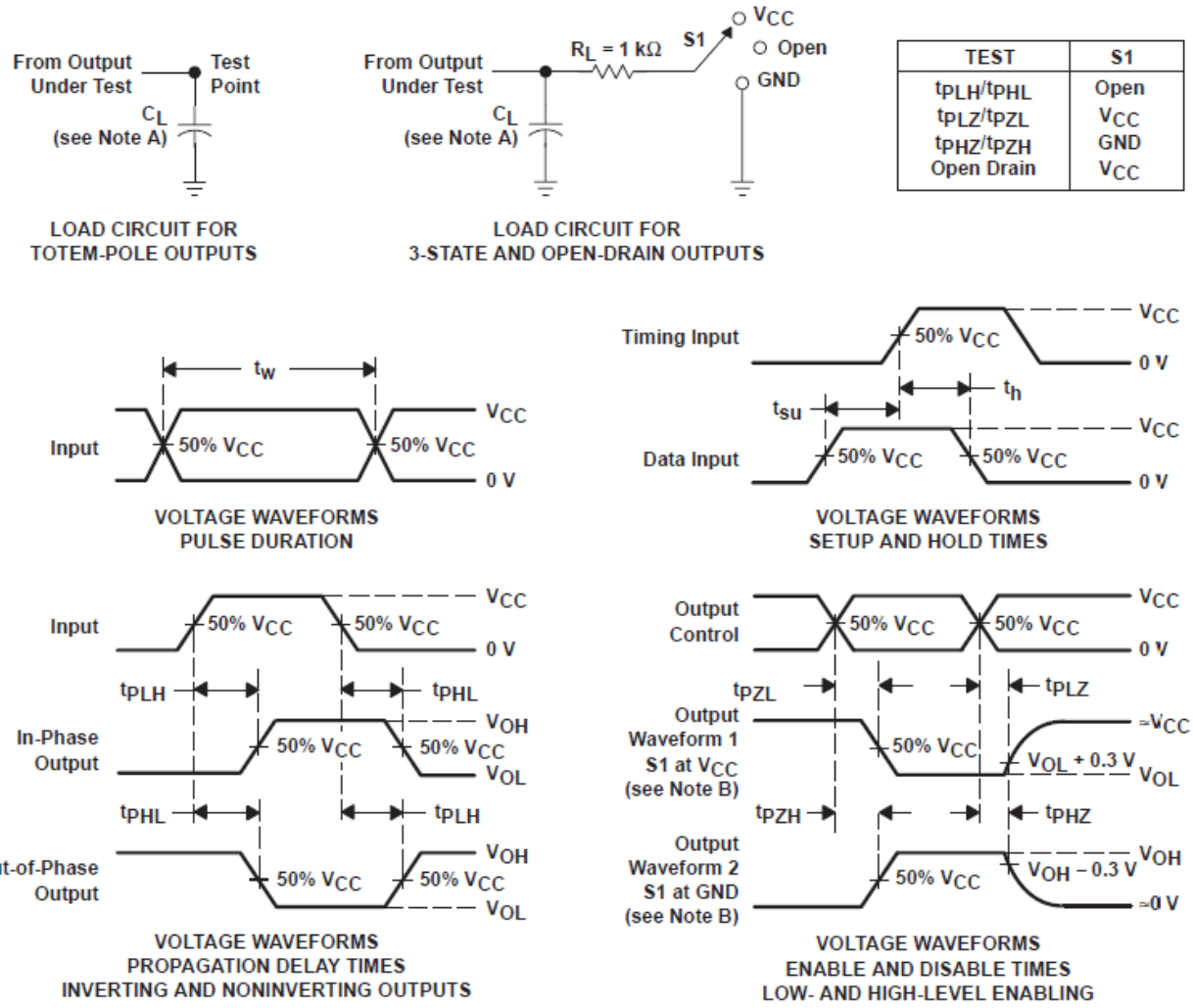


Figure 3. TPD vs. Vcc at 25°C

7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

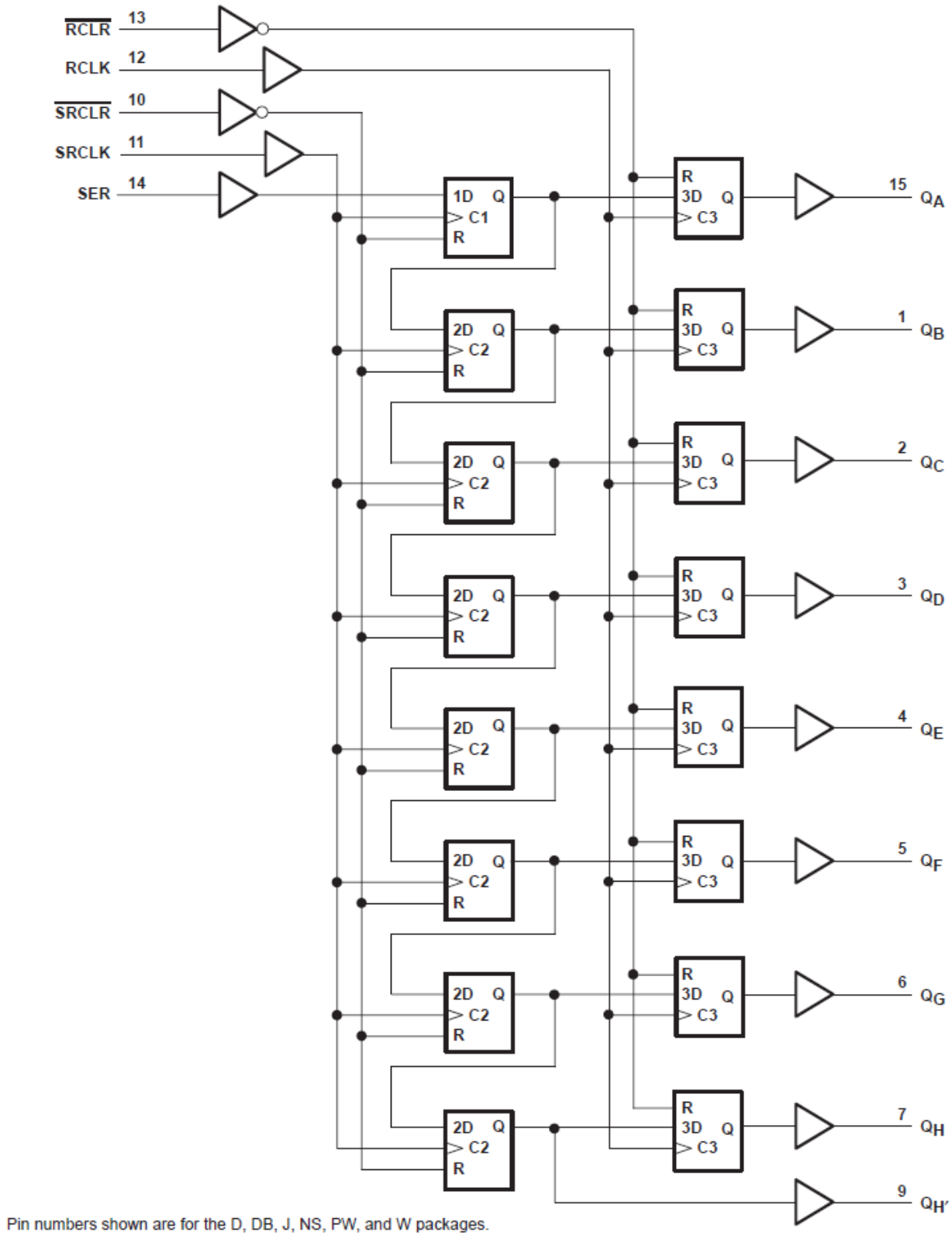
8 Detailed Description

8.1 Overview

The SN74LV594A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on the shift and storage registers. A serial output ($Q_{H'}$) is provided for cascading purposes. The shift-register (SRCLK) and storage-register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, NS, PW, and W packages.

Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

Table 1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, repectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV594A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

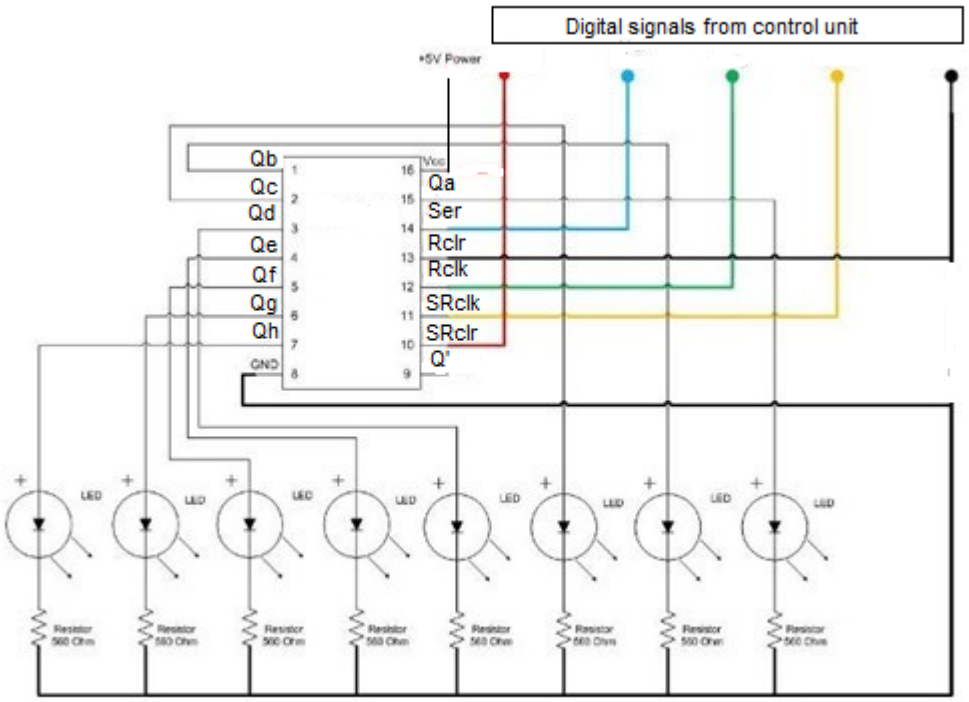


Figure 6. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs. See (Δt/ΔV) in *Recommended Operating Conditions*.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

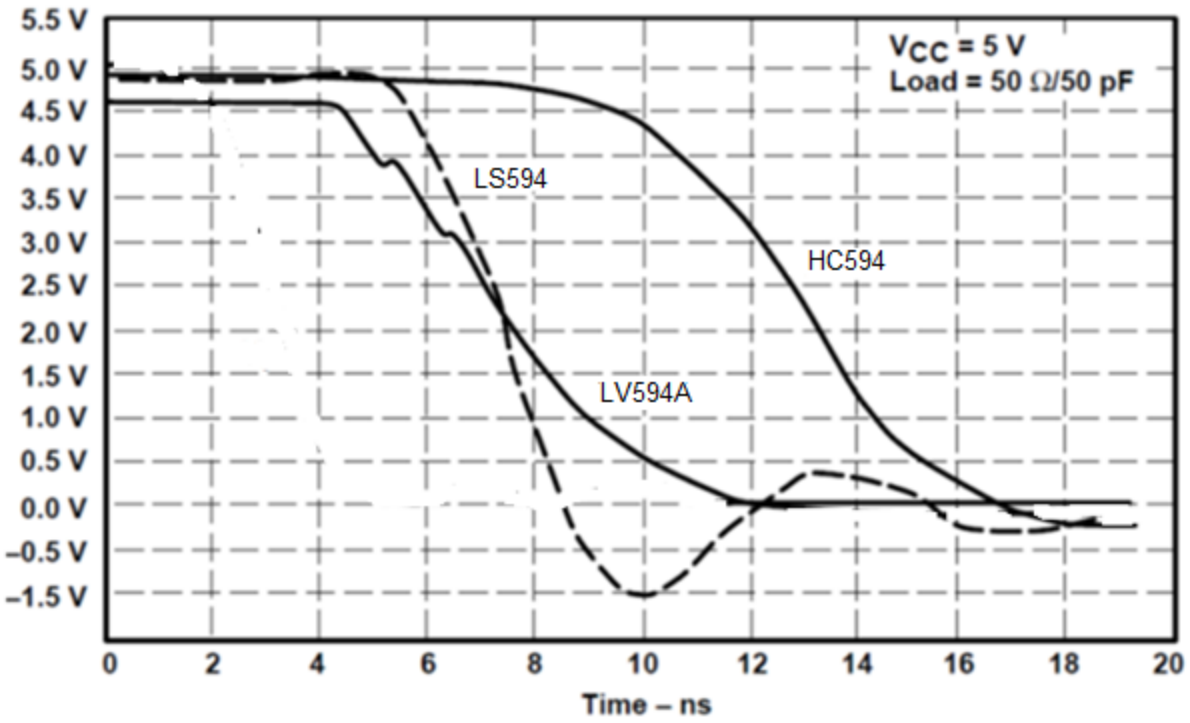


Figure 7. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

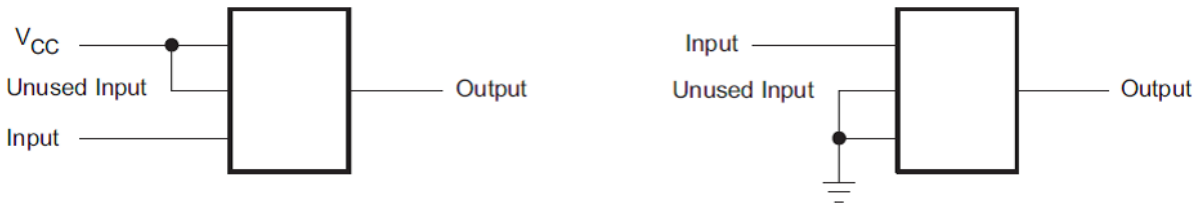


Figure 8. Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV594AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594ADE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594ADG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594ADRG4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125		Samples
SN74LV594APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594APWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594APWRE4	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
SN74LV594APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594APWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples
SN74LV594APWTG4	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV594A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

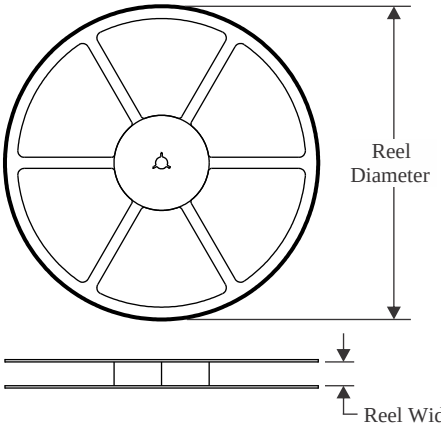
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

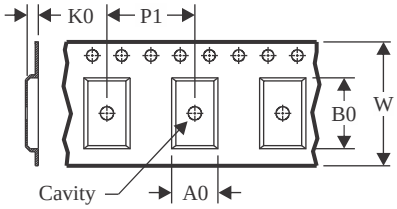
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

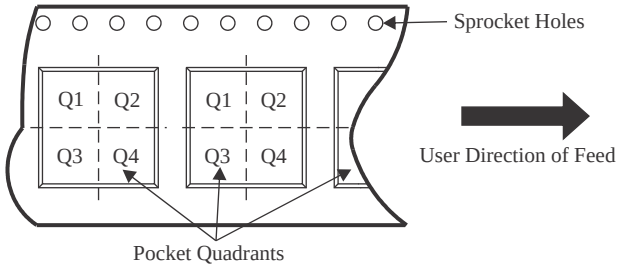


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

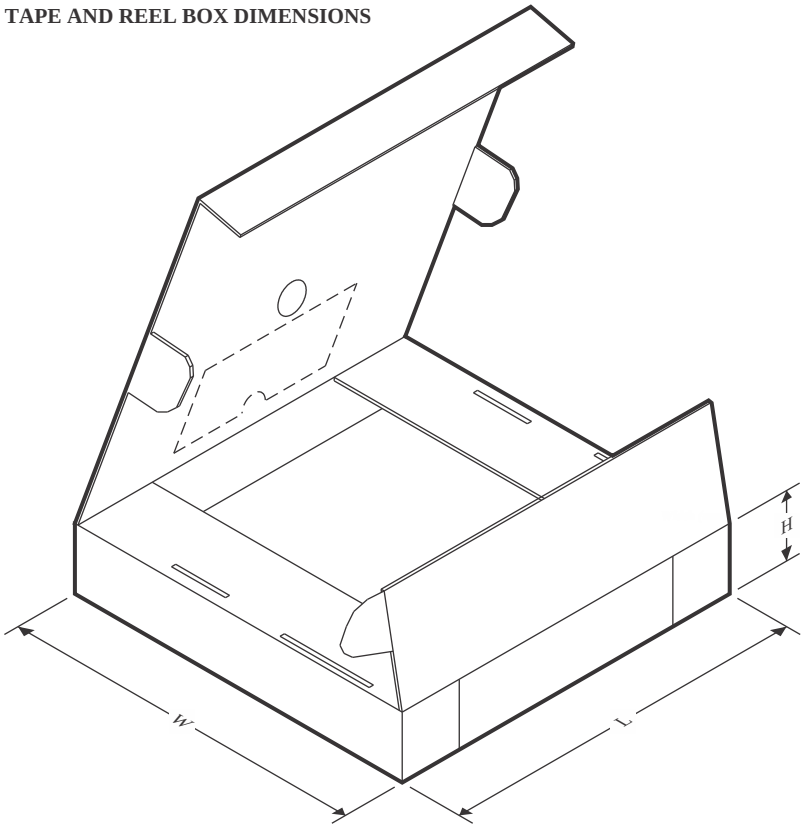
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV594ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV594ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV594APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV594APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV594APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV594APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

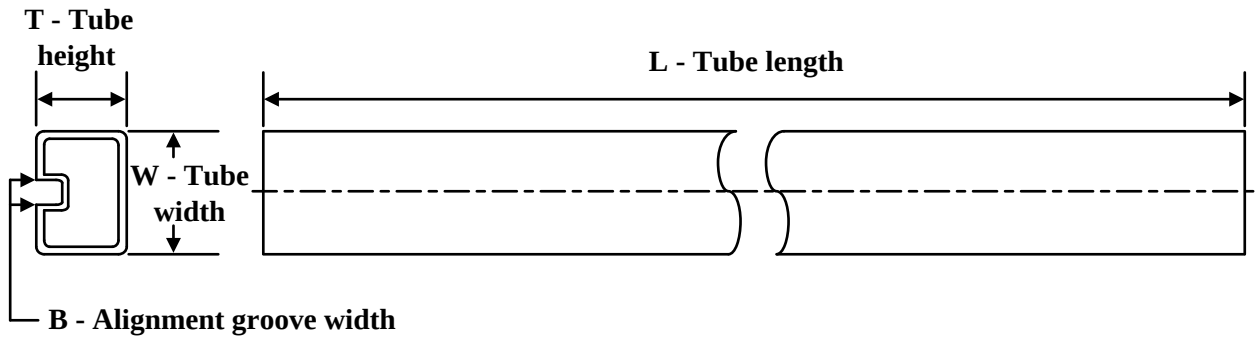
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV594ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LV594ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV594APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV594APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV594APWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV594APWT	TSSOP	PW	16	250	356.0	356.0	35.0

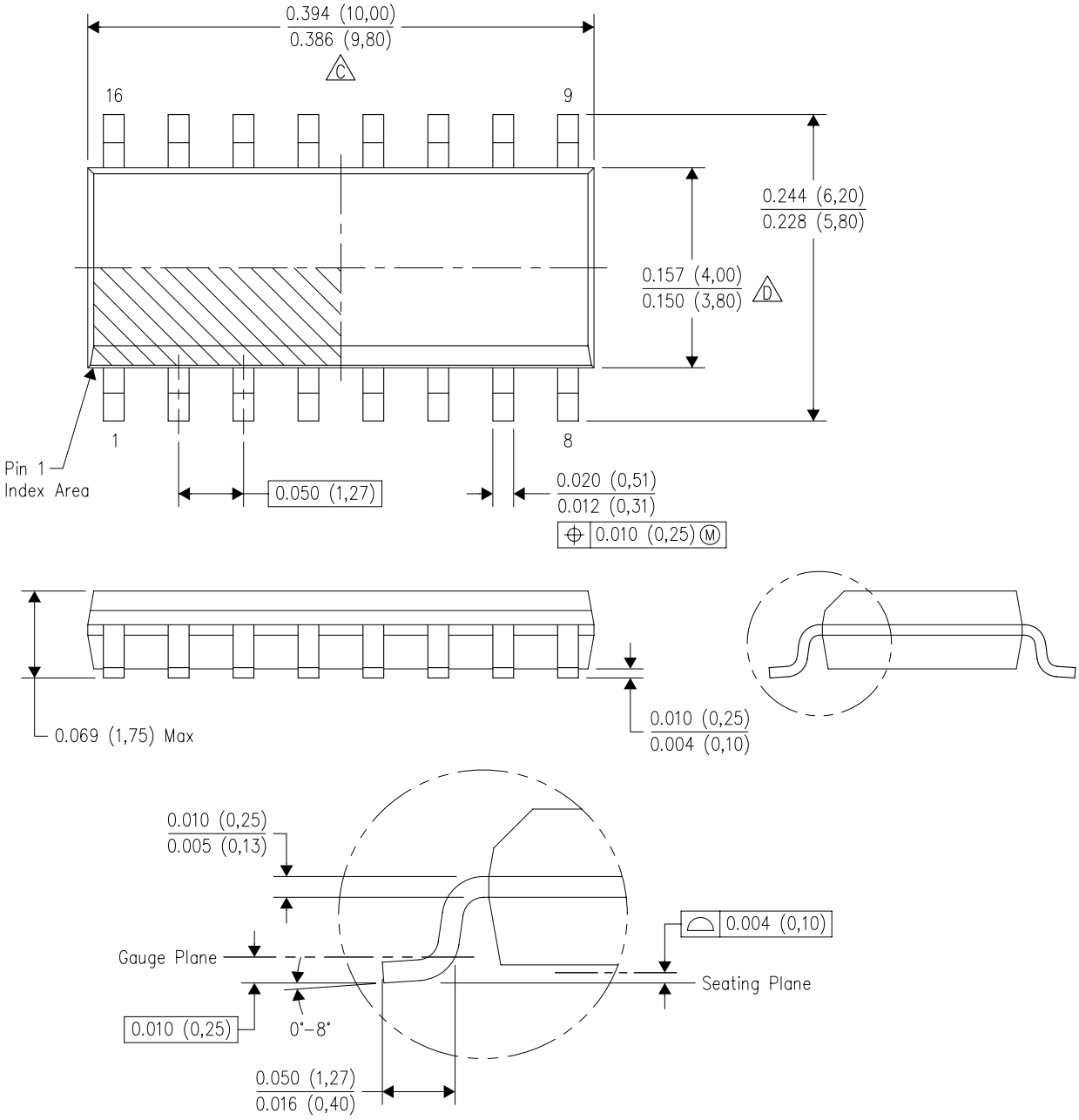
TUBE



*All dimensions are nominal

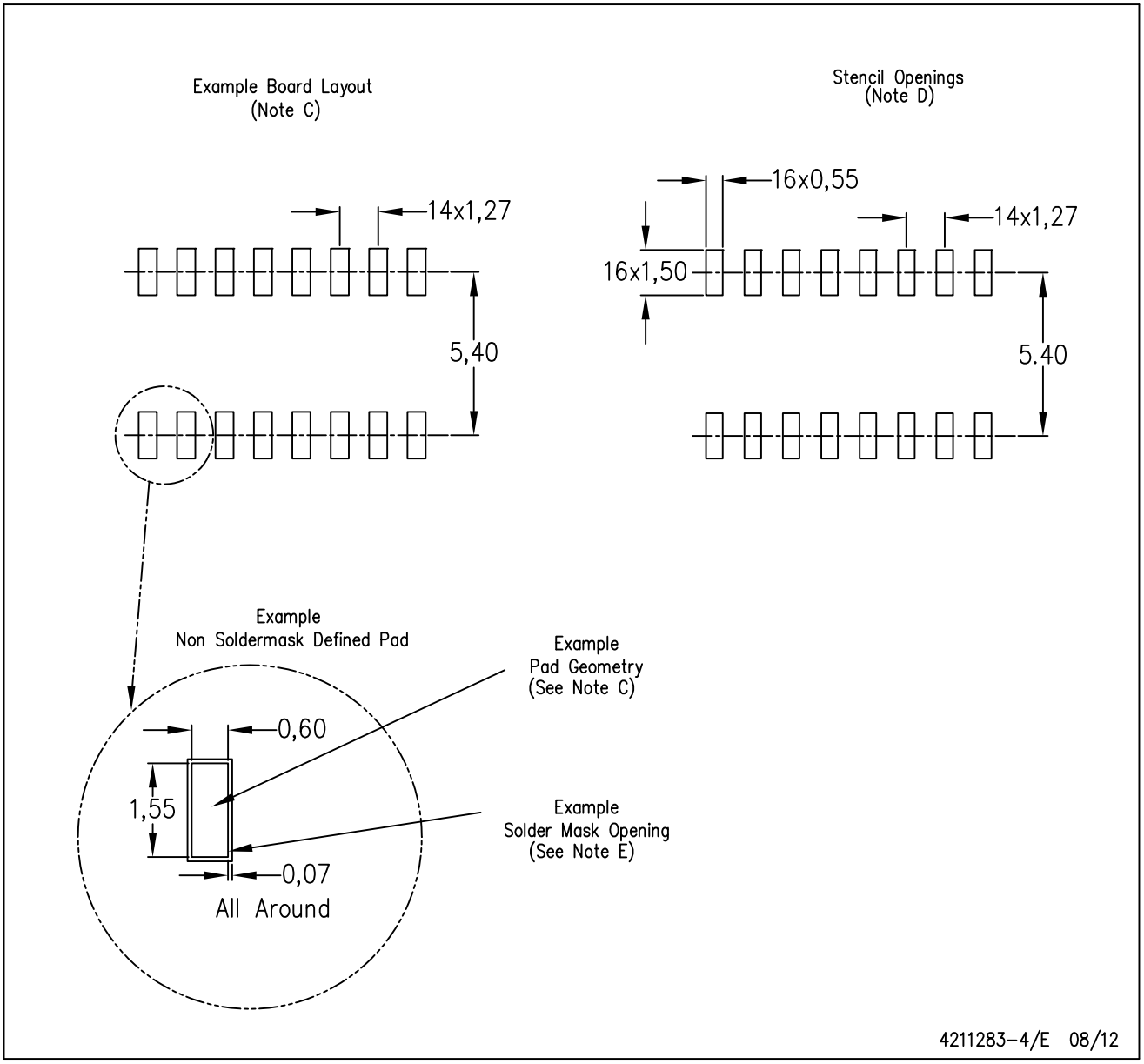
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV594AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV594ADE4	D	SOIC	16	40	507	8	3940	4.32
SN74LV594ADG4	D	SOIC	16	40	507	8	3940	4.32
SN74LV594APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV594APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



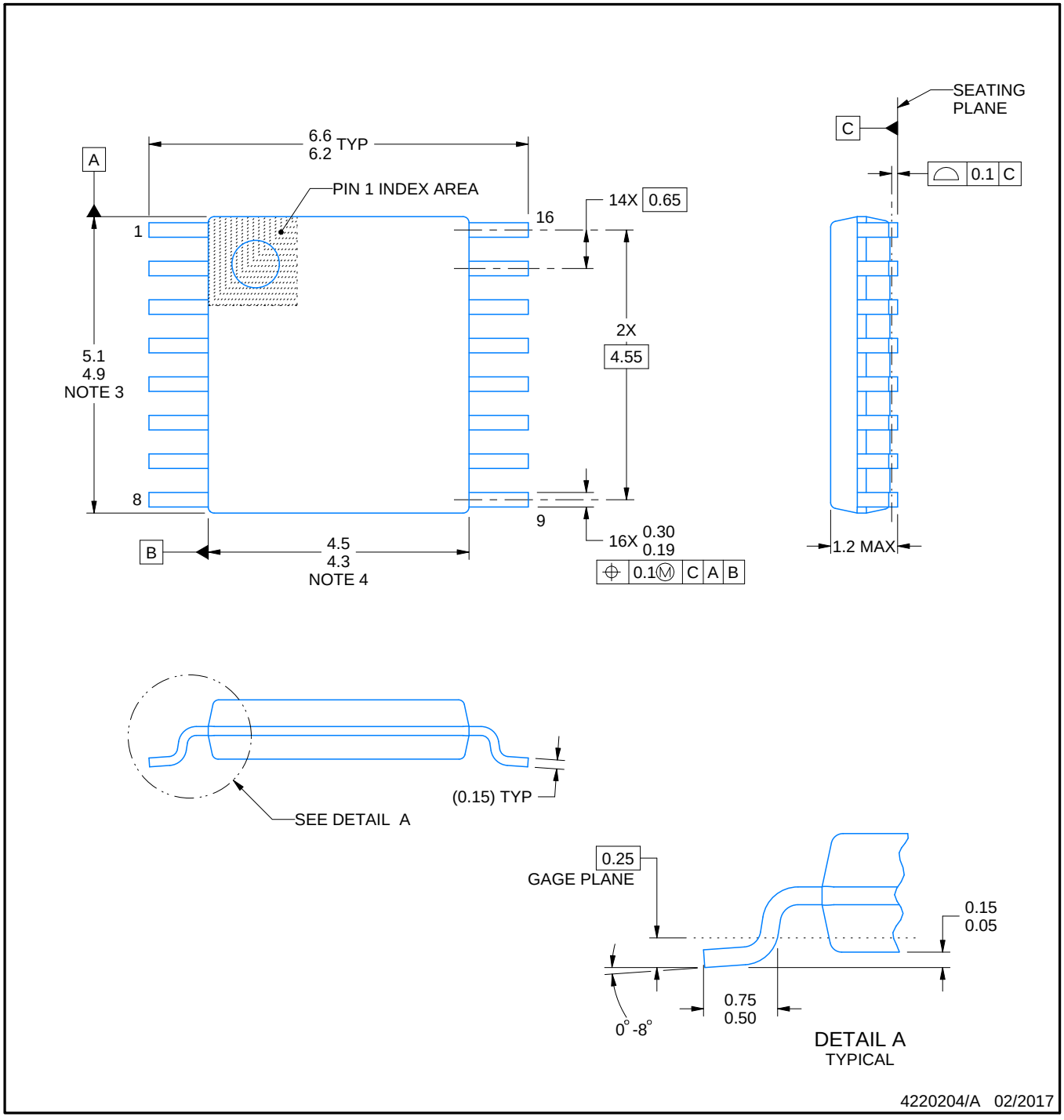
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

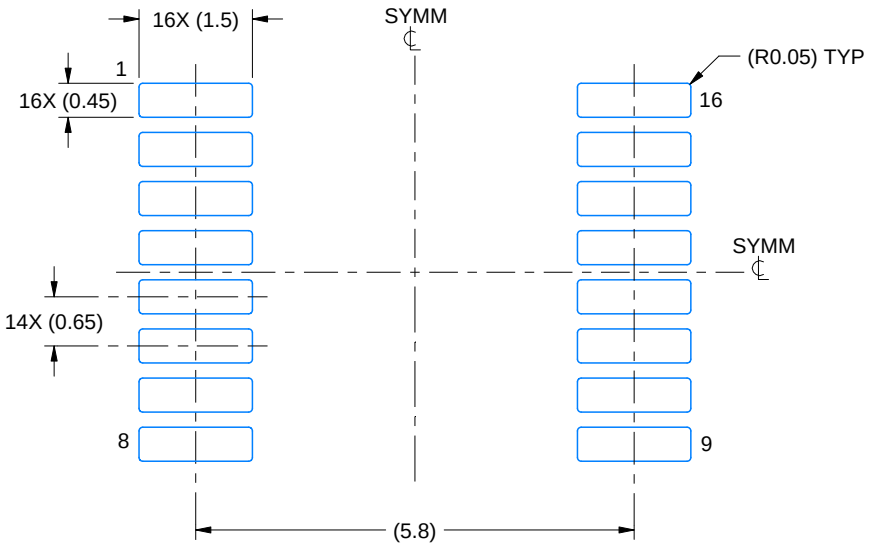
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

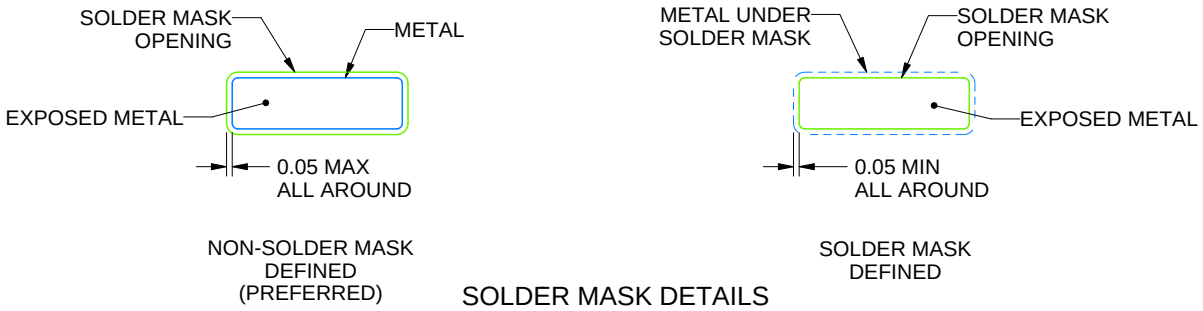


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

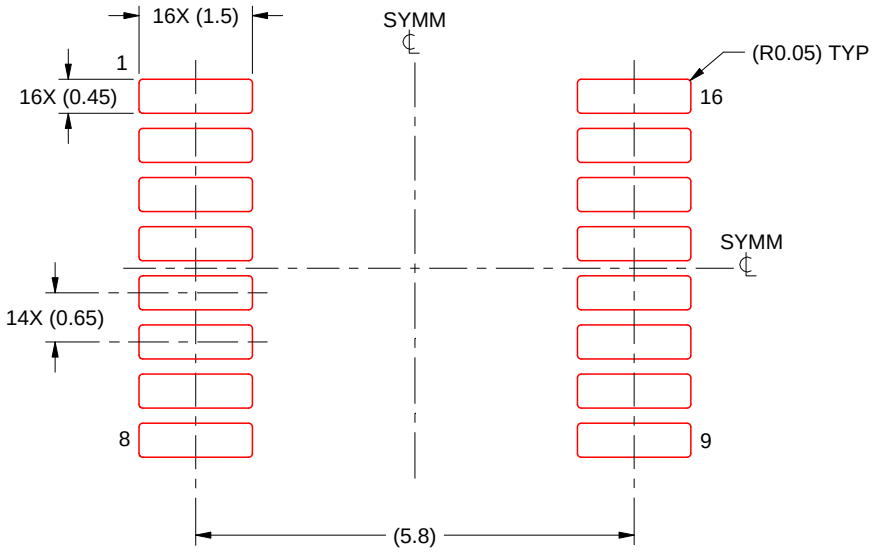


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

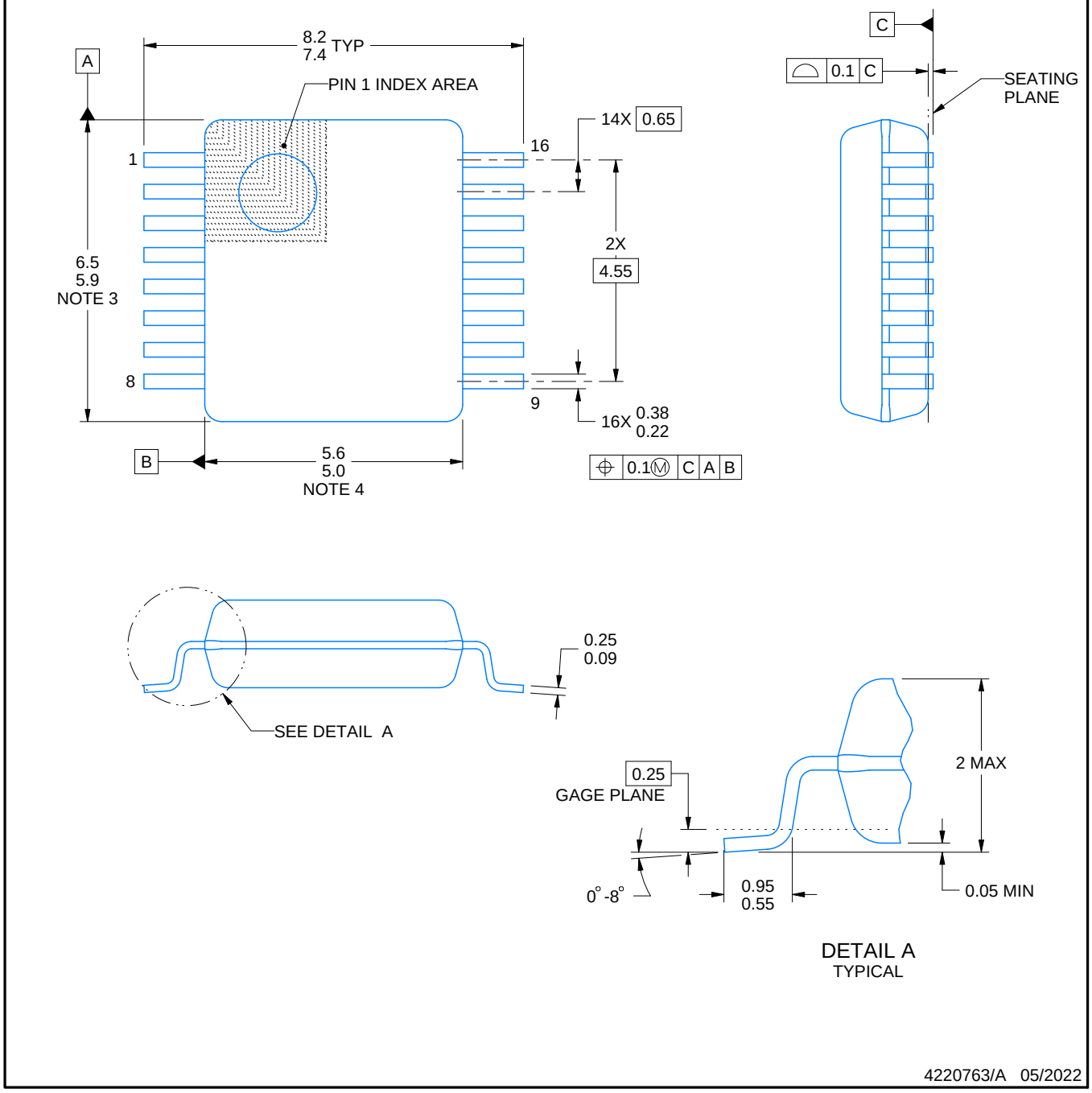
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

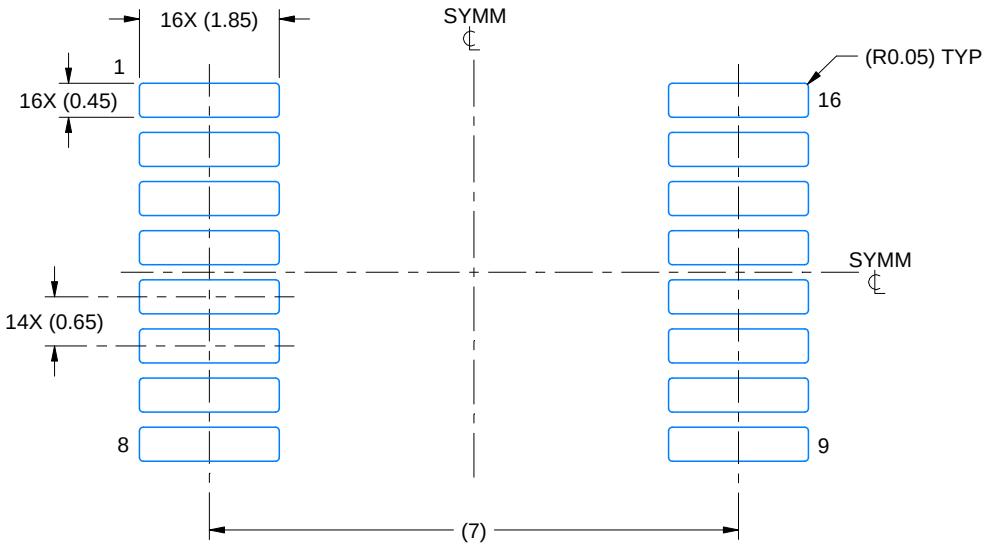
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

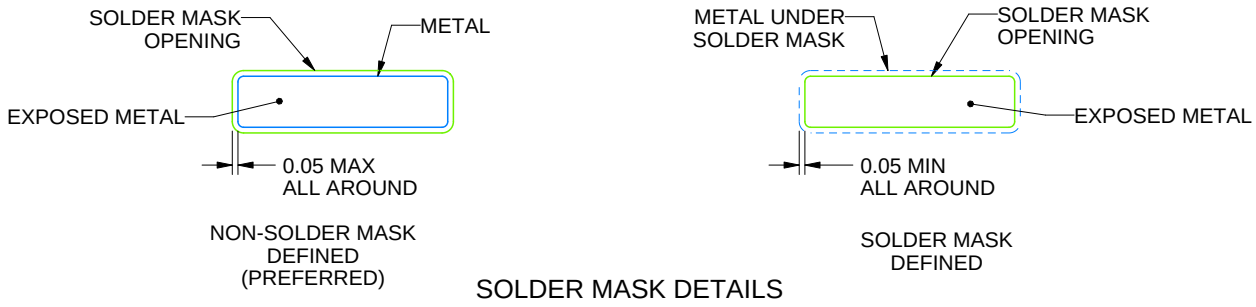


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

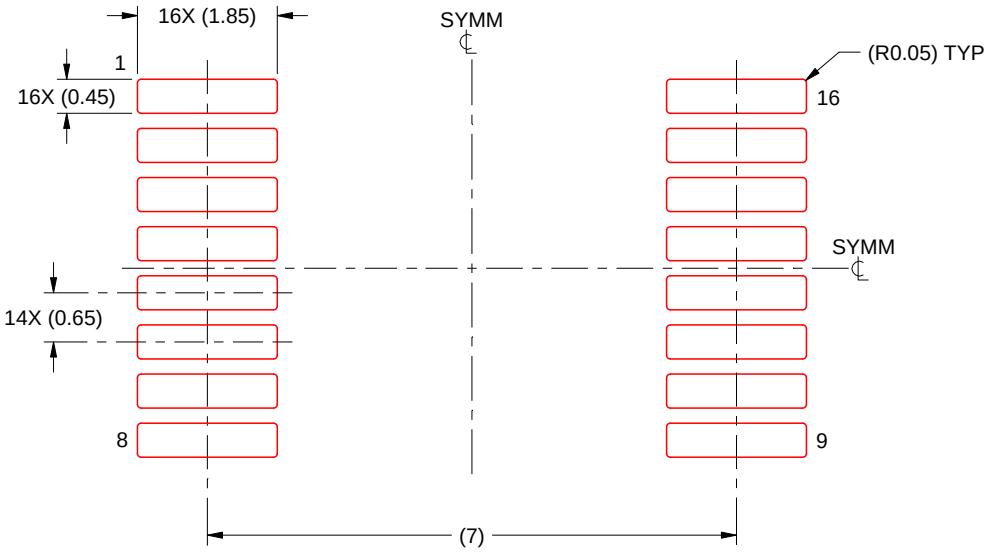


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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