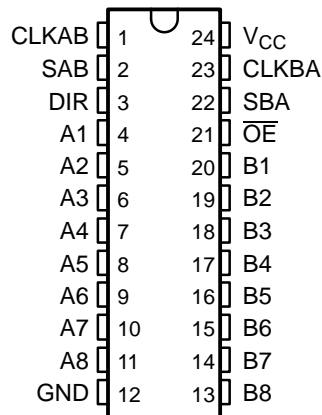


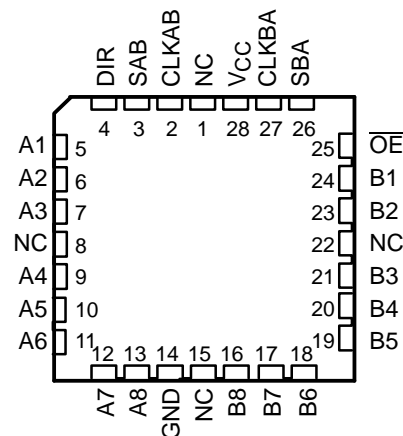
FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 7.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVC646A . . . JT OR W PACKAGE
SN74LVC646A . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVC646A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC646A octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC646A octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|----------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube of 25 | SN74LVC646ADW | LVC646A |
| | | Reel of 2000 | SN74LVC646ADWR | |
| | SOP – NS | Reel of 2000 | SN74LVC646ANSR | LVC646A |
| | SSOP – DB | Reel of 2000 | SN74LVC646ADBR | LC646A |
| | TSSOP – PW | Tube of 60 | SN74LVC646APW | LC646A |
| | | Reel of 2000 | SN74LVC646APWR | |
| Reel of 250 | | SN74LVC646APWT | | |
| -55°C to 125°C | CDIP – JT | Tube of 15 | SNJ54LVC646AJT | SNJ54LVC646AJT |
| | CFP – W | Tube of 85 | SNJ54LVC646AW | SNJ54LVC646AW |
| | LCCC – FK | Tube of 42 | SNJ54LVC646AFK | SNJ54LVC646AFK |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCAS302J—JANUARY 1993—REVISED AUGUST 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that are performed with the 'LVC646A devices.

Output-enable (\overline{OE}) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port is stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data is stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|-----------------|-----|--------|--------|-----|-----|----------------------------|----------------------------|---------------------------------------|
| \overline{OE} | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified ⁽¹⁾ | Store A, B unspecified ⁽¹⁾ |
| X | X | X | ↑ | X | X | Unspecified ⁽¹⁾ | Input | Store B, A unspecified ⁽¹⁾ |
| H | X | ↑ | ↑ | X | X | Input | Input | Store and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

(1) The data-output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

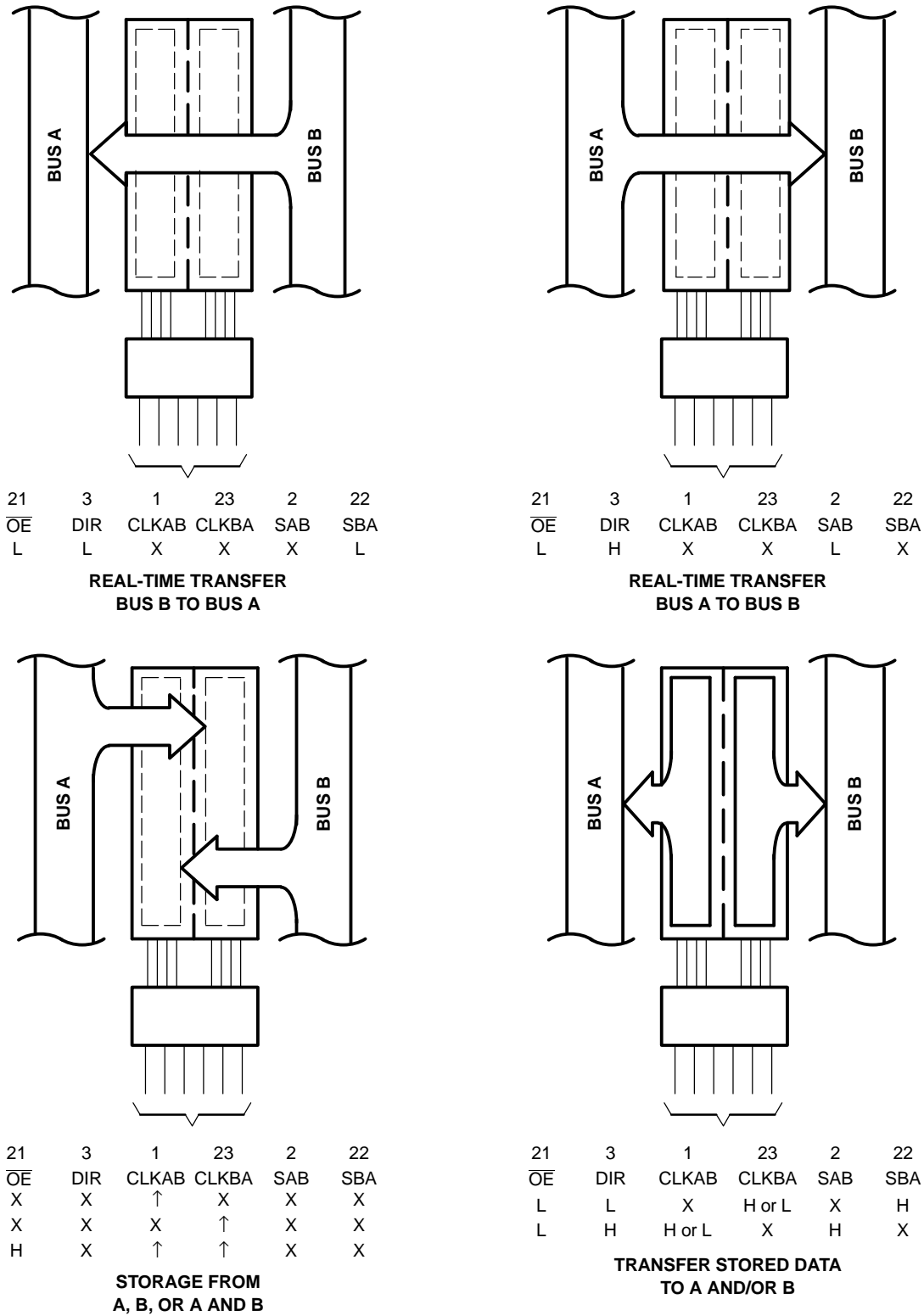
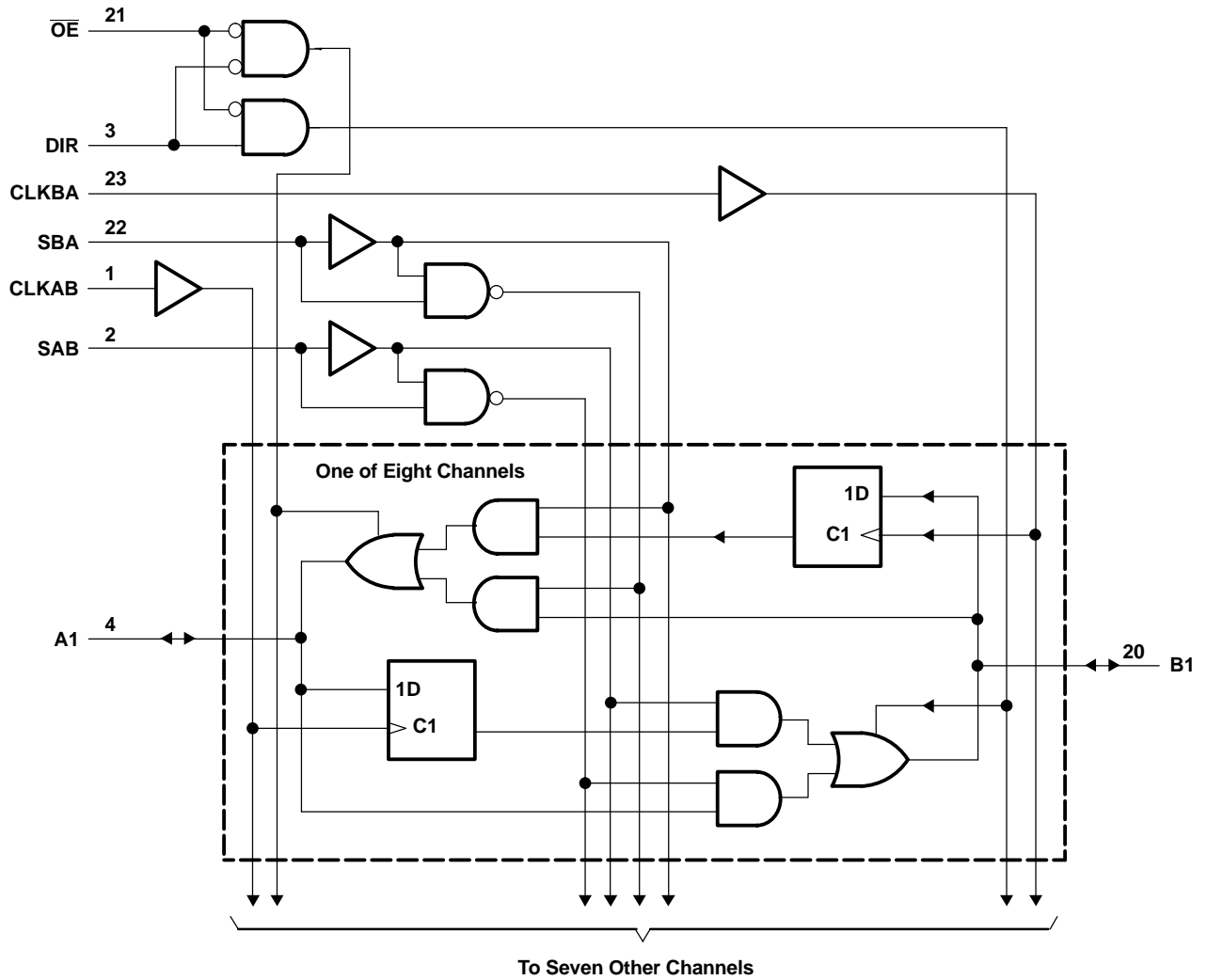


Figure 1. Bus-Management Functions

SN54LVC646A, SN74LVC646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DB, DW, JT, NS, PW, and W packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| θ _{JA} | Package thermal impedance ⁽⁴⁾ | DB package | 63 | °C/W |
| | | DW package | 46 | |
| | | NS package | 65 | |
| | | PW package | 88 | |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | SN54LVC646A | | SN74LVC646A | | UNIT | |
|-----------------|------------------------------------|------------------------------------|-----|-----------------|------------------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | | |
| V _{CC} | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | | | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | | 0.8 | |
| V _I | Input voltage | 0 | 5.5 | | | 5.5 | V |
| V _O | Output voltage | High or low state | 0 | V _{CC} | | V _{CC} | V |
| | | 3-state | 0 | 5.5 | | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | | | -4 | mA |
| | | V _{CC} = 2.3 V | | | | -8 | |
| | | V _{CC} = 2.7 V | | -12 | | -12 | |
| | | V _{CC} = 3 V | | -24 | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | | | 4 | mA |
| | | V _{CC} = 2.3 V | | | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | | 12 | |
| | | V _{CC} = 3 V | | 24 | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | 10 | | | 10 | ns/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LVC646A | | | SN74LVC646A | | | UNIT |
|--------------------------------|---------------------------|--|-----------------------|--------------------|------|-----------------------|--------------------|-----|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OH} | I _{OH} = –100 μA | 1.65 V to 3.6 V | | | | V _{CC} – 0.2 | | | V |
| | | 2.7 V to 3.6 V | V _{CC} – 0.2 | | | | | | |
| | I _{OH} = –4 mA | 1.65 V | | | 1.2 | | | | |
| | I _{OH} = –8 mA | 2.3 V | | | 1.7 | | | | |
| | I _{OH} = –12 mA | 2.7 V | | 2.2 | | 2.2 | | | |
| | | 3 V | | 2.4 | | 2.4 | | | |
| I _{OH} = –24 mA | 3 V | | 2.2 | | 2.2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | | 0.2 | | | V |
| | | 2.7 V to 3.6 V | | | 0.2 | | | | |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | | | | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.7 | | | | |
| | I _{OL} = 12 mA | 2.7 V | | | 0.4 | 0.4 | | | |
| 3 V | | | | 0.55 | 0.55 | | | | |
| I _I | Control inputs | V _I = 0 to 5.5 V | 3.6 V | | | ±5 | | ±5 | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | | | | ±10 | μA |
| I _{OZ} ⁽²⁾ | | V _O = 0 to 5.5 V | 3.6 V | | | ±15 | | ±10 | μA |
| I _{CC} | | V _I = V _{CC} or GND 3.6 V ≤ V _I ≤ 5.5 V ⁽³⁾ | I _O = 0 | 3.6 V | | 10 | | 10 | μA |
| | | | | | | 10 | | 10 | |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | | 500 | μA |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | | 4.5 | | | 4.5 | pF |
| C _{io} | A or B port | V _O = V _{CC} or GND | 3.3 V | | 7.5 | | | 7.5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(3) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

| | | SN54LVC646A | | | | UNIT |
|--------------------|------------------------------|-------------------------|-----|------------------------------------|-----|------|
| | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 150 | | 150 | | MHz |
| t _w | Pulse duration | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before CLK↑ | 1.6 | | 1.5 | | ns |
| t _h | Hold time, data after CLK↑ | 1.7 | | 1.7 | | ns |

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | SN74LVC646A | | | | | | | | UNIT |
|--------------------|--|--|-----|---|-----|-------------------------|-----|---|-----|------|
| | | $V_{CC} = 1.8\text{ V}$ $\pm 0.18\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | (1) | | (1) | | 150 | | 150 | | MHz |
| t_w | Pulse duration | (1) | | (1) | | 3.3 | | 3.3 | | ns |
| t_{su} | Setup time, data before CLK \uparrow | (1) | | (1) | | 1.6 | | 1.5 | | ns |
| t_h | Hold time, data after CLK \uparrow | (1) | | (1) | | 1.7 | | 1.7 | | ns |

(1) This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC646A | | | | UNIT |
|------------------|------------------------|----------------|-------------------------|-----|---|-----|------|
| | | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | |
| f_{max} | | | 150 | | 150 | | MHz |
| t_{pd} | A or B | B or A | 7.9 | | 1 | 7.4 | ns |
| | CLK | A or B | 8.8 | | 1 | 8.4 | |
| | SBA or SAB | | 9.9 | | 1 | 8.6 | |
| t_{en} | $\overline{\text{OE}}$ | A | 10.2 | | 1 | 8.2 | ns |
| t_{dis} | $\overline{\text{OE}}$ | A | 8.9 | | 1 | 7.5 | ns |
| t_{en} | DIR | B | 10.4 | | 1 | 8.3 | ns |
| t_{dis} | DIR | B | 8.7 | | 1 | 7.9 | ns |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC646A | | | | | | | | UNIT |
|------------------|------------------------|----------------|--|-----|---|-----|-------------------------|-----|---|-----|------|
| | | | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | (1) | | (1) | | 150 | | 150 | | MHz |
| t_{pd} | A or B | B or A | (1) | (1) | (1) | (1) | 7.9 | | 1 | 7.4 | ns |
| | CLK | A or B | (1) | (1) | (1) | (1) | 8.8 | | 1 | 8.4 | |
| | SBA or SAB | | (1) | (1) | (1) | (1) | 9.9 | | 1 | 8.6 | |
| t_{en} | $\overline{\text{OE}}$ | A | (1) | (1) | (1) | (1) | 10.2 | | 1 | 8.2 | ns |
| t_{dis} | $\overline{\text{OE}}$ | A | (1) | (1) | (1) | (1) | 8.9 | | 1 | 7.5 | ns |
| t_{en} | DIR | B | (1) | (1) | (1) | (1) | 10.4 | | 1 | 8.3 | ns |
| t_{dis} | DIR | B | (1) | (1) | (1) | (1) | 8.7 | | 1 | 7.9 | ns |

(1) This information was not available at the time of publication.

SN54LVC646A, SN74LVC646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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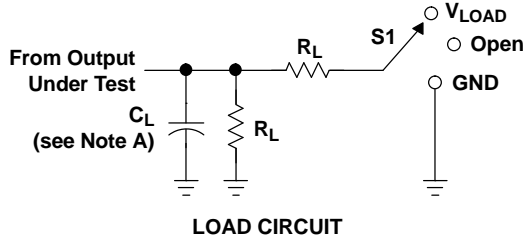
Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------------|---|-----------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per transceiver | f = 10 MHz | (1) | (1) | 75 | pF |
| | Outputs enabled | | (1) | (1) | 9 | |
| | Outputs disabled | | (1) | (1) | | |

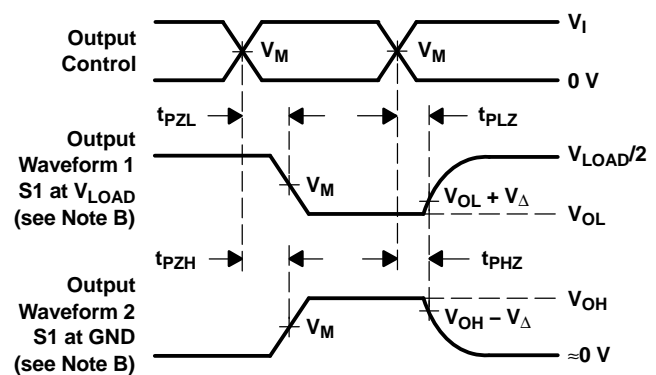
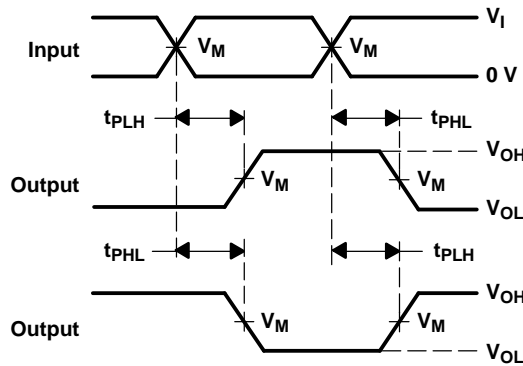
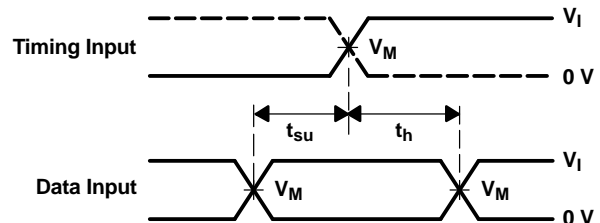
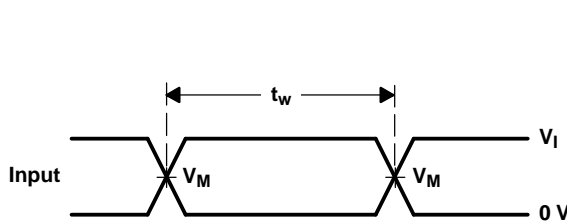
(1) This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC646ADBR | ACTIVE | SSOP | DB | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC646A | Samples |
| SN74LVC646ADW | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC646A | Samples |
| SN74LVC646ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| SN74LVC646APW | ACTIVE | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC646A | Samples |
| SN74LVC646APWR | ACTIVE | TSSOP | PW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC646A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC646ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC646APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC646ADBR | SSOP | DB | 24 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC646APWR | TSSOP | PW | 24 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVC646ADW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74LVC646APW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

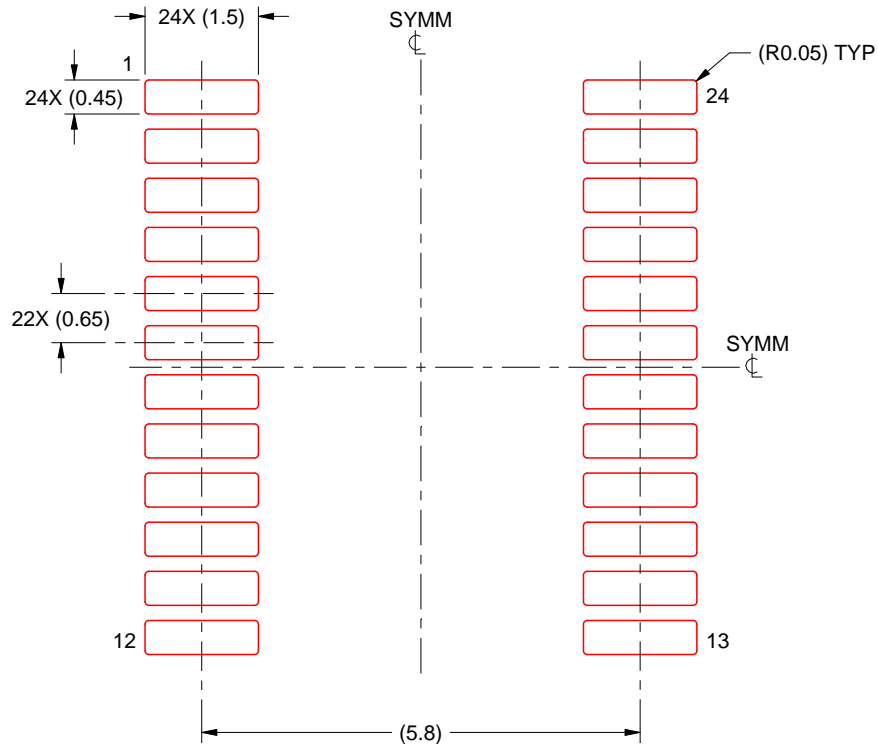
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

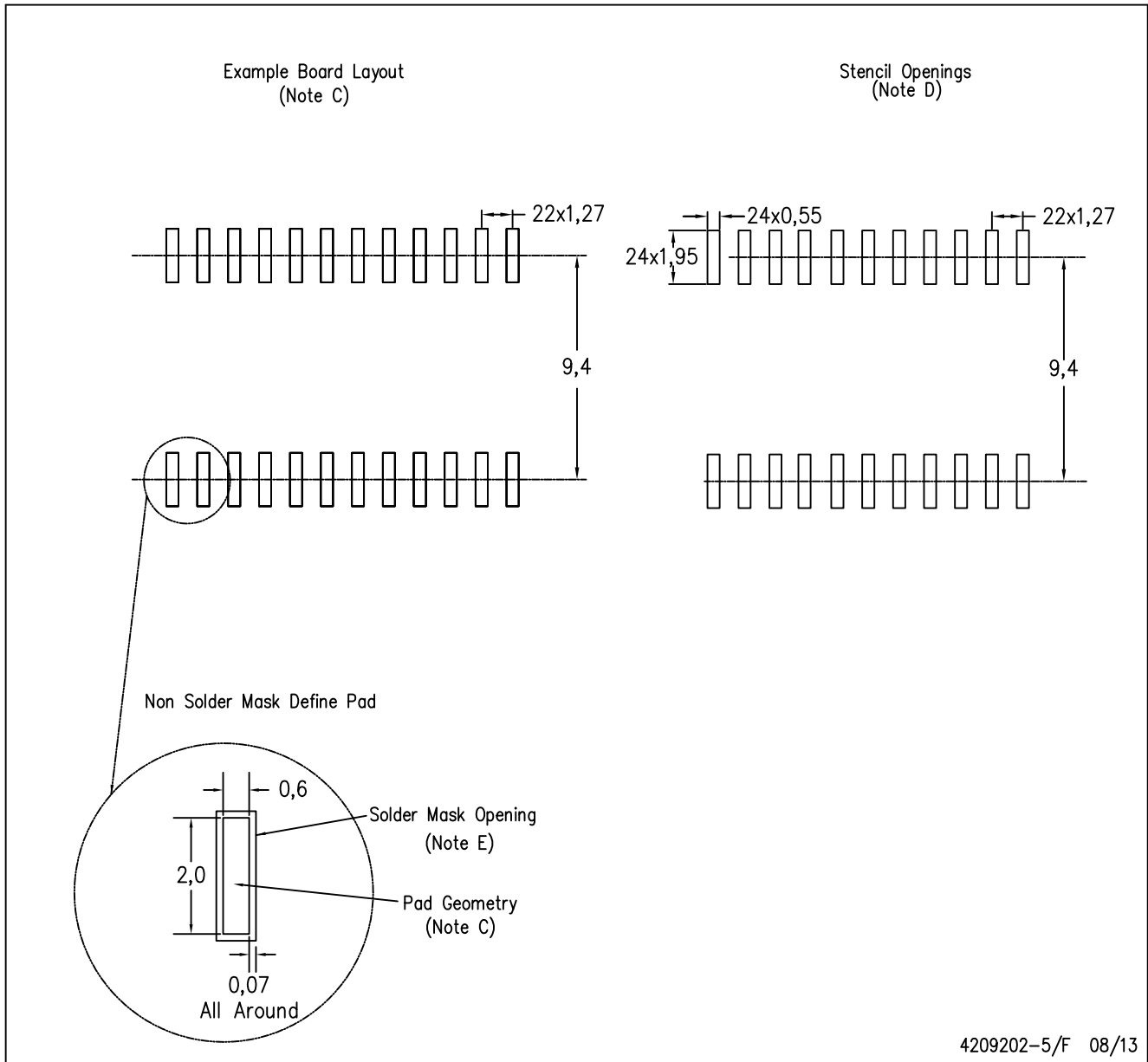
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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