Application Report
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Programmable Yn Clock Phase Shift With SN74SSQEA32882 DDR3 Register

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ABSTRACT

This application report describes how to shift the Yn clock position on TI's DDR3 register SN74SSQEA32882 (V4.2) by using extended CMR commands. This Yn clock position shift can be used for the analysis of post register margin at the DRAMs. Note that this application report does not apply to SN74SSQE32882 (V3.1).

1 CMR Commands

SSTE32882-compliant DDR3 registers have internal control bits (also called Control Mode registers) to configure certain device features.

If the device is operated in Dual Chip Select Mode (QCSEN#=HIGH), then the control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# LOW.

If Quad Chip Select Mode is enabled (QCSEN#=LOW), then the control bits are accessed by the simultaneous LOW assertion of both DCS0# and DCS1# or DCS2# and DCS3# or all four DCS[n:0].

SSTE32882-compliant DDR3 registers allocate decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0, and DBA1.

For more details on CMR commands and how to use them, see the SSTE32882 JEDEC Specification or TI application report SCAA102.

2 Extended CMR Commands

Extended CMR command to the register are not standardized by JEDEC; they only apply to TI DDR3 Registers. To access an extended CMR, the device has to be put into extended CMR mode by setting RC7 bit DA2 to 1.

The purpose of the extended CMRs is mainly for TI internal testing. Different device versions may have different mappings for extended CMRs.

3 Yn Clock Phase Shift Function of SN74SSQEA32882 (V4.2)

TI's DDR3 register SN74SSQEA32882 (V4.2) allows manual adjustment of the Yn edge position within the Command/Address (C/A) data eye. Note that this feature is not supported in TI register SN74SSQE32882 (V3.1).

The Yn clock edge phase can be modified with the following steps:

1. Enable Extended CMR range in RC7.
2. Disable C/A tracking of Yn in RC23.
3. Enable manual phase adjustment in RC17.
4. Write manual phase adjust control word (PA<19:0>, see Table 1). This requires programming of RC18-RC22.
5. Switch back to standard CMR range in RC7 (if standard CMR programming is required)

Table 1. Simplified Phase Adjust Control Word Lookup Table[(1)]

Phase Adjustment in Degrees	Phase Adjust Control Word PA<0:19>				
	<0>	<1>	<2>	<3>	<4:19>
0°	0	0	0	0	0x0000
22.5°	1	0	0	0	0xFFFF
45°	1	1	0	0	0x0000
67.5°	0	1	0	0	0xFFFF
90°	0	1	1	0	0x0000
112.5°	1	1	1	0	0xFFFF
135°	1	1	1	1	0x0000
157.5°	0	1	1	1	0xFFFF
180°	0	1	0	1	0x0000
202.5°	1	1	0	1	0xFFFF
225°	1	0	0	1	0x0000
247.5°	0	0	0	1	0xFFFF
270°	0	0	1	1	0x0000
292.5°	1	0	1	1	0xFFFF
315°	1	0	1	0	0x0000
337.5°	0	0	1	0	0xFFFF

(1) More detailed lookup table available, if required.

3.1 CMR Sequence for Adjusting the Yn Phase

Table 2. CMR Sequence for Changing Yn Clock Phase

Change Yn Clock Phase								
CMR7	Enable Extended CMR							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	1	1	1		0	0	0	1
Wait 8 clock cycles								
CMR23	Disabled C/A Tracking of Yn							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
1	0	0	1		0	0	1	0
Wait 8 clock cycles								
CMR17	Enable Manual Phase Adjust							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	0	0	1		1	0	0	0
Wait 8 clock cycles								
CMR18	<3:0> (Manual Phase Adjust Value)							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	0	1	0		*PA<3>*	*PA<2>*	*PA<1>*	*PA<0>*
Wait 8 clock cycles								
CMR19	<7:4> (Manual Phase Adjust Value)							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	0	1	1		*PA<7>*	*PA<6>*	*PA<5>*	*PA<4>*
Wait 8 clock cycles								
CMR20	<11:8> (Manual Phase Adjust Value)							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	1	0	0		*PA<11>*	*PA<10>*	*PA<9>*	*PA<8>*
Wait 8 clock cycles								
CMR21	<15:12> (Manual Phase Adjust Value)							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	1	0	1		*PA<15>*	*PA<14>*	*PA<13>*	*PA<12>*
Wait 8 clock cycles								
CMR22	<19:16> (Manual Phase Adjust Value)							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
1	0	0	1		*PA<19>*	*PA<18>*	*PA<17>*	*PA<16>*
Wait 8 clock cycles								
CMR7	Switch back to Standard CMR							
DBA2	DA2	DA1	DA0		DBA1	DBA0	DA4	DA3
0	1	1	1		0	0	0	0

3.2 Example Phase Adjustments of Yn Clock

The following scope shots are examples of how the Yn clock phase can be changed within the C/A data eye.

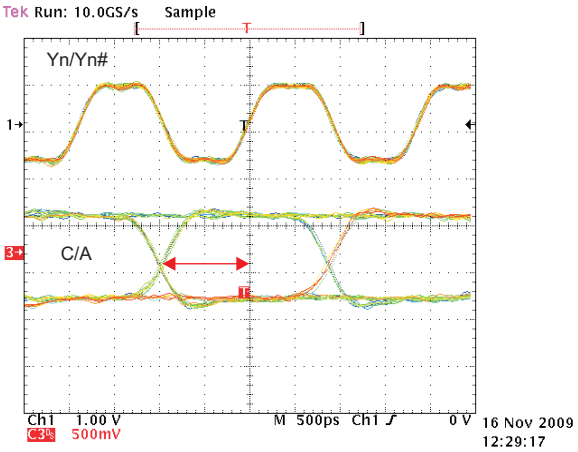

Figure 1. Yn Clock Default Phase Setting (Center of C/A eye)

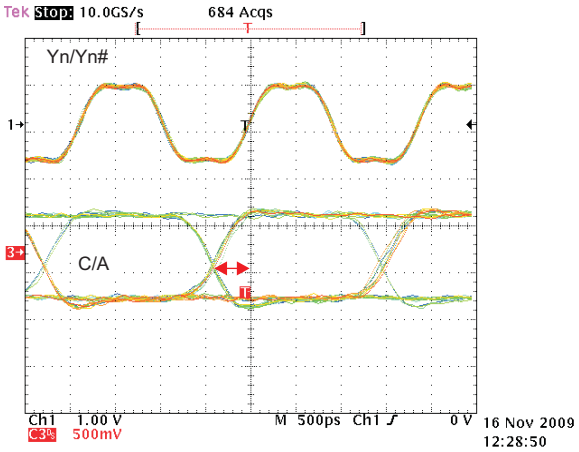

Figure 2. Yn Clock With Phase Adjust Value 0°

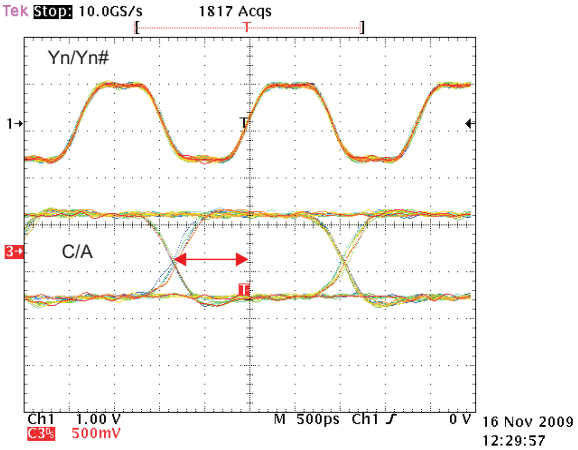

Figure 3. Yn Clock With Phase Adjust Value 90°

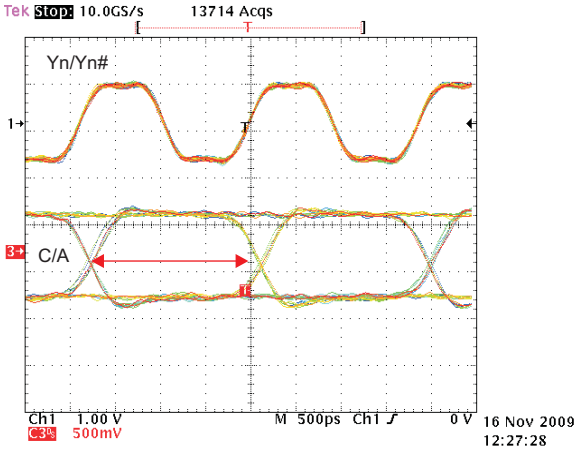

Figure 4. Yn Clock With Phase Adjust Value 270°

4 References

1. *SN74SSQE32882, 28-Bit to 56-Bit Registered Buffer WIth Address Parity Test One Pair to Four Pair Differential Clock PLL Driver* data sheet (SCAS857)
2. *SN74SSQEA32882, 28-Bit to 56-Bit Registered Buffer WIth Address Parity Test One Pair to Four Pair Differential Clock PLL Driver* data sheet (SCAS879)
3. *CMR Programming for DDR3 Registers* application report (SCAA102)
4. SSTE32882 JEDEC Specification

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