Designing With TI SN74V2x5 FIFO Programmable Flags

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ABSTRACT

Many FIFOs being released today include programmable almost-empty and almost-full flags. TI's newly released SN74V2x5 FIFOs are functionally equivalent to devices offered by IDT and are pin-for-pin compatible. The programmable flags can be used to provide interrupt signals when used in digital signal processor (DSP) and microprocessor applications. Additional configurations use the programmable flags for driving read-enable control pins to provide data delays and even programmable-depth shift registers.

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Introduction

TI has recently released a new family of FIFOs that are speed upgrades for an equivalent IDT family of FIFOs. Table 1 lists the TI parts and the IDT pin-for-pin functional equivalents. These FIFOs provide a glueless interface to the C6x X-Bus.

Table 1. TI and IDT Equivalent Programmable-Flag FIFOs

SIZE	TI FIFO		IDT FIFO	
	TI DEVICE	MAXIMUM SPEED	IDT DEVICE	MAXIMUM SPEED
4096 × 18	SN74V245	133 MHz	IDT72V245	100 MHz
2048 × 18	SN74V235	133 MHz	IDT72V235	100 MHz
1024 × 18	SN74V225	133 MHz	IDT72V225	100 MHz
512 × 18	SN74V215	133 MHz	IDT72V215	100 MHz

Programmable flags in FIFOs often are used to provide a signal to indicate that a specified block of memory is available for data storage or that a specified block of stored data is available for transfer (see Figure 1). The flags are valid only as long as the condition is true, so they are ideal for providing an interrupt signal for microprocessor and digital signal-processor (DSP) applications.

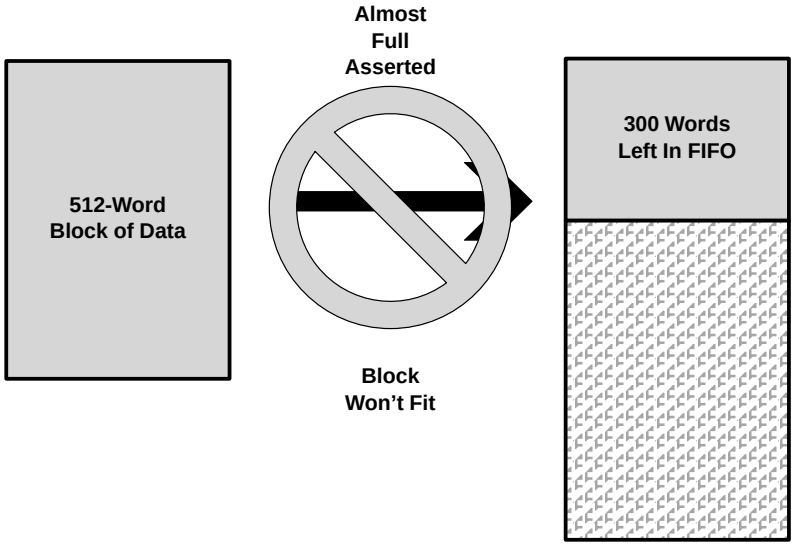


Figure 1. Functional Example of Programmable Flags for Data Burst

The programmable flags allow blocks of data to be burst without further flag monitoring, thus reducing the control overhead needed for data transfers.

Another application for which programmable flags often are used is the delay of data (see Figure 2). Sometimes a delay is needed to allow time for decoding node addresses, data alignment, digital filtering, etc.

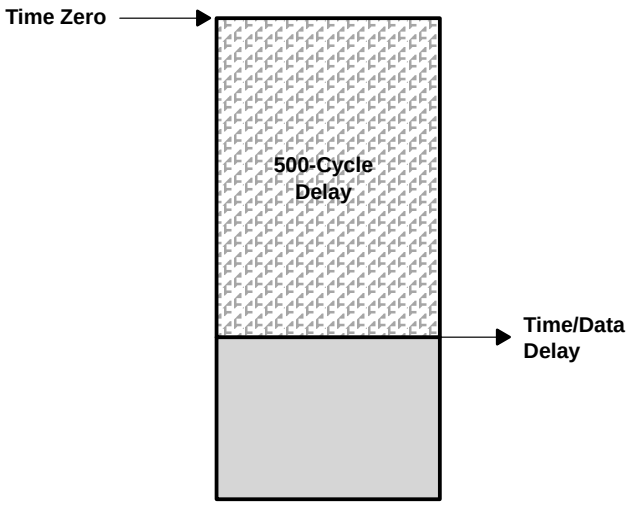


Figure 2. Delay-of-Data Application

Zero-Cycle Flag Latency for Driving Interrupts

TI SN74V2x5 devices offer programmable-flag operation that occurs in the same clock cycle that triggers the flags to be asserted. The programmable almost-empty ($\overline{PAE}$) flag is asserted in the same read-clock (RCLK) cycle that reduces the number of data words stored in the FIFO to the almost-empty offset value.

Figure 3 illustrates the $\overline{PAE}$ flag operation for SN74V2x5 devices. In this example, the FIFO is in synchronous mode and, as a result, the $\overline{PAE}$ flag is asserted and updated on the rising edge of RCLK only. A minimum skew is required between a rising RCLK edge and a rising WCLK edge for $\overline{PAE}$ to go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than the minimum, the $\overline{PAE}$ deassertion time might be delayed an additional WCLK cycle.

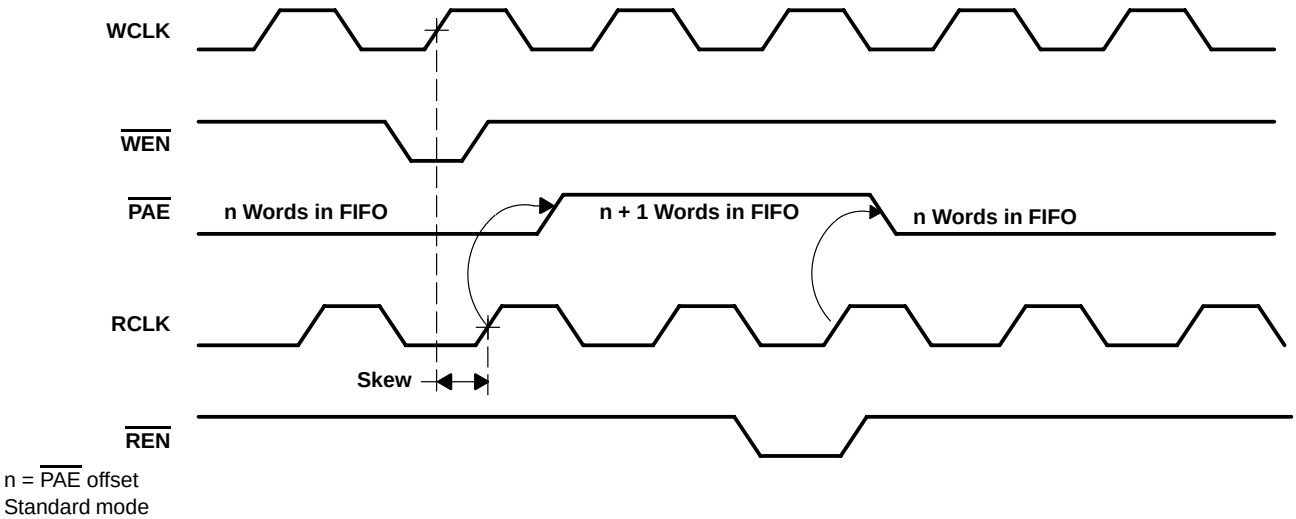
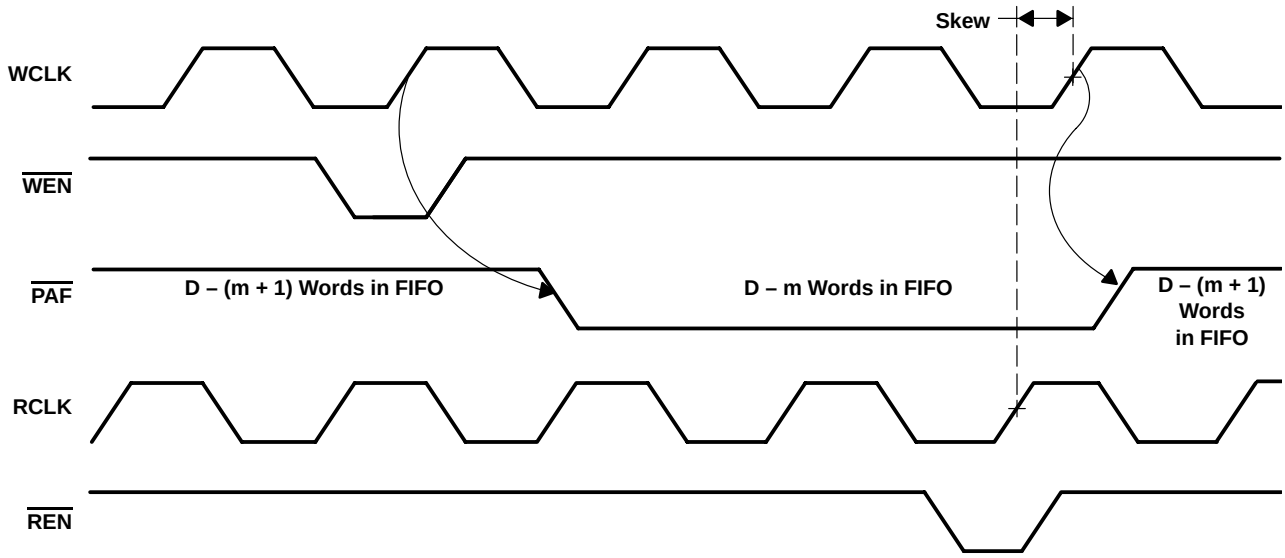


Figure 3. $\overline{PAE}$ Flag Operation

Figure 4 shows the response of the programmable almost-full ($\overline{PAF}$) flag. In this example the FIFO is in synchronous mode and, as a result, the $\overline{PAF}$ flag is asserted and updated on the rising edge of WCLK only. As in the case of the $\overline{PAE}$ flag deassertion, a minimum skew between the WCLK and RCLK rising edges is required for the $\overline{PAF}$ flag to be updated during the current cycle.



m = $\overline{PAF}$ offset
D = Maximum FIFO depth
Standard mode

Figure 4. $\overline{PAF}$ Flag Operation

Programmable Flag Operation for Data Delays

In many applications involving node networks, it is necessary to decode a node address before passing the data to the correct node. In this case, the block of data is delayed for the time needed to address the node. Also, in applications such as line buffers for HDTV, software-controlled data alignment, sample-rate conversion, and digital filtering, programmable delays are needed to achieve the desired results.

Frame buffers and some other applications require the acquisition of data before and/or after certain actions are performed. In this case, the $\overline{WEN}$ signal defines the range of the data between start and stop actions. For instance, the controller sends a command to store a value in the programmable offset register, which defines the range of data that is to be stored continuously in the FIFO during the period of action. In any of these applications, $\overline{PAF}$ and $\overline{PAE}$ are used to meet the requirements.

Figure 5 shows a typical FIFO connection for the programmable delay of data. The almost-empty offset register was loaded with the value n = 3 and the almost-full offset register was loaded with the value m = 4090. Figure 6 illustrates the flag behavior on the high-to-low transition of $\overline{PAF}$ while writing to the FIFO.

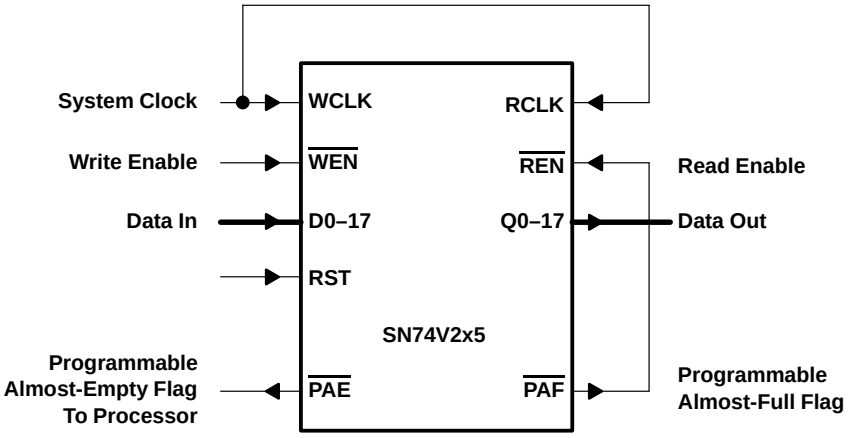
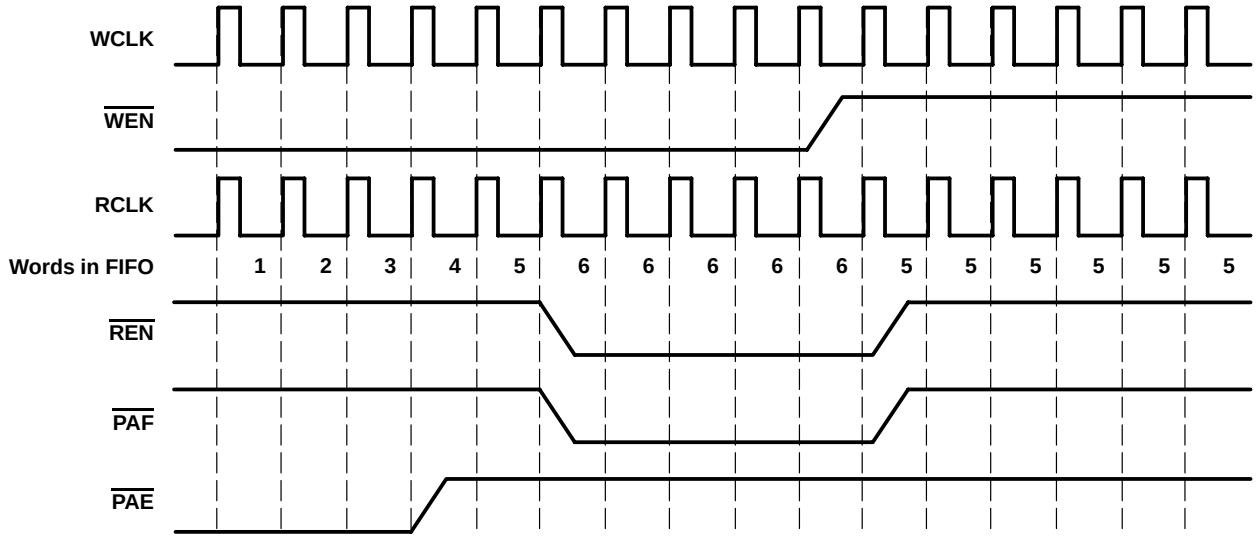


Figure 5. Typical Connections for Programmable Delay of Data

The waveforms in Figure 6 are based on the configuration in Figure 5. The effect of this configuration is that the FIFO stores six words, then begins reading data out at the same rate as it is stored. Hence, there always is a six-cycle delay between the data being presented to the FIFO and the data being sent from the FIFO. The $\overline{PAF}$ flag goes low when the FIFO is almost full. In this case, $\overline{PAF}$ goes low when 4096 – 4090 = 6 words are written to the FIFO. It also should be noted that a minimum skew between WCLK and RCLK is required for the flags to be updated correctly.



n = $\overline{PAE}$ offset = 3
m = $\overline{PAF}$ offset = 4090
Standard synchronous mode

Figure 6. FIFO Input and Output Data Timing

Programmable-Depth Shift Register

The programmable flags also can be used to realize a shift register with programmable depth. Figure 7 illustrates a data wrap-around configuration to generate an 18-tap shift register that is programmable in 18-bit increments.

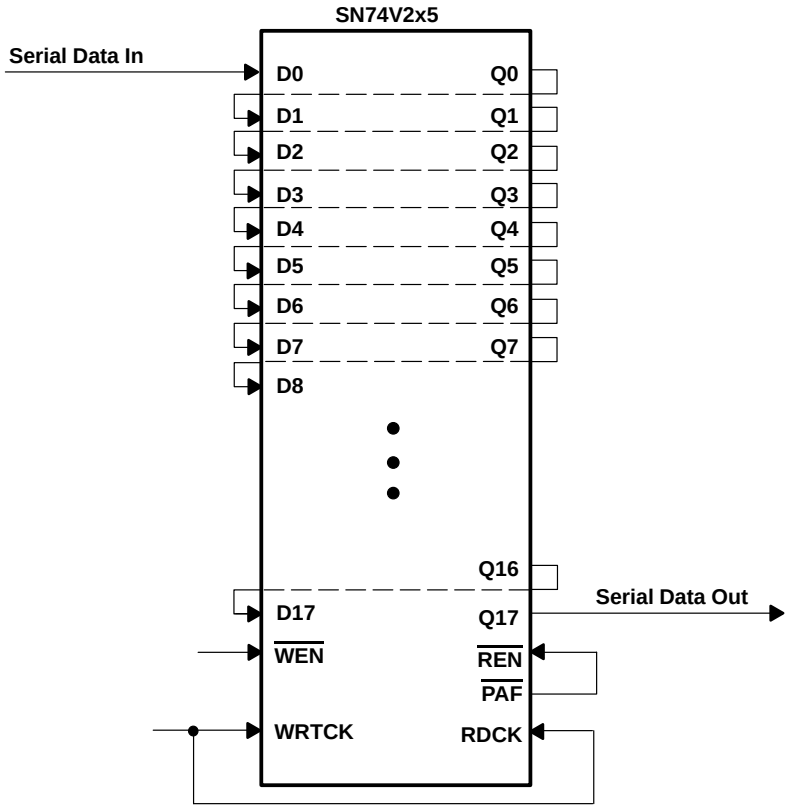


Figure 7. Programmable-Depth Shift-Register Configuration

In this configuration, the programmable offset register is loaded when $\overline{LD}$ is low on a low-to-high transition of WCLK. This offset determines the size of the resulting shift register. The programmable full offset, m, is an index referenced from the maximum FIFO depth, D. The size of the shift register, SRS, is calculated in equation 1.

$$SRS = (D - m) \times 18 \quad (1)$$

After the offset is programmed, data shifted into D0. While valid data is shifted into D0, D1 through D17 are shifting in invalid data. When the offset is reached, $\overline{PAF}$ goes low, driving $\overline{REN}$ low as well. On the next clock, the first valid bit of data is read from Q0 by D1, while another valid data bit is shifted into D0. When $\overline{PAF}$ becomes valid, the data from Qx is presented to D(x + 1). The number of clocks necessary to shift out the first valid data bit on Q17 also is calculated using equation 1. The latency required to shift out the first data bit is the clock period, τ, multiplied by the size of the shift register, SRS (see equation 2).

$$Latency = \tau \times SRS \quad (2)$$

The data bit present at each output, Qx, of the FIFO can be calculated using equation 3. This equation applies when the shift register is full of valid data. This also assumes that the first data bit is labeled as bit 1, not bit 0.

$$\text{Data bit present on Qx} = \text{number of clocks} - x \times (D - m) + 1 \quad (3)$$

Another way to visualize this shift register is shown in Figure 8.

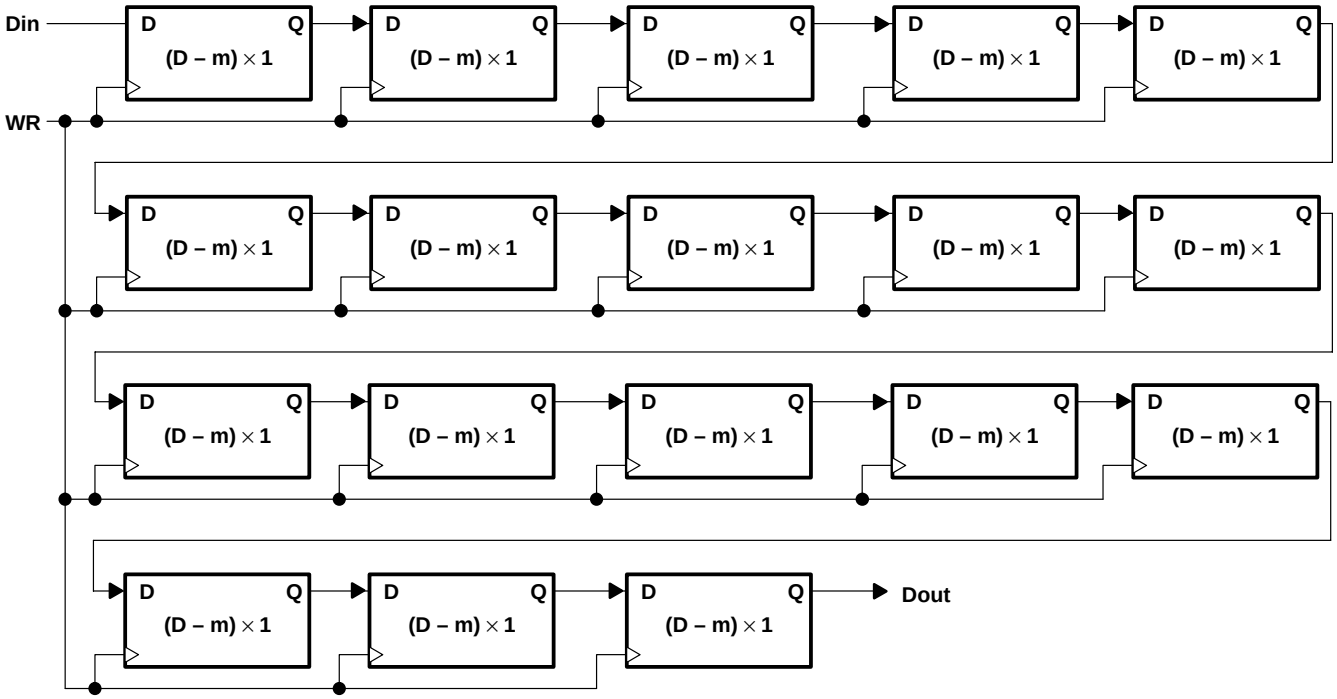


Figure 8. Alternate Visualization of the Programmable-Depth Shift Register

Conclusion

The TI SN74V2x5 family of high-speed low-voltage 18-bit FIFOs provides a glueless interface to the C6x X-Bus. Their high speed provides the next-generation choice for new DSP designs.

Programmable flags provide many design alternatives for data buffering, data bursting, and data delays. Using a wrap-around data-flow configuration, the programmable flags also can render a programmable-depth shift register.

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