Application Report
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How to Bridge HDMI/DVI to LVDS/OLDI

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ABSTRACT

This document provides an overview of how to connect HDMI (High-Definition Multimedia Interface) or DVI (Digital Visual Interface) source to LVDS (Low Voltage Differential Signaling) or OLDI (OpenLDI) panel or display. The two-chip solutions receive 3 TMDS (Transition Minimized Differential Signaling) pairs and a clock, and output 4 or 8 LVDS/OLDI data pairs and clocks.

Trademarks

1 Block Diagrams

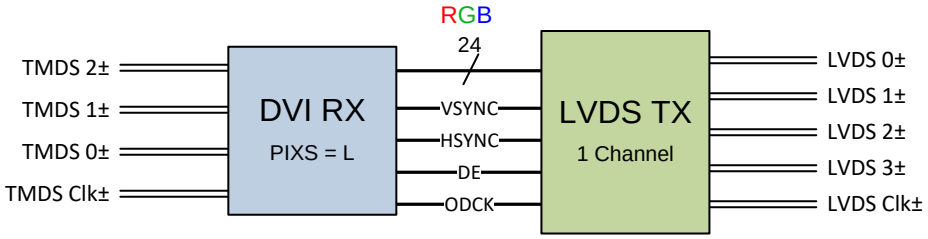

Figure 1. DVI Receiver to a 1-channel LVDS/OLDI Transmitter

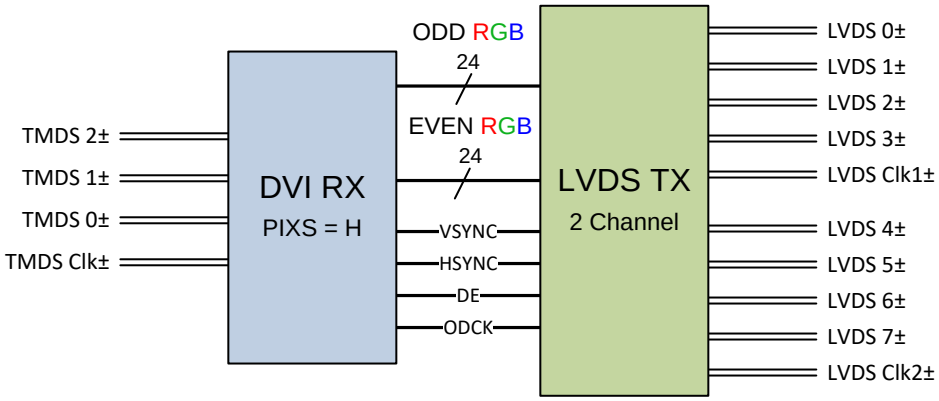

Figure 2. DVI Receiver to a 2-channel LVDS/OLDI Transmitter

The DVI RX output is configurable with pin “PIXS”. When PIXS is Low, RGB data is output on 24 bits (QE[23:0]). When PIXS is High, RGB data is split odd/even on 48-bits (QO[23:0] & QE[23:0]). The 4 additional bits are VSYNC, HSYNC, DE, and ODCK.

2 1-Channel vs. 2-Channel

The choice between using a 1-channel or 2-channel LVDS/OLDI transmitter depends on what the connecting panel uses. Most panels that receive LVDS/OLDI that have a resolution of < 1400 x 1050 use 1-channel, which consists of 3 or 4 LVDS/OLDI data pairs (depending on 18-bit or 24-bit color). Most panels that have a resolution between 1400 x 1050 – 1920 x 1200 use a 2-channel receiver interface, with 6 or 8 LVDS data pairs.

3 The DVI RX

There are 4 recommended DVI receivers to choose from as shown in Table 1.

Table 1. DVI Receivers

Part Name	Temperature Range (°C)	Max Frequency (MHz)	HDCP	Automotive
TFP401A	0 to 70	165	No	No
TFP401A-EP	-55 to 125	165	No	No
TFP401A-Q1	-40 to 85	165	No	Yes
TFP501	0 to 70	165	Yes	No

4 The LVDS TX

For LVDS/OLDI, there are 5 recommended devices shown in Table 2.

Table 2. LVDS Transmitters

Part Name	Temperature Range (°C)	Frequency Range (MHz)	Number of RGB Bits	Automotive
SN65LVDS93A	-40 to 85	10 to 135	24	No
SN65LVDS93A-Q1	-40 to 85	10 to 135	24	Yes
SN65LVDS93B	-40 to 85	10 to 85	24	No
SN65LVDS93B-Q1	-40 to 85	10 to 85	24	Yes
DS90C387A	-10 to 70	32.5 to 112/170	48	No

5 Notes on Common Resolutions

- 1280 x 800 and 720p normally use 1-channel LVDS/OLDI with a 70-75 MHz pixel clock.
- 1080p normally use 2-channel LVDS/OLDI with a 74.25 MHz pixel clock.
- 1080p 120 Hz normally use high frequency HDMI and 4-channel LVDS/OLDI; this is not supported.
- For further elaboration, visit this *pixel clock requirements* blog.

6 Design Guidelines

1. If using the SN65LVDS93A (93A), SN65LVDS93A-Q1 (93A-Q1), SN65LVDS93B (93B), or SN65LVDS93B-Q1 (93B-Q1), set the power supply “IOVCC” to 3.3 V to match the DVI RX output that is always 3.3 V.
2. Set the same clock edge for the two devices. For example, for rising edge the DVI RX pin “OCK_INV” is High, and the LVDS TX pin “CLKSEL” (93A/93A-Q1/93B/93B-Q1) or “R_FB” (Ds90C387A) is also set to High. When using the DS90C387A (387A), set pin “DUAL” to High to set the 48:8 mode.
3. Length match all data and control signals between devices to be within 400 mils of ODK with a maximum distance of 6 inches.
4. The incoming TMDS data must be DVI-compliant, and not contain HDMI island data (that is, audio) or deep color (more than 24 color bits).

7 Pin Mapping Examples

The parallel pin mapping defines the sequence of bits in the LVDS/OLDI lanes. It must match the bit sequence that the panel expects. The 1-channel and 2-channel examples below show common schemes, to serve as a reference.

There are two color bit mapping standards that are commonly used, VESA and JEIDA. VESA (Video Electronics Standard Association) is shown on the left in Figure 3, and JEIDA (Japan Electronic Industried Development Association) is shown on the right in Figure 3. Different mapping standards can be achieved by changing the DVI RX output is connected with LVDS TX input. The convention followed in 93A/93A-Q1/93B/93B-Q1 is VESA, as shown in Table 3, but JEIDA is also shown as a reference.

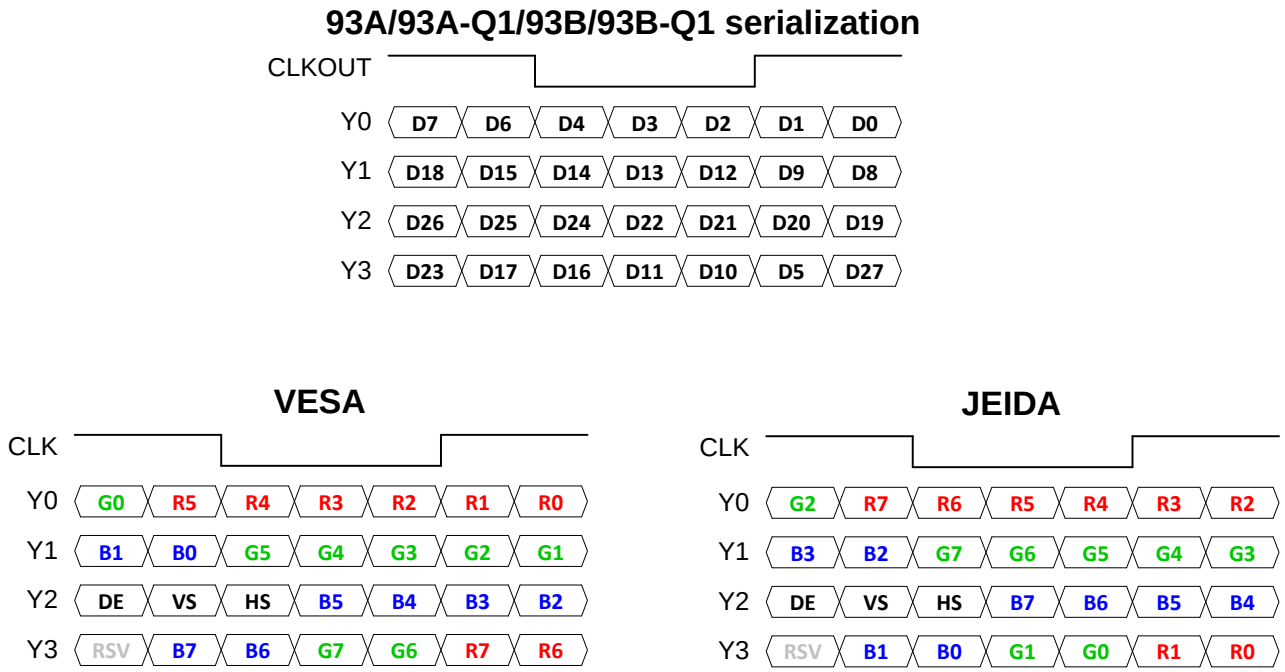

Figure 3. 1-Channel LVDS Connection Example

Table 3. 1-Channel LVDS Connection

DVI Output	Description	93A/93A-Q1/93B/93B-Q1 Input
QE[0]	B0 (LSB)	D15
QE[1]	B1	D18
QE[2]	B2	D19
QE[3]	B3	D20
QE[4]	B4	D21
QE[5]	B5	D22
QE[6]	B6	D16
QE[7]	B7 (MSB)	D17
QE[8]	G0 (LSB)	D7
QE[9]	G1	D8
QE[10]	G2	D9
QE[11]	G3	D12
QE[12]	G4	D13
QE[13]	G5	D14
QE[14]	G6	D10
QE[15]	G7 (MSB)	D11
QE[16]	R0 (LSB)	D0
QE[17]	R1	D1
QE[18]	R2	D2
QE[19]	R3	D3
QE[20]	R4	D4
QE[21]	R5	D6
QE[22]	R6	D27
QE[23]	R7 (MSB)	D5
HSYNC	HSYNC	D24
VSYNC	VSYNC	D25
DE	DATA EN	D26
	RSVD	D23
ODCK	CLK	CLKIN

Figure 4 shows the odd/even pin mapping for the DS90C387A following the VESA standard in Table 4, but the JEIDA standard is still shown for reference. There is an important caveat for 2-channel applications: different panels define “odd” versus “even” differently. Some users believe the first pixel (top-left) is odd, and some believe it is even. Table 4 and Figure 4 show the first pixel as odd. If used in a panel that defines the first pixel as even, then QO[0:23] and QE[0:23] must be swapped from what is shown in the table (that is, R10 maps to QE[16] and R20 maps to QO[16]). A0-A3 in Figure 4 then corresponds to even serialization instead of odd serialization, and A4-A7 corresponds to odd serialization instead of even serialization. Always check with the display-vendor’s mapping, as normally there is a mapping requirement listed in the datasheet for comparison.

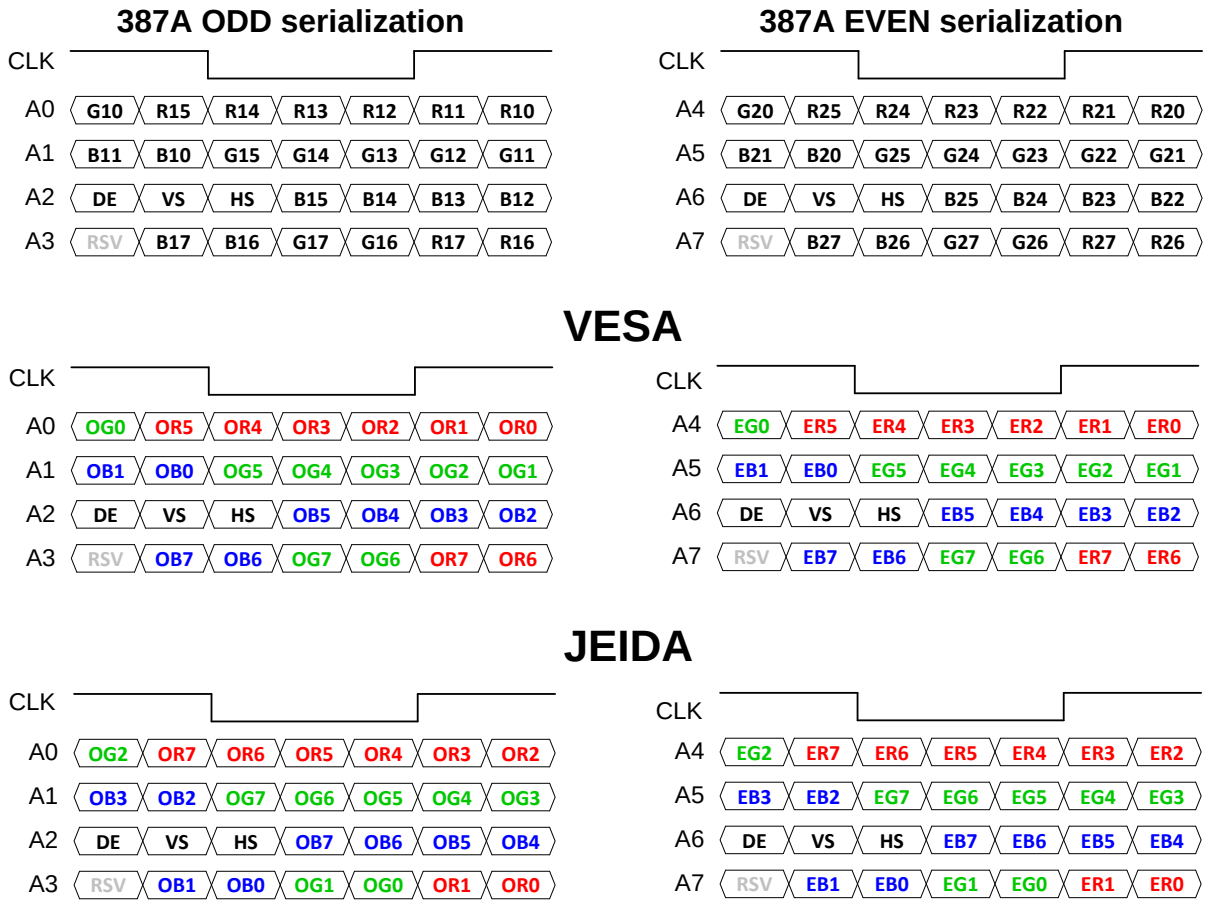

Figure 4. 2-Channel LVDS Connection Example

Table 4. 2-Channel LVDS Connection

DVI Output	Description	387A Input		DVI Output	Description	387A Input
QO[0]	Odd B0 (LSB)	B10		QE[0]	Even B0 (LSB)	B20
QO[1]	Odd B1	B11		QE[1]	Even B1	B21
QO[2]	Odd B2	B12		QE[2]	Even B2	B22
QO[3]	Odd B3	B13		QE[3]	Even B3	B23
QO[4]	Odd B4	B14		QE[4]	Even B4	B24
QO[5]	Odd B5	B15		QE[5]	Even B5	B25
QO[6]	Odd B6	B16		QE[6]	Even B6	B26
QO[7]	Odd B7 (MSB)	B17		QE[7]	Even B7 (MSB)	B27
QO[8]	Odd G0 (LSB)	G10		QE[8]	Even G0 (LSB)	G20
QO[9]	Odd G1	G11		QE[9]	Even G1	G21
QO[10]	Odd G2	G12		QE[10]	Even G2	G22
QO[11]	Odd G3	G13		QE[11]	Even G3	G23
QO[12]	Odd G4	G14		QE[12]	Even G4	G24
QO[13]	Odd G5	G15		QE[13]	Even G5	G25
QO[14]	Odd G6	G16		QE[14]	Even G6	G26
QO[15]	Odd G7 (MSB)	G17		QE[15]	Even G7 (MSB)	G27
QO[16]	Odd R0 (LSB)	R10		QE[16]	Even R0 (LSB)	R20
QO[17]	Odd R1	R11		QE[17]	Even R1	R21
QO[18]	Odd R2	R12		QE[18]	Even R2	R22
QO[19]	Odd R3	R13		QE[19]	Even R3	R23
QO[20]	Odd R4	R14		QE[20]	Even R4	R24
QO[21]	Odd R5	R15		QE[21]	Even R5	R25
QO[22]	Odd R6	R16		QE[22]	Even R6	R26
QO[23]	Odd R7 (MSB)	R17		QE[23]	Even R7 (MSB)	R27
HSYNC	HSYNC	HSYNC		DE	ENABLE	DE
VSYNC	VSYNC	VSYNC		ODCK	CLK	CLKIN

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2012) to A Revision **Page**

- Changed the The LVDS TX, Notes on Common Resolutions, and Design Guidelines section 2

Changes from A Revision (April 2013) to B Revision **Page**

- Updated all tables and images 1

Changes from B Revision (June 2018) to C Revision **Page**

- Changed the paragraph following Table 3 5

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