Application Report
SLAA921–December 2019

TAS2562 Schematic and Layout Guidelines

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ABSTRACT

In audio applications, it is always important to minimize the noise effects that may be induced by external conditions or even by the same components of the PCB. All the audio amplifiers require a clean and stable power supply to get the best performance. Any noise issue at the power supplies may be the cause of a high THD+N, SNR, and PSRR levels. In addition, the analog inputs and outputs require good noise immunity against the digital activity from nearby devices.

This document describes an optimized layout for the TAS2562 device in mono and stereo configuration. The goal of utilizing these layout guidelines is to minimize the noise issues and ensure the best device performance. The TAS2562EVM was taken as reference for the suggested guidelines.

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1 Mono Version

1.1 Typical Application Circuit

Figure 1 shows the typical application circuit for the TAS2562 device with the component names used in this document.

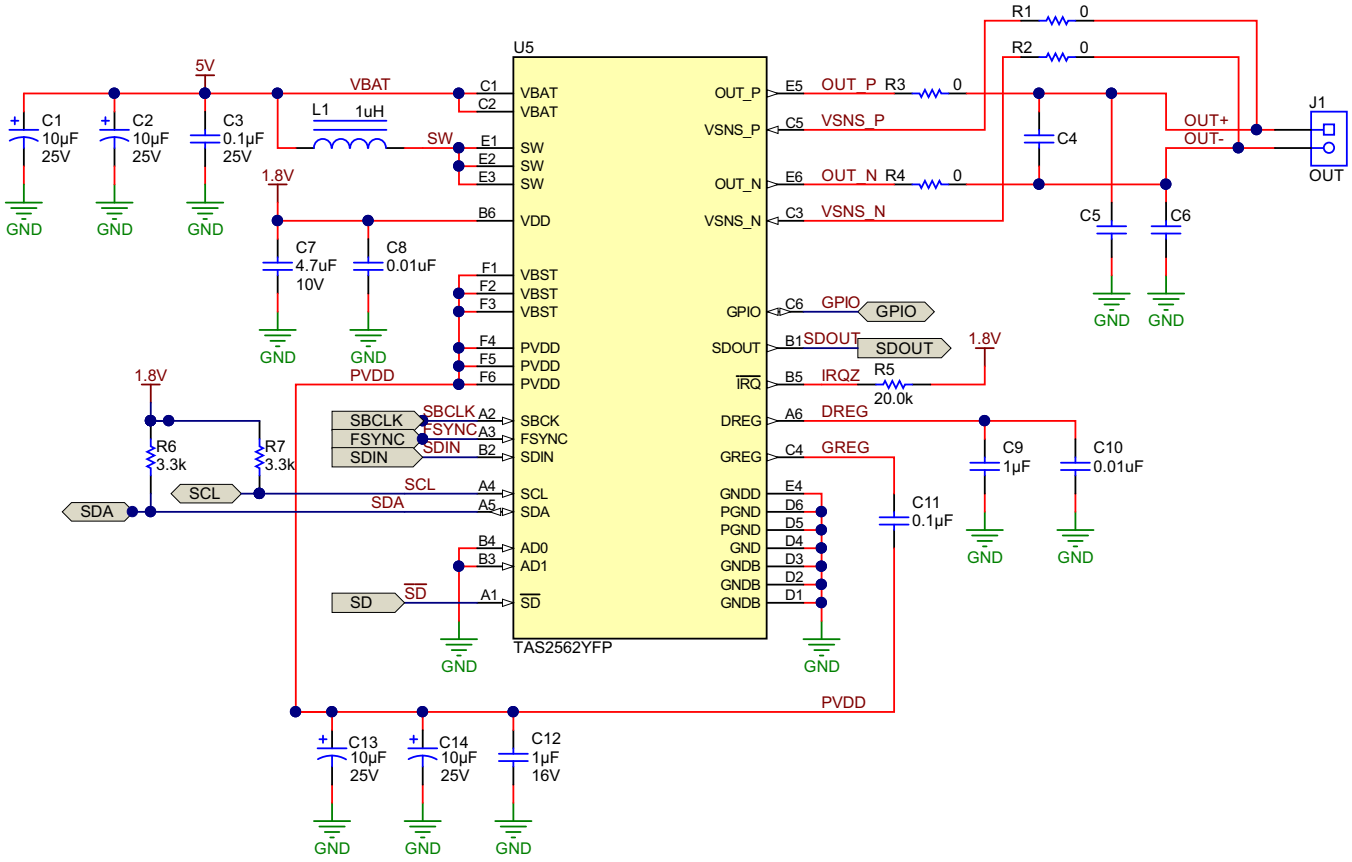

Figure 1. TAS2562 Schematic

Figure 2 and Figure 3 show the components location of the PCBA reference layout.

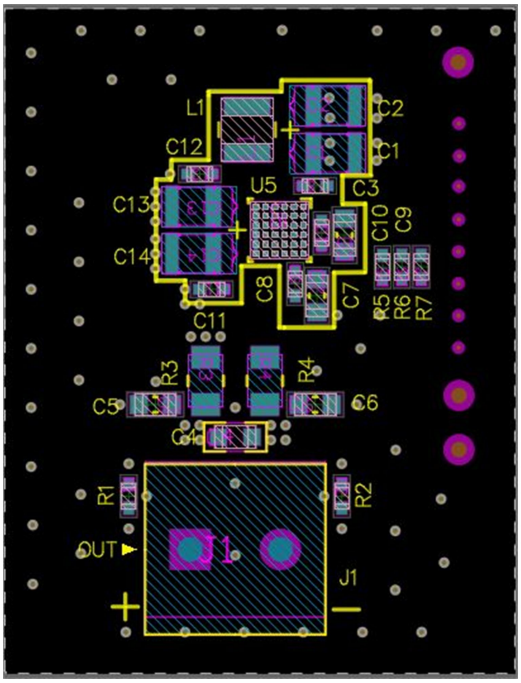

Figure 2. Components Location

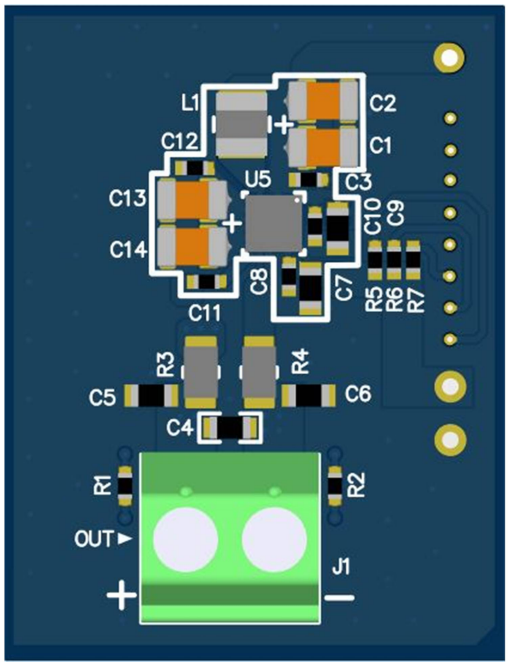

Figure 3. Components Location (3-D View)

Figure 4 illustrates the colors used for all the layout lines in this document.

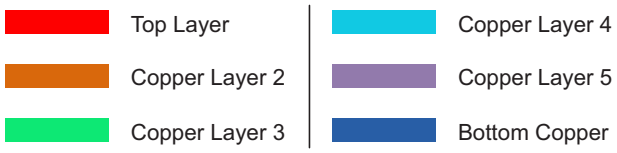

Figure 4. Layout Line Color Codes in This Document

For detailed information about the recommended external components, see Table 1.

1.2 GREG Pin

The GREG pin is the output of the high-side gate charge-pump regulator. As mentioned in the data sheet, this pin must not be connected to an external load. A minimum of 0.1-µF capacitor must be connected from the GREG pin to the PVDD pin (see Figure 1, for details).

TI recommends verifying that the PCB design does not generate a parasitic inductance higher than 200 pH. In addition, it is important to connect the GREG pin capacitor to PVDD with a star connection and not to the boost plane. This practice reduces the possibility of EMI radiation.

Similar to the ground pins connections, the layer changes should use multiple vias to minimize the parasitic inductance.

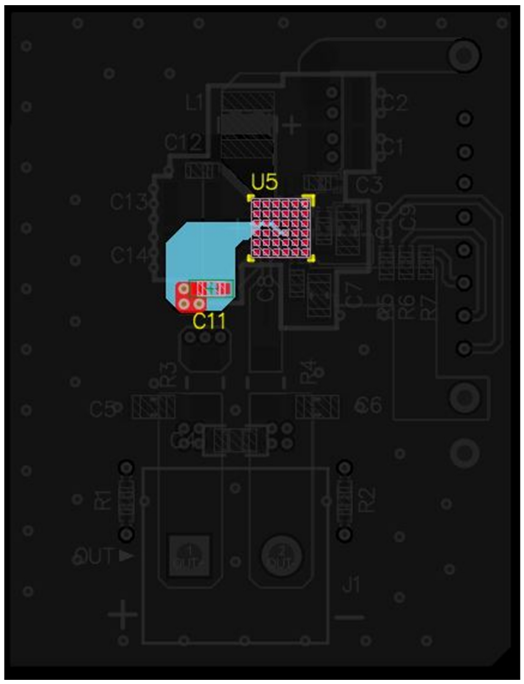

Figure 5. GREG Pin Connection

1.3 SW Pin

The boost inductor is selected to carry a high amount of current. Its saturation current should be higher than the limit current to deliver Class-D peak power. The PCB traces must be wide enough to handle this overcurrent limit.

The immediate layer below the top layer must be dedicated as a ground plane. A keepout region should be placed below the SW pin trace for noise reduction.

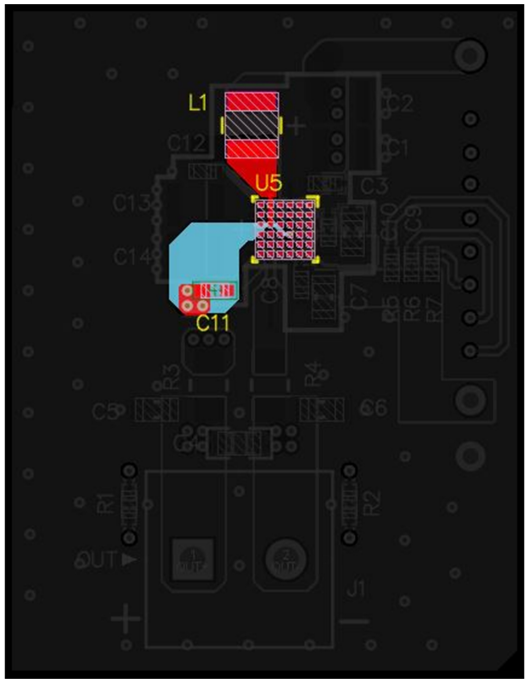

Figure 6. SW Pin

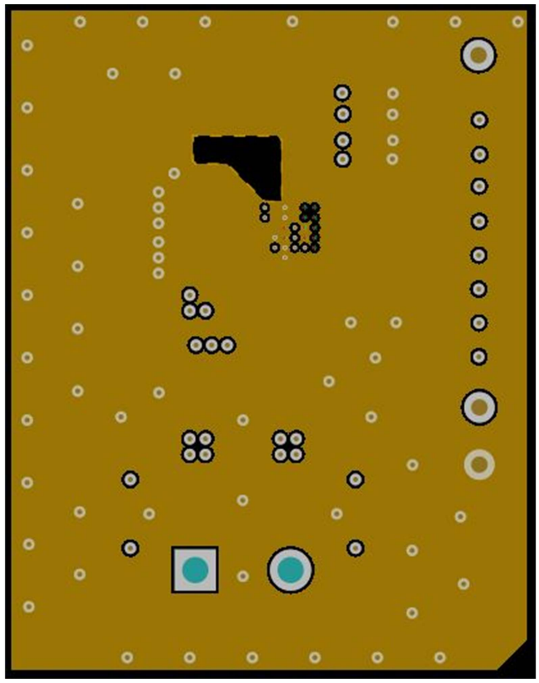

Figure 7. Ground Plane With Keepout Region

1.4 VBAT Pin

VBAT is the battery power supply input. This power pin supplies the internal boost. Since it carries a considerable amount of current, a decoupling capacitor is required. At least a 10-µF decoupling capacitor must be used to bypass VBAT to GND. See the *Decoupling Capacitors* section for details.

It is important to consider the following recommendations for VBAT:

1. Ensure that the parasitic inductance from the device pin to decoupling is below 500 pH.
2. Add an extra bulk decoupling capacitor to reduce overall THD+N at high power.
3. Have the VBAT traces wide enough to handle total output power.
4. Connect VBAT to and SW inductor through the thick plane.
5. Do not use vias between device pins and related capacitors and inductor.

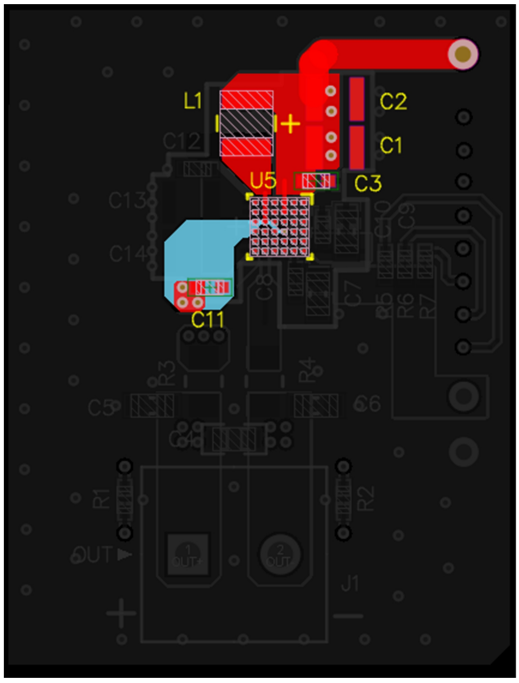

Figure 8. VBAT Pin Connection

1.5 DREG Pin

DREG is the digital core voltage regulator output. This pin must be bypassed to GND with a 1-µF capacitor and it must not be connected to an external load. TI recommends ensuring that both decoupling capacitor ends see as low inductance as possible between this DREG pin and GND. Multiple vias are suggested to reduce the inductance. See the *Decoupling Capacitors* section for details.

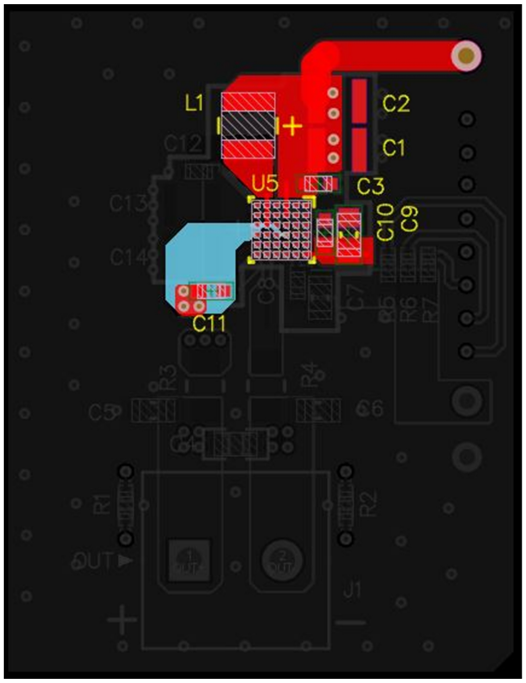

Figure 9. DREG Pin Connection

1.6 VBST and PVDD Pins

VBST is the internal boost converter output. This is the pin that will supply the power stage supply pin (PVDD). PVDD must be shorted to the VBST pin using a strong connection.

There are a few considerations that must be taken into account for the PVDD to VBST connection:

- VBST must not be connected to an external load. This pin should be bypassed to GND with a decoupling capacitor. The decoupling capacitor ends should see as low an inductance as possible between the VBST pin and the BGND pin. See the *Decoupling Capacitors* section for details.
- There should be a maximum parasitic inductance of 100 pH from the device pin to decoupling.
- VBST should be connected to PVDD through the thick plane (use multiple vias to reduce parasitic inductance).
- PVDD should be connected with a star connection to the GREG capacitor.
- VBST and PVDD traces carry a high amount of current. The traces should support currents up to the device overcurrent limit.
- Boost capacitor derating should satisfy the ratio with boost inductor: L/C < 1/3
- Ceramic capacitors derate with the applied DC voltage. Often, a 10-µF capacitor loses 80% of the nominal value at the 10-V to 12-V range (for example, a 10-µF capacitance value would result in 2 µF). Typically, it is recommended to use a 20-µF capacitor (or a pair of two 10-µF capacitors) as decoupling capacitor.

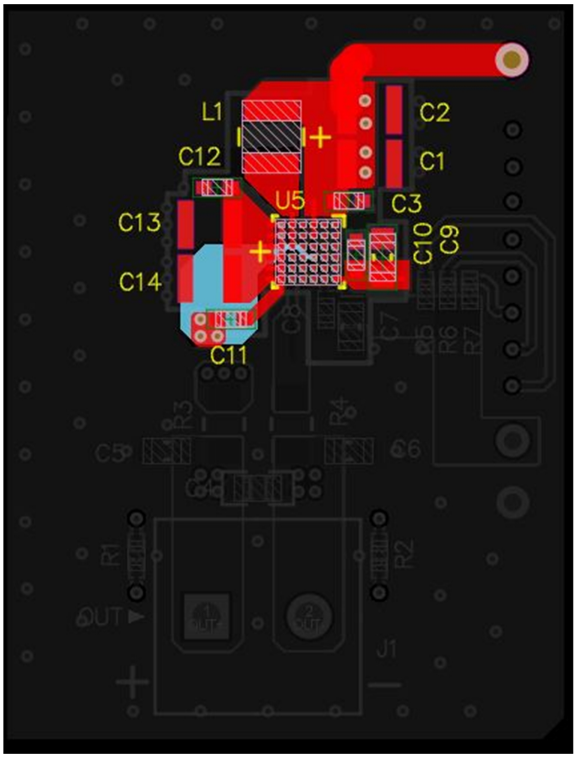

Figure 10. PVDD and VBST Pins Connection

1.7 VDD Pin

VDD is the analog, digital, and I/O power supply input. Similar to the VBAT pin, this power pin requires a decoupling capacitor. A minimum of 4.7-µF capacitor is suggested to bypass VDD to GND. See the *Decoupling Capacitors* section for details.

This pin requires having a maximum parasitic inductance of 200 pH.

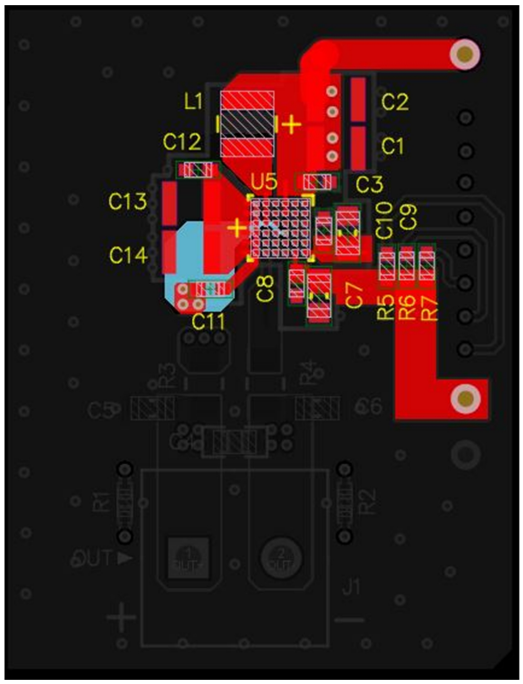

Figure 11. VDD Pin Connection

1.8 Output Pins (OUT_N and OUT_P)

OUT_N and OUT_P are the Class-D receiver channel negative and positive output, respectively. Due to its switching nature, TI recommends keeping the routing short to limit the emissions.

For optimal current flow, the PCB traces must be widened closely to the output pins. In addition, the outputs need to be routed on two layers using several vias to minimize parasitic impedance.

It is important to consider a few things when using an EMI filter (LC array):

- Inductance should be the first element in the filter.
- Capacitance to GND or other output will pull high-current spikes capable of triggering overcurrent protection.
- TI recommends fixing 1.5 MHz as the lower limit of the corner frequency to simplify the filter debug and noise issues.

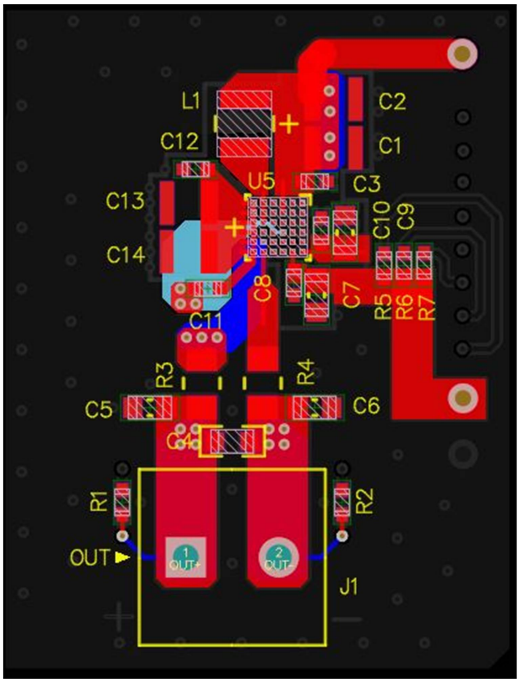

Figure 12. OUT_N and OUT_P Pin Connections

1.9 VSNS_N and VSNS_P Pins

VSNS_N and VSNS_P are the voltage sense negative and positive inputs, respectively. These inputs are connected to the Class-D outputs (VSNS_N to OUT_N and VSNS_P to OUT_P) after the ferrite bead filter.

When routing these pins to the ferrite bead filter, it is necessary to the make the connection to its respective output at the speaker terminal, not to a pin or trace. In addition, it is recommended to add a 1-kΩ resistor for each voltage sense path. This practice helps to reduce emissions and reduce ICN increments that result from the EMI filter.

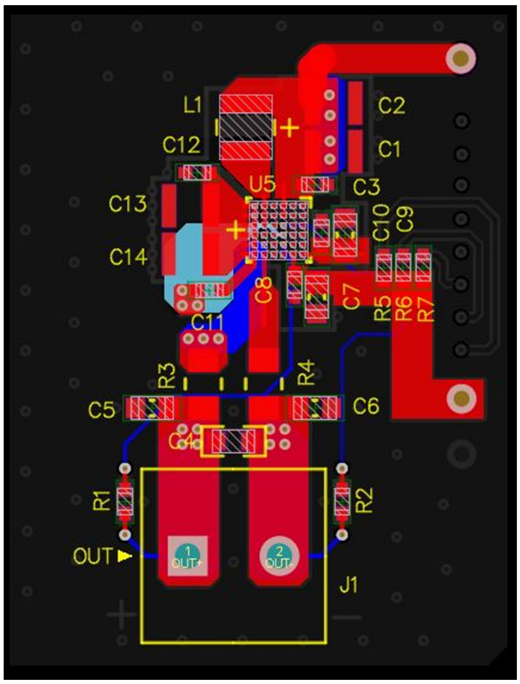

Figure 13. VSNS_N and VSNS_P Pin Connections

1.10 Digital Portion Connections

The TAS2562 device involves digital and analog activity. Care must be taken when routing the different signals since it may result in noise issues, especially from the digital lines to the analog portion.

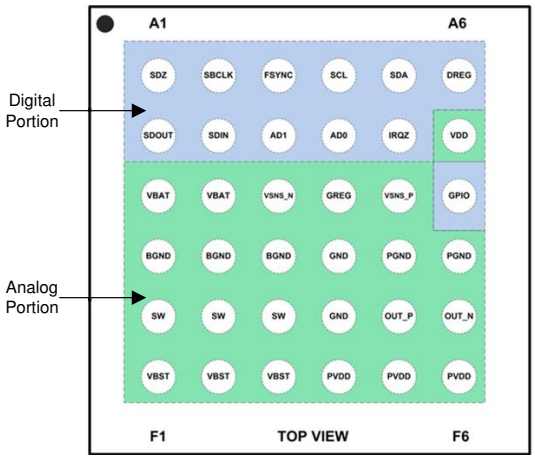

Figure 14. TAS2562 Analog and Digital Portions

The digital lines can reach frequencies up to 1 MHz for the I2C lines in *Fast-Mode Plus* and up to 50 MHz for the I2S lines. This high-frequency content can affect the performance of the analog signals. For measurement purposes, the digital noise level may affect the scope captures or a THD+N measurement.

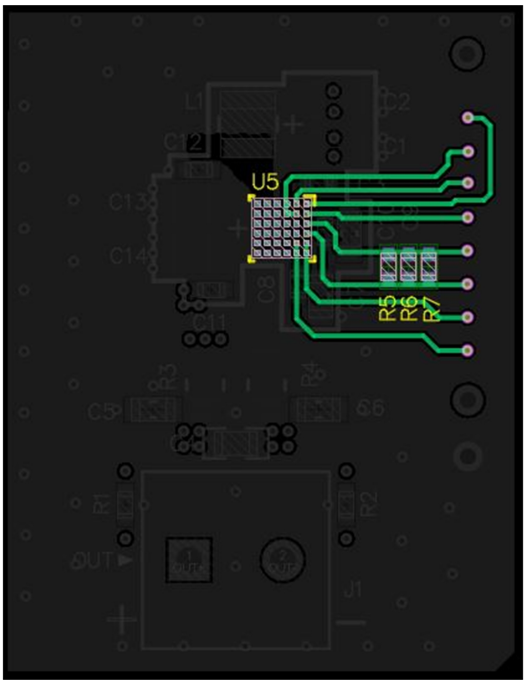

Figure 15. Digital Pins Connections

The TAS2562 device is already designed to separate the digital and analog traces. In Figure 16, the analog portion involves almost all the four pins lines C to F, while the digital portion is located in lines A and B. This structure allows routing the digital and analog planes separately.

1.11 Ground Pins (BGND, GND, and PGND)

The ground plane routing is important when designing the PCB layout. These planes must be designed to have a proper thermal dissipation and minimize the parasitic impedance as much as possible. Design tips for the different ground pins are listed here:

- All the ground pins must be shorted below the package and connected to the PCB ground plane through multiple vias.
- The vias are the best way to carry heat from the different sections in the board. Since the GND plane will need to quickly dissipate all the elevated temperatures, it is necessary to add multiple vias close to the ground pins.
- A maximum 150 pH of parasitic inductance is recommended. Having many vias reduces the additional impedance and provides good conduction in both electrical and thermal perspective.
- An entire layer immediately below the top layer must be dedicated to GND, as best practice.

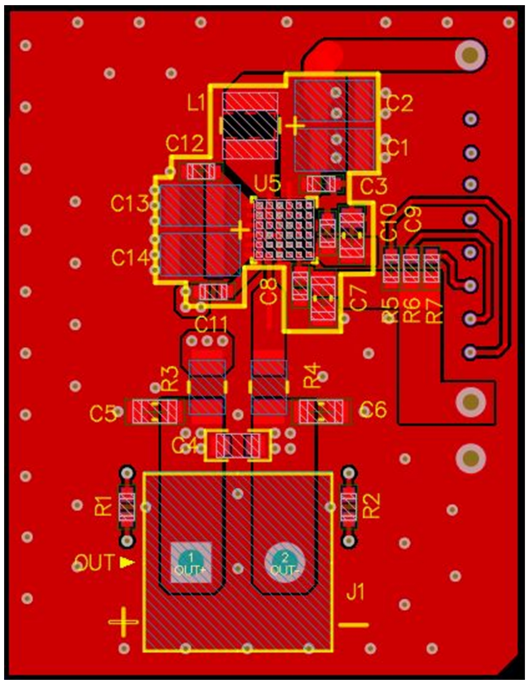

Figure 16. Top Layer

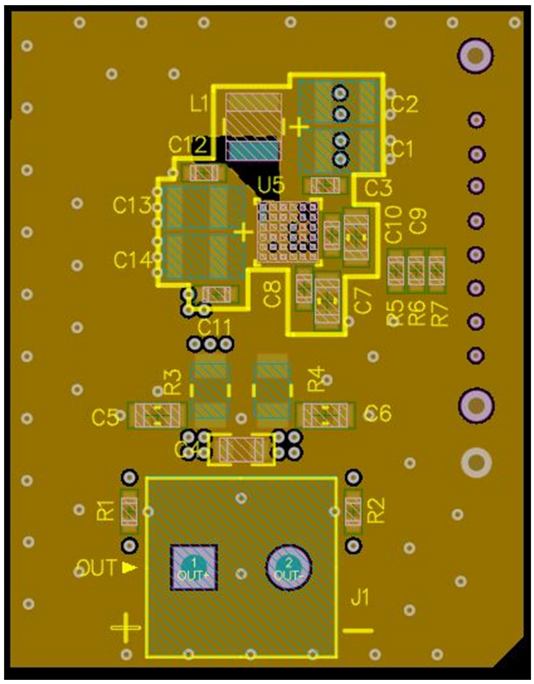

Figure 17. Copper Layer 2 (GND Exclusive Layer)

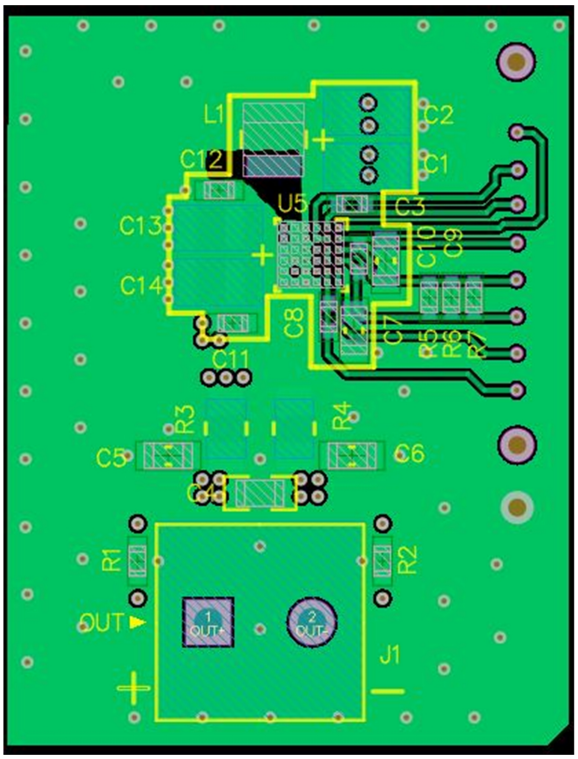

Figure 18. Copper Layer 3

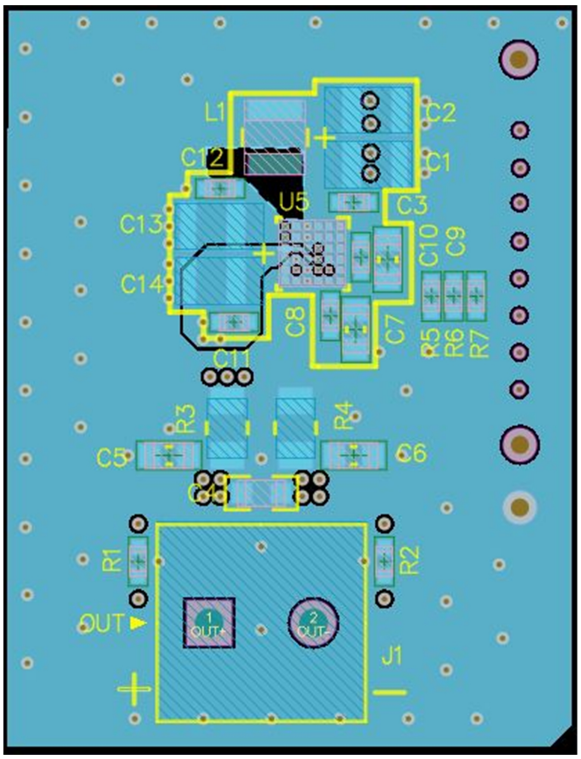

Figure 19. Copper Layer 4

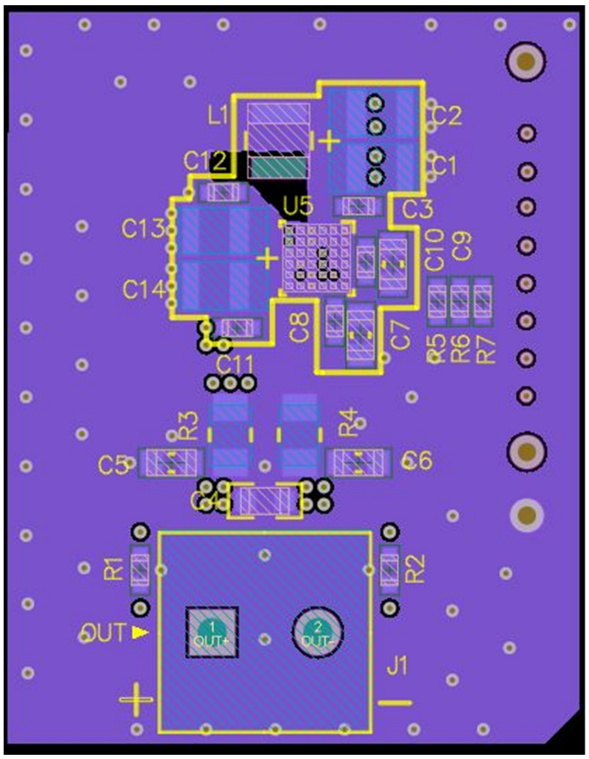

Figure 20. Copper Layer 5

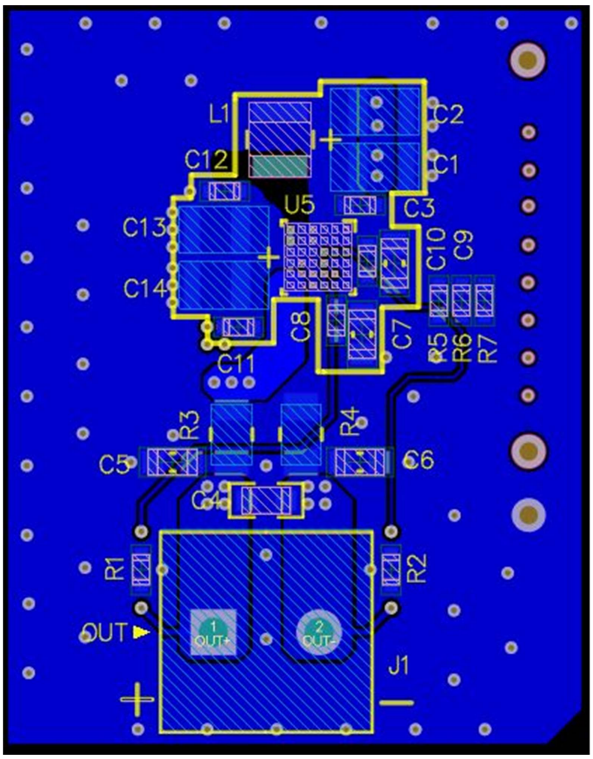

Figure 21. Bottom Layer

2 Stereo Version

2.1 Typical Application Circuit

Figure 22 shows the TAS2562 in stereo configuration.

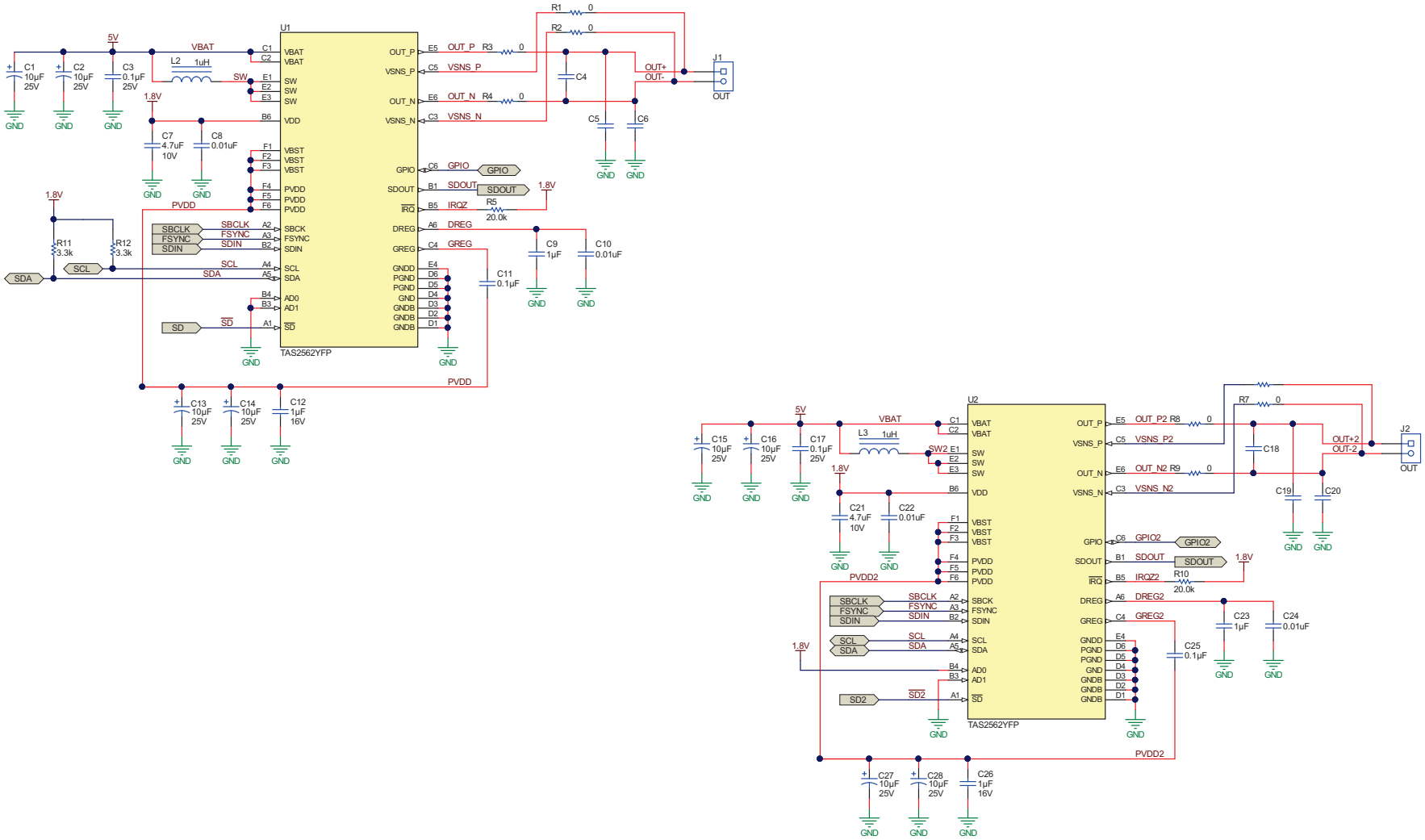

Figure 22. TAS2562YFP Stereo Schematic

Figure 23 and Figure 24 show the component locations of the PCBA reference layout.

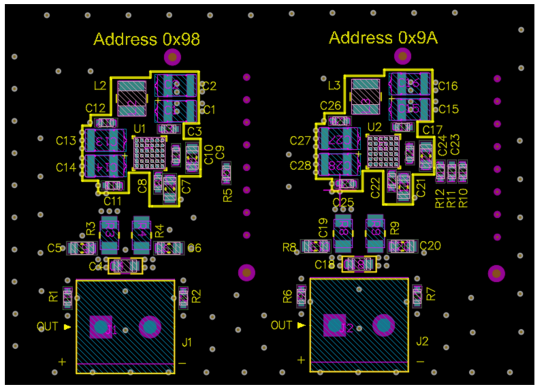

Figure 23. Components Location (Stereo)

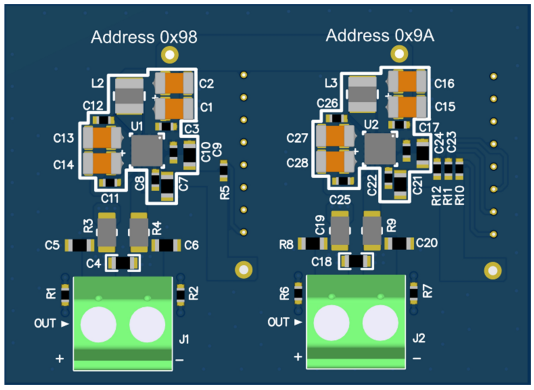

Figure 24. Components Location (3-D View, Stereo)

Table 1. Recommended External Components

Component	Description	Specification	MIN	TYP	MAX	Unit
L2, L3	Boost converter inductor	Inductance, 20% tolerance	0.47	1		µH
		Saturation current		4.5		A
N/A	EMI filter inductors (optional). These are not recommended because it degrades THD+N performance. The TAS2562 device is a filter-less class-D and does not require these bead inductors.	Impedance at 100 MHz		120		Ω
		DC resistance			0.095	Ω
		DC current			2	A
		Size		0402		EIA
C1, C2, C15, C16	Boost converter input capacitor	Capacitance, 20% tolerance	10			µF
C13, C14, C27, C28	Boost converter output capacitor	Type	X5R			
		Capacitance, 20% tolerance	10		47	µF
		Rated voltage	16			V
		Capacitance at 11.5 V derating	3.3			µF
N/A	EMI filter capacitors (optional, must use L2, L3 if C3, C4 used)	Capacitance		1		nF
C7, C21	VDD decoupling capacitor	Capacitance	4.7			µF
C9, C23	DREG decoupling capacitor	Capacitance	1			µF
C11, C25	GREG Fly capacitor	Capacitance	100			nF

For more information, see the *TAS2562 6.1-W Boosted Class-D Audio Amplifier with IV Sense* data sheet.

2.2 GREG Pin (Stereo)

The GREG pins for the stereo version have the same recommendations as stated in Section 1.2.

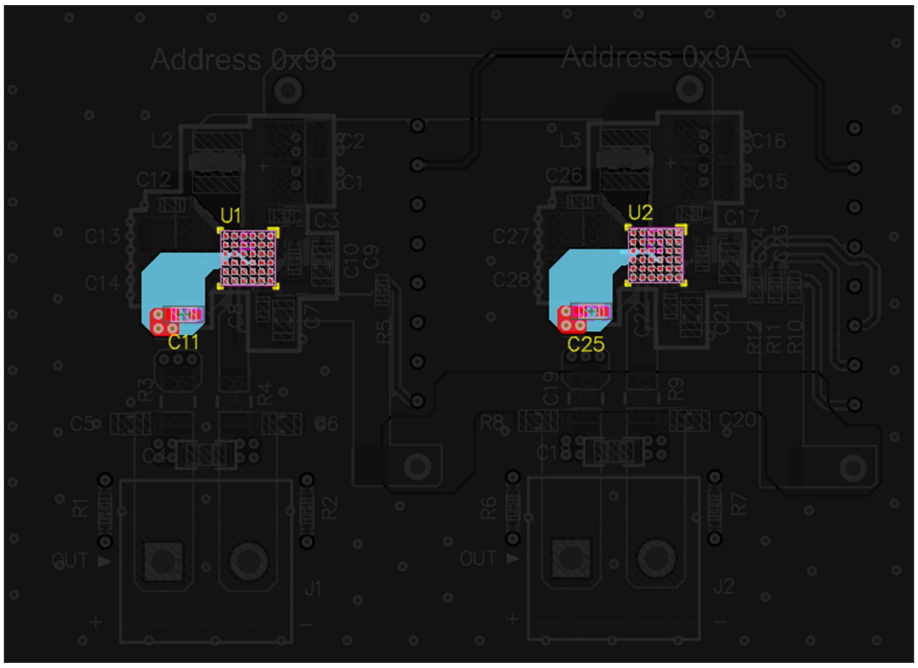

Figure 25. GREG Pin Connection (Stereo)

2.3 SW Pin (Stereo)

The GREG pins for the stereo version have the same considerations as stated in Section 1.3.

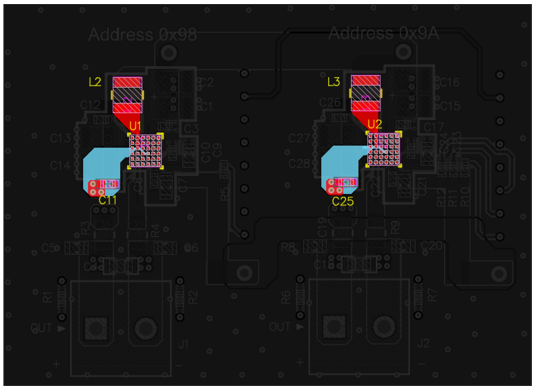

Figure 26. SW Pin Connection (Stereo)

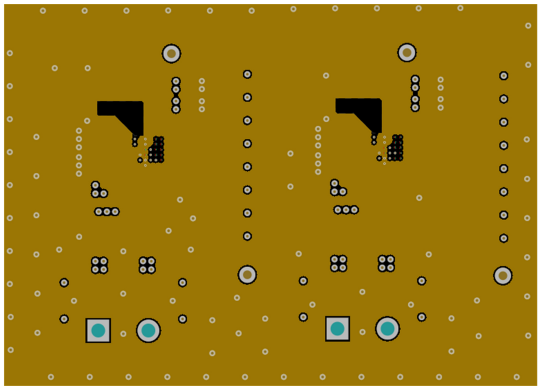

Figure 27. Ground Plane With Keepout Region (Stereo)

2.4 VBAT Pin (Stereo)

The VBAT pins for the stereo version have the same considerations as stated in Section 1.4.

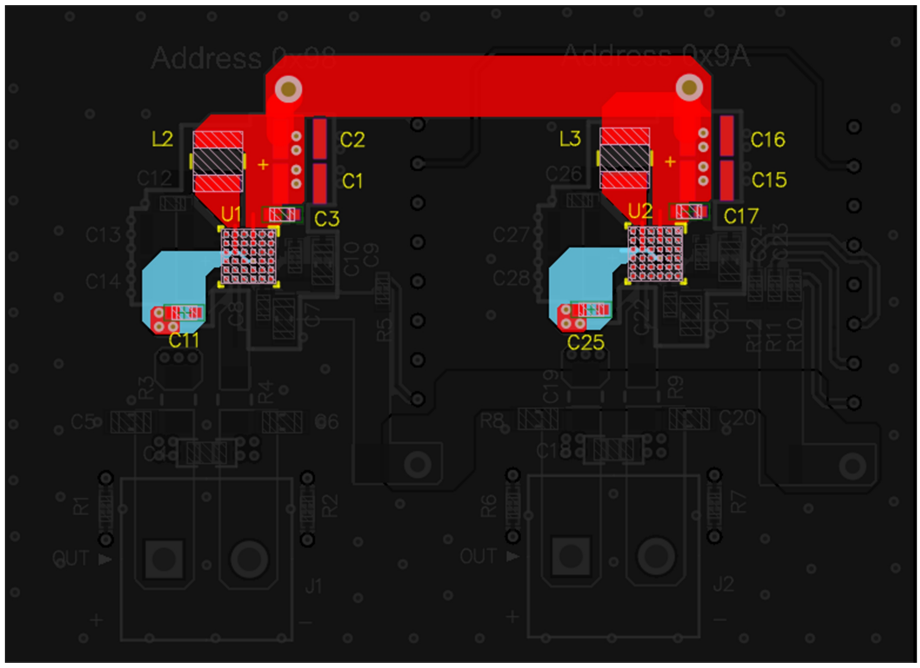

Figure 28. VBAT Pin Connection (Stereo)

2.5 DREG Pin (Stereo)

The DREG pins for the stereo version have the same considerations as stated in Section 1.5.

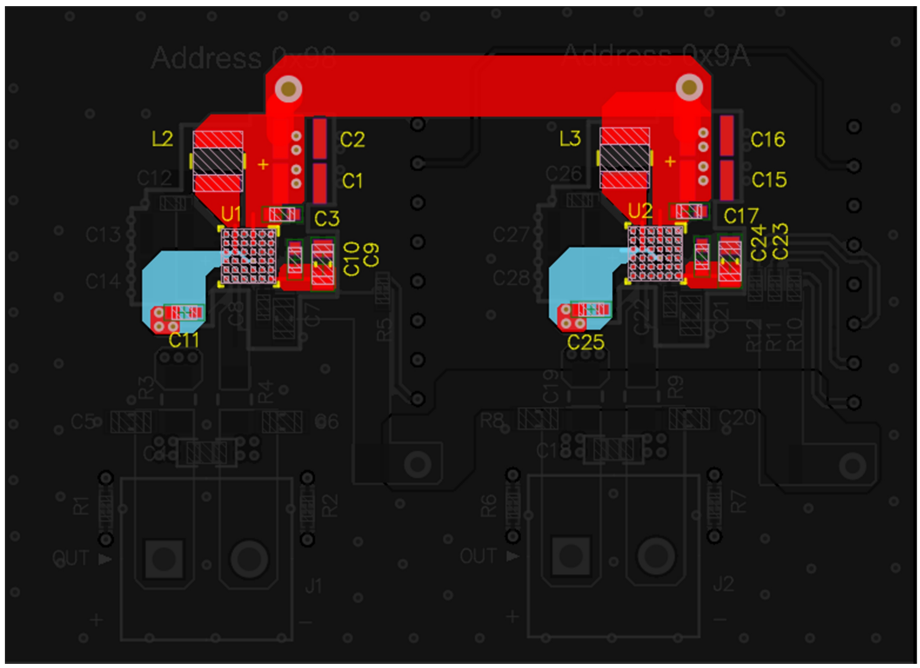

Figure 29. DREG Pin Connection (Stereo)

2.6 VBST and PVDD Pins (Stereo)

The VBST and PVDD pins for the stereo version have the same considerations as stated in BVST and PVDD Pins.

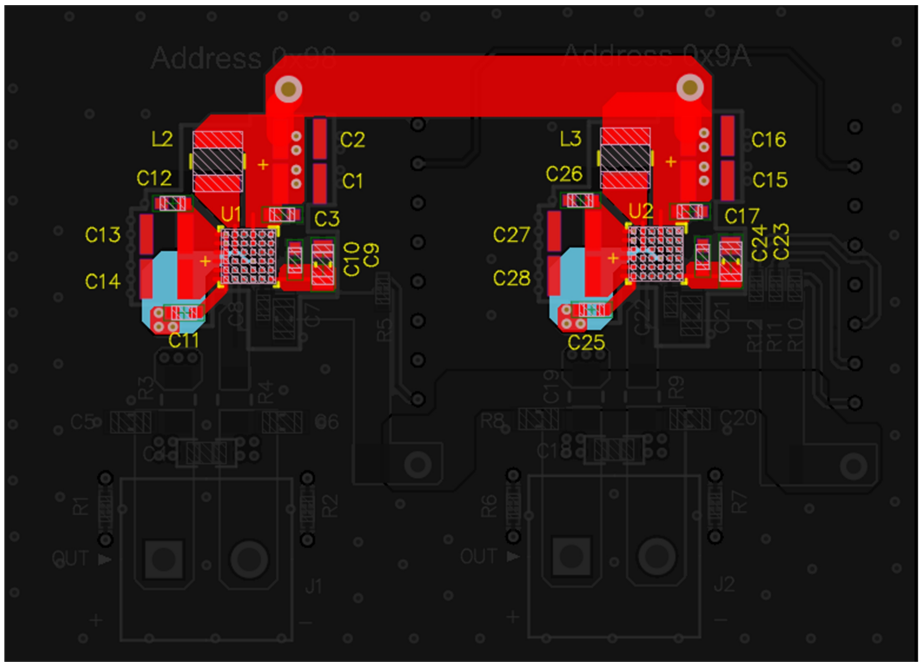

Figure 30. VBST and PVDD Pins Connection (Stereo)

2.7 VDD Pin (Stereo)

The VDD pin for the stereo version has the same considerations as stated in Section 1.7.

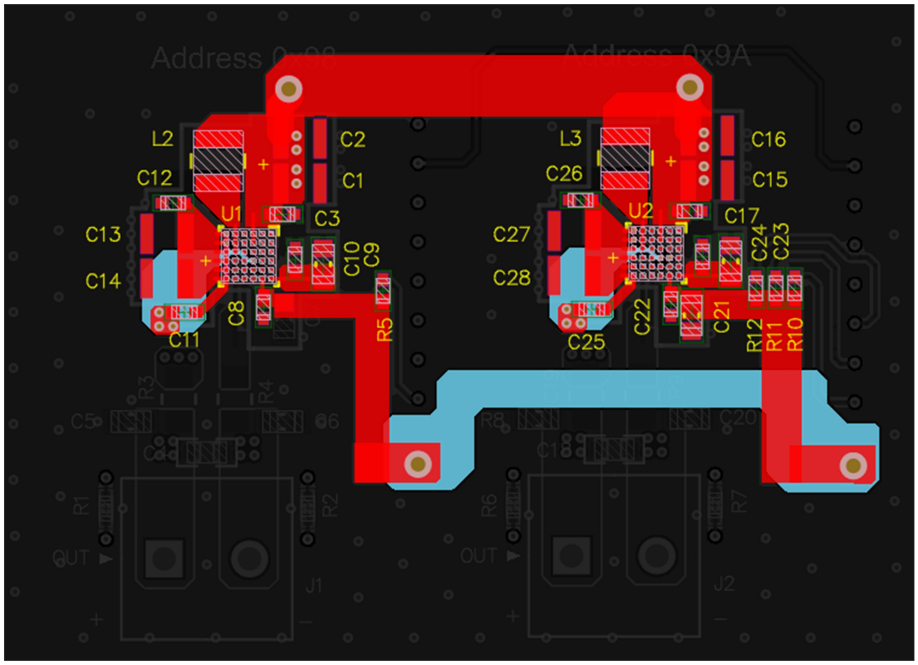

Figure 31. VDD Pin Connection (Stereo)

2.8 Output Pins (OUT_N and OUT_P, Stereo)

The output pins (OUT_N and OUT_P) for the stereo version have the same considerations as stated in Section 1.8.

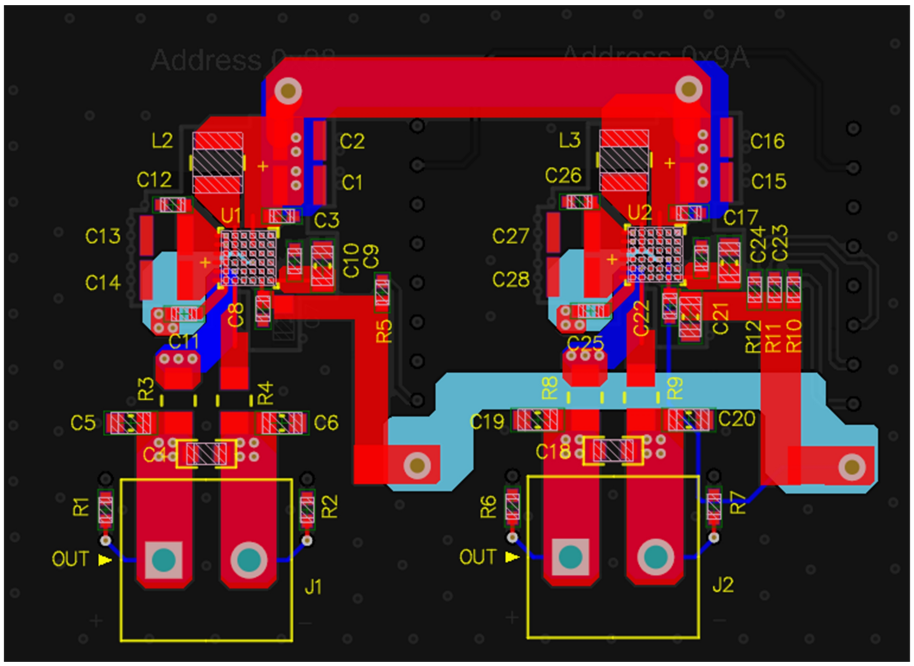

Figure 32. OUT_N and OUT_P Pins Connection (Stereo)

2.9 VSNS_N and VSNS_P Pins (Stereo)

The VSNS_N and VSNS_P pins for the stereo version have the same considerations as stated in Section 1.9.

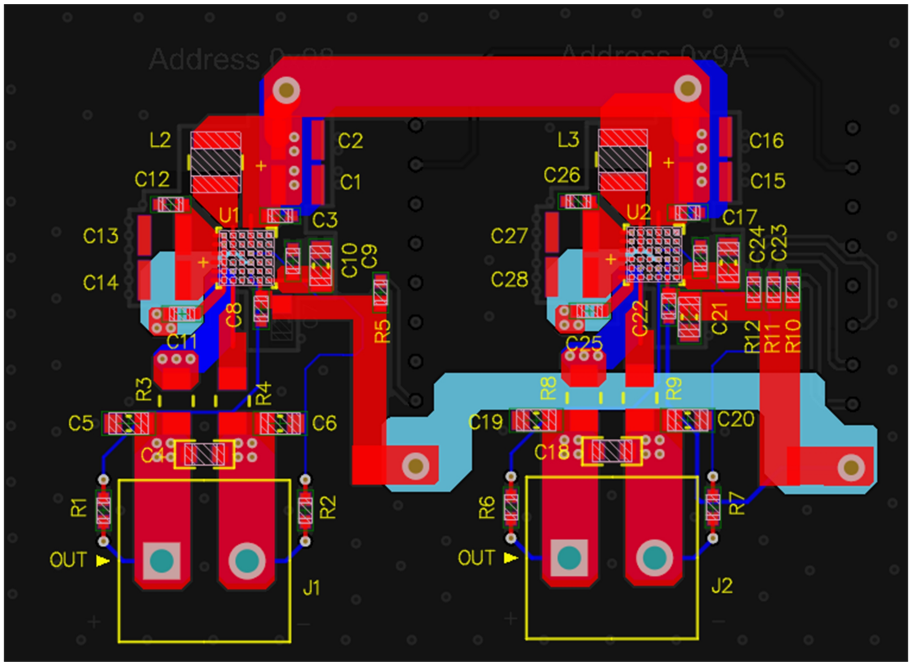

Figure 33. VSNS_N and VSNS_P Pins Connection (Stereo)

2.10 Digital Portion Connections (Stereo)

The digital portion connections for the stereo version have the same considerations as stated in Section 1.10.

In addition, care must be taken when routing the digital pins between both TAS2562 channels. Avoid routing the digital traces below the traces with switching activity such as the SW pin. Otherwise, there could be noise on the digital portion and may cause a wrong activity.

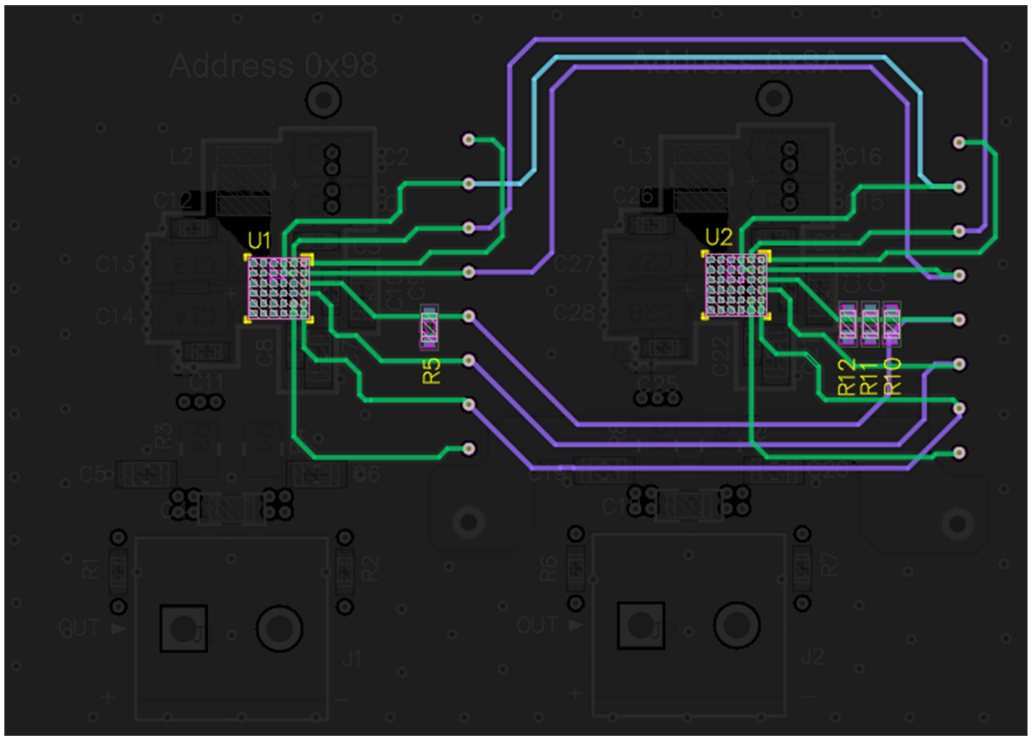

Figure 34. Digital Pins Connections

2.11 Ground Pins (BGND, GND, and PGND)

The ground pins (BGND, GND, and PGND) for the stereo version have the same considerations as stated in Section 1.11.

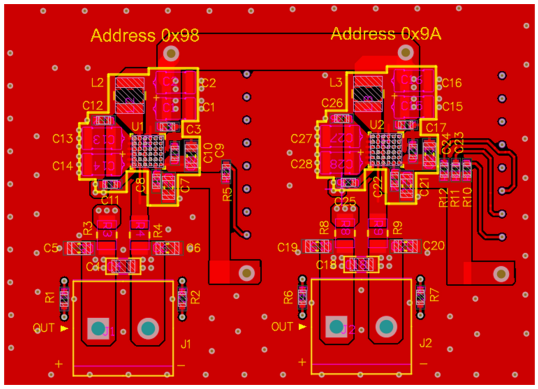

Figure 35. Top Layer (Stereo)

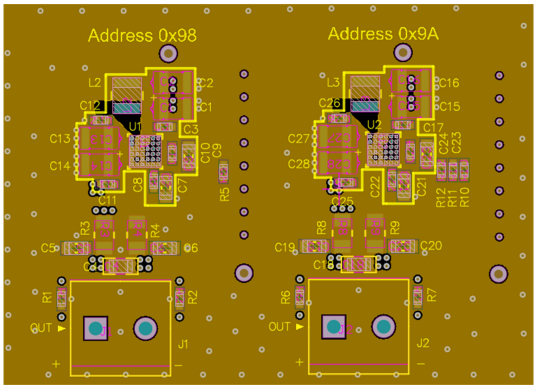

Figure 36. Copper Layer 2 (GND Exclusive Layer)

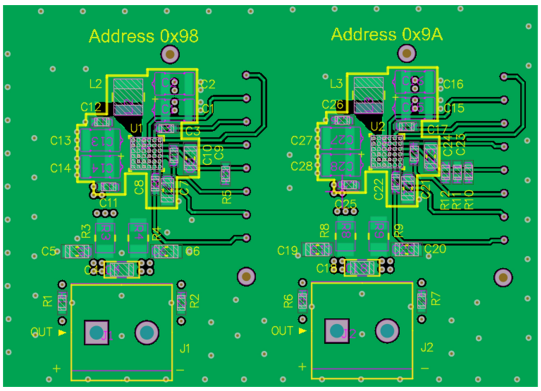

Figure 37. Copper Layer 3

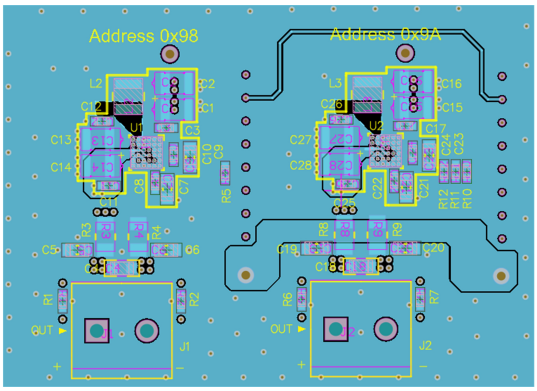

Figure 38. Copper Layer 4

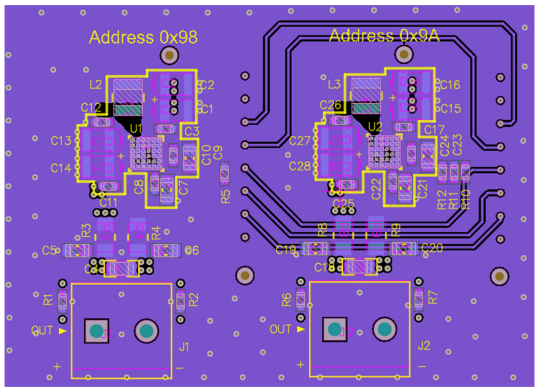

Figure 39. Copper Layer 5

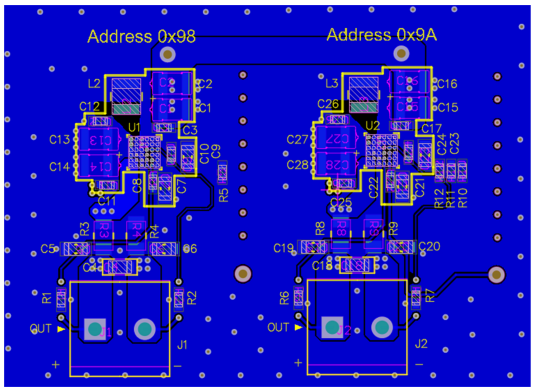

Figure 40. Bottom Layer

3 Bill of Materials (BOM)

Table 2 details the bill of materials.

Table 2. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C1, C2, C13, C14, C15, C16, C27, C28	8	10 µF	CAP, TA, 10 µF, 25 V, 10%, 2 Ω, SMD	3.2 mm × 1.7 mm	F951E106KAAAQ2	AVX		
C7, C21	2	4.7 µF	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603	0603	CGB3B1X5R1A475K055AC	TDK		
C4, C5, C6, C9, C12, C18, C19, C20, C23, C26	10	1 µF	CAP, CERM, 1 µF, 16 V,±20%, X7R, 0603	0603	CL10B105MO8NNWC	Samsung		
C3, C11, C17, C25	4	0.1 µF	CAP, CERM, 0.1 µF, 25 V,±10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1E104K050BB	TDK		
C8, C10, C22, C24	4	0.01 µF	CAP, CERM, 0.01 µF, 25 V, ±10%, X7R, 0402	0402	GCM155R71E103KA37D	MuRata		
J1, J2	2		Conn Term Block, 2POS, 3.81 mm, TH	2POS Terminal Block	1727010	Phoenix Contact		
L1, L2, L3	3	1 µH	Inductor, Shielded, Metal Composite, 1 µH, 3.3 A, 0.04 Ω, SMD	2.5 mm × 1.2 mm × 2 mm	DFE252012F-1R0M=P2	MuRata Toko		
R3, R4, R8, R9	4	0 Ω	RES, 0, 5%, 0.125 W, 0805	0805	RC0805JR-070RL	Yageo America		
R5, R10	2	20.0 kΩ	RES, 20.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT3K3	Stackpole Electronics Inc		
R11, R12	2	3.3 kΩ	RES, 3.3 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT3K3	Stackpole Electronics Inc		
R1, R2, R6, R7	4	0 Ω	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic		
U1, U2, U5	3		6W Boosted Class-D Audio Amplifier with IV-sense, YFP0036-C02 (DSBGA-36)	YFP0036-C02	TAS2562YFPR	Texas Instruments	TAS2562YFPT	Texas Instruments

4 Decoupling Capacitors

All the PCB routes have defined impedance that must be considered during all design stages. These signal paths will act as additional components in the board. In addition, the PCB lines have a parasitic inductance and capacitance that result in a different power distribution.

To reduce the negative effects of all these parasitic impedances, we recommend that the VBAT and VDD decoupling capacitor connections respect the following rules:

- **Place the decoupling capacitor close to the device pin in the same layer.** The decoupling capacitor stores local charge and supplies the large transient currents when it is required. The TAS2562 device has many switching activity and voltage fluctuations that demand large current transients in a short period of time. In addition, the parasitic effects caused by the vias, traces, and pads generate a voltage drop in the power supply. The proximity of the decoupling capacitors to the power pins compensates these effects and supplies the large transient currents when it is required. On a multi-layer board, the capacitors must be placed in the same layer where the TAS2562 device is located. Otherwise, the decoupling capacitor value may be reduced by the additional capacitance due to the vias connections.
- **Place the VDD and GND vias as close as possible to the decoupling capacitors.** If possible, place the vias directly or the closest as possible to the capacitor mounting pads. The vias have defined impedance determined by its length and diameter. This impedance may cause a voltage drop (in high-frequency applications the signal integrity is greatly influenced) and a current flow that must be reduced or avoided. For that reason, it is recommended to add many vias around the mounting pads. This practice reduces the parasitic impedance.

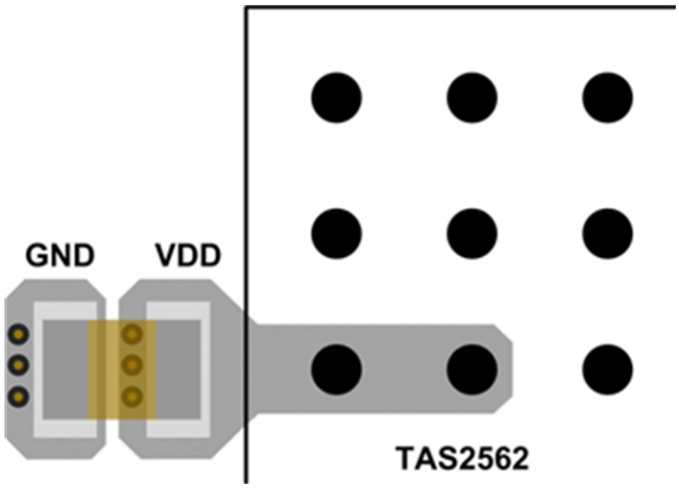

Figure 41. VIAS Placement

Refer all the pins that require a decoupling capacitor to this section for detailed information.

5 Layout Guidelines Summary

Table 3 summarizes the layout guidelines.

Table 3. Layout Guidelines Summary

Name	Pin	Description	Typical Component Value	Component Instructions	Layout Instructions	Priority
BGND	D1, D2, D3	Boost ground. Connect to PCB GND plane.			Maximum 150-pH parasitic inductance. Short BGND, GND, GNDD, PGDN below the package and connect them to PCB ground plane strongly through multiple vias. Minimize inductance as much as possible	Critical
GND	D4, E4	Digital ground. Connect to PCB GND plane.			Maximum 150-pH parasitic inductance. Short BGND, GND, GNDD, PGDN below the package and connect them to PCB ground plane strongly through multiple vias. Minimize inductance as much as possible	Critical
GREG	C4	High-side gate CP regulator output. Do not connect to external load	100 nF	Connect between GREG and PVDD. Connection to PVDD should be a star connection instead of connecting to decoupling route. Layer changes should use multiple vias to minimize parasitic inductance	Maximum 200-pH parasitic inductance. Connect it to PVDD with a star connection and not to boost plane. Do not connect to external load.	Critical
PGND	D5, D6	Power stage ground. Connect to PCB GND plane			Maximum 150-pH parasitic inductance. Short BGND, GND, GNDD, PGDN below the package and connect them to PCB ground plane strongly through multiple vias. Minimize inductance as much as possible	Critical
SW	E1, E2, E3	Boost converter switch input	1 µH	Inductor connects between SW and VBAT.	Connect to VBAT with boost inductor. Reduce parasitic capacitor and resistance for efficiency. Boost inductor should be as close as possible to the SW pin. Inductor should be connected to SW through thick plane. Traces should support currents up to device over-current limit. Ground bounce can be reduced by placing a keep out below this trace and preventing any signal from routing beneath. Do not route digital under this net.	Critical
VBAT	C1, C2	Battery power supply input. Connect to 2.7 V to 5.5-V supply and decouple with a capacitor	10 µF	Extra bulk decoupling may help reduce overall THD+N at high power by preventing supply droop	Maximum 500-pH parasitic inductance from device pin to decoupling. Bypass to GND with capacitor. Should be connected to inductor through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBAT pin and PGND pin. Routing from VBAT should be wide enough to handle total output power.	Critical
DREG	A6	Digital core voltage regulator output. Bypass to GND with a cap. Do not connect to external load.	1 µF		Maximum 500-pH parasitic inductance from device pin to decoupling. Bypass to GND with capacitor. Do not connect to external load. Both ends of decoupling cap should see as low inductance as possible between this pin and GND pins.	High

Table 3. Layout Guidelines Summary (continued)

Name	Pin	Description	Typical Component Value	Component Instructions	Layout Instructions	Priority
PVDD	F4, F5, F6	Power stage supply.	20 µF	Capacitor derating should satisfy ratio of L/C < 1/3 with respect to Boost inductor. Considering component tolerances, should target no less than 3.3 µF at a typical 11.5 V Boost when using a 1 - µH inductor. This requirement requires checking the DC bias derating of the capacitor. 16 V capacitors typically are derated by around 80% at the boost voltage.	Maximum 100-pH parasitic inductance from device pin to decoupling. Short it to VBST(boost) plane through strong connection. Connect it to GREG with a star connection and not to boost plane.	High
VBST	F1, F2, F3	Boost converter output. Do not connect to external load.	20 µF	Capacitor derating should satisfy ratio of L/C < 1/3 with respect to Boost inductor. Considering component tolerances, should target no less than 3.3 µF at a typical 11.5 V Boost when using a 1-µH inductor. This requirement requires checking the DC bias derating of the capacitor. 16 V capacitors typically are derated by around 80% at the boost voltage.	Maximum 100-pH parasitic inductance from device pin to decoupling. Do not connect to external load. Bypass to GND with capacitor. Connect to PVDD through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBST pin and BGND pin. Traces should support currents up to device over-current limit.	High
VDD	B6	Analog, digital, and I/O power supply. Connect to 1.8-V supply and decouple to GND with a capacitor.	4.7 µF		Maximum 200-pH parasitic inductance from device pin to decoupling. Bypass to GND with capacitor. Both the end of decoupling cap should see as low inductance as possible between this pin and GND pin	High
OUT_N	E6	Class-D negative output for receiver channel.		If using an EMI filter, inductance should be the first element in the filter. Capacitance to GND or other output will pull high current spikes capable of triggering over current protection. It is recommended to set the filter corner frequency no lower than 1.5 MHz.	Route with wide traces to speaker connection. Make Vsense connections as close to speaker as possible. Keep route short to limit emissions.	Medium
OUT_P	E5	Class-D positive output for receiver channel		If using an EMI filter, inductance should be the first element in the filter. Capacitance to GND or other output will pull high current spikes capable of triggering over current protection. It is recommended to set the filter corner frequency no lower than 1.5 MHz.	Route with wide traces to speaker connection. Make Vsense connections as close to speaker as possible. Keep route short to limit emissions.	Medium
VSNS_N	C3	Voltage sense negative input. Connect to Class-D out_N output after ferrite bead filter	1 kΩ	Additional place holder for series resistance may be beneficial with limiting emissions	Make connection to OUTN at speaker terminal	Medium
VSNS_P	C5	Voltage sense positive input. Connect to Class-D Out_P output after ferrite bead filer.	1 kΩ	Additional place holder for series resistance may be beneficial with limiting emissions	Make connection to OUTN at speaker terminal	Medium
FSYNC	A3	I2S word clock or TDM frame sync for ASI1 and ASI2 channels				Low
SBCLK	A2	ASI1 channel I2S/TDM serial bit clock.				Low
SCL	A4	I2C Mode: I2C clock pin. Pull up to VDD with a resistor. SPI Mode: active low chip select.				Low
SDA	A5	I2C Mode: I 2C Data Pin. Pull up to VDD with a resistor. SPI Mode: Serial data input pin				Low

Table 3. Layout Guidelines Summary (continued)

Name	Pin	Description	Typical Component Value	Component Instructions	Layout Instructions	Priority
SDIN	B2	ASI1 channel I2S/TDM serial data input				Low
SDOUT	B1	ASI1 channel I2S/TDM serial data output				Low
AD0	B4	I2C Mode - Address selection pin See General I2C operation. SPI Mode - SPI clock				Not critical
AD1	B3	I2C Mode - Address selection pin See General I2C operation. SPI Mode - SPI clock				Not critical
IRQZ	B5	Open drain, active low interrupt pin. Pull up to VDDD with resistor if optional internal pull up is not used.	10 kΩ			Not critical
SDZ	A1	Active low hardware shutdown.				Not critical
GPIO	C6	General purpose I/O, no connect if not used		Additional place holder for series resistance may be beneficial with limiting emissions	Make connection to OUTP at the speaker terminal	Not critical

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