Application Report
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Maximum Clock Frequency of I2C Bus Using Repeaters

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ABSTRACT

In this application report we show how to calculate the maximum clock frequency (f_{SCL} (max)) of an I2C bus when using a repeater. The propagation delays added by the repeater are included in the timing budget calculations and shown to limit the maximum clock frequency in the case of I2C FM+ bus.

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1 Introduction

The I2C communication standard is a widely used inter-chip communication standard in today's electronic systems. The I2C standard limits the maximum allowed capacitance on the bus to 400 pF for I2C fast mode (FM) and 550 pF for I2C fast mode plus (FM+). With ever-growing system complexity more and more integrated circuits (IC's) are added to the I2C bus and complying with the I2C spec capacitance limit has become a concern. Each IC added results in a capacitance increase up to approximately 15 pF on the I2C bus. I2C repeaters are circuits which provide a solution to the previously described problem by isolating the capacitance between two I2C bus, hence, allowing greater capacitance on an I2C bus for a given timing budget.

The maximum clock frequency (f_{SCL} (max)) is specified to be up to 400 kHz for I2C FM and up to 1000 kHz for FM+ spec. With the increasing number of devices, application requirements also tend to dictate faster operating frequencies to improve overall system response time. Since I2C repeaters typically buffer both the clock (SCL) and the data (SDA) lines, an I2C system utilizing I2C repeaters must properly account for the propagation delays through the repeater when determining the optimal operating frequency. In this article we show the calculations that can be used to determine the maximum clock frequency on an I2C bus-based on repeater propagation delays. The trade-offs that need to be considered between system design parameters and timing budget requirements are also discussed.

2 I2C Bus Without a Repeater

The timing diagram for an I2C bus with a master generating the SCL clock signal and a slave responding with data on SDA is shown in Figure 1 (refer to the I2C spec for a detailed description of the timing parameters).

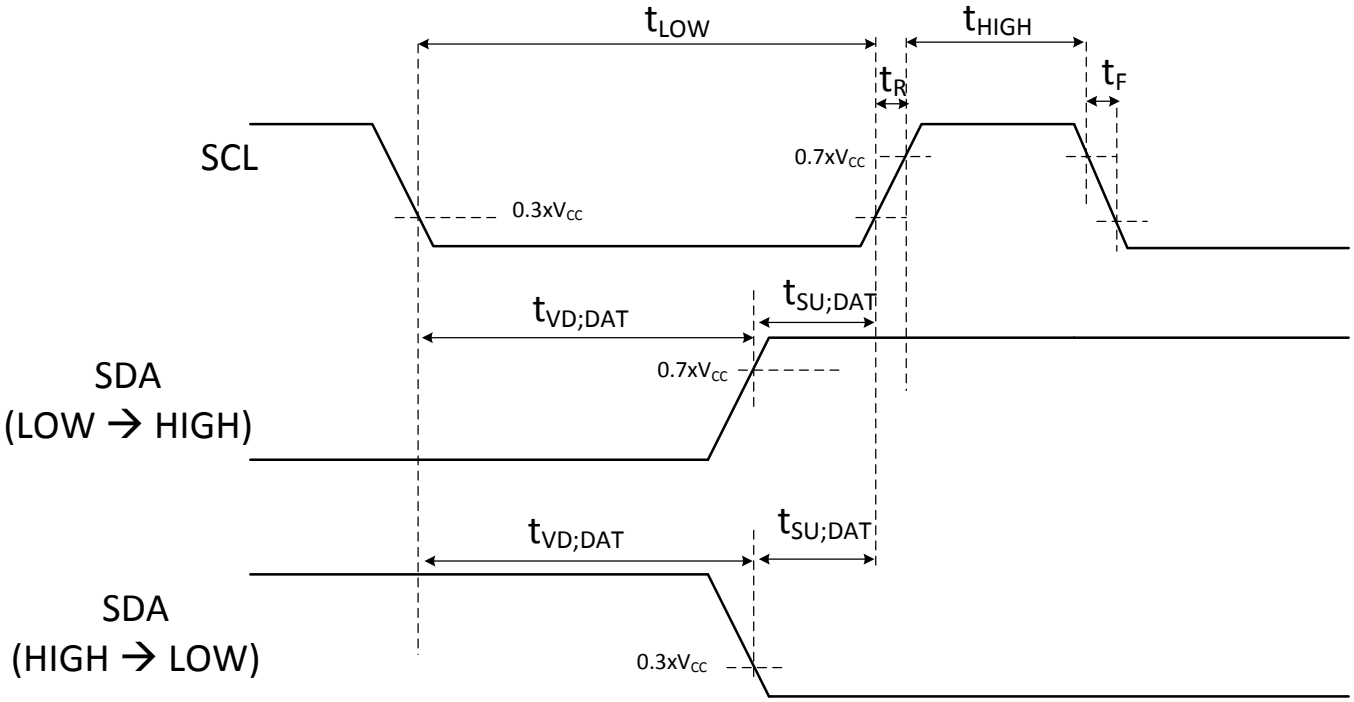

Figure 1. Timing Diagram for an I2C System With the Master Generating the SCL Clock Signal and a Slave Responding With Data on SDA

The maximum clock frequency for this case can be calculated as:

$$f_{SCL}(\max) = \frac{1}{t_{LOW} + t_{HIGH} + t_R + t_F} \quad (1)$$

Where,

t_{LOW} = low period of the clock

t_{HIGH} = high period of the clock

t_R = rise time of the clock

t_F = fall time of the clock

The timing parameters in Equation 1 and the f_{SCL} (max) calculation result based on these timing parameters for a system based on I2C FM and FM+ spec is shown in Table 1. As expected, the f_{SCL} (max) for FM spec is 400 kHz and for FM+ spec is 1000 kHz, as also mentioned in the I2C spec.

Table 1. f_{SCL} (max) Calculation for I2C Systems Based on FM or FM+ Masters and Slaves

Parameter	Based on I2C FM Spec Limits	Based on I2C FM+ Spec Limits
LOW period of SCL clock (t_{LOW} (min))	1300 ns	500 ns
HIGH period of SCL clock (t_{HIGH} (min))	600 ns	260 ns
Rise time of both SDA and SCL signals (t_R (max))	300 ns	120 ns
Fall time of both SDA and SCL signals (t_F (max))	300 ns	120 ns
Maximum clock frequency (f_{SCL} (max))	**400 kHz**	**1000 kHz**

From the timing diagram in Figure 1, t_{LOW} (min) must be greater than $t_{VD;DAT}$ (max) plus $t_{SU;DAT}$ to satisfy the data valid and setup time requirement.

$$t_{LOW}(min) > t_{VD;DAT} + t_{SU;DAT} \quad (2)$$

Based on numbers in Table 2, the FM spec has enough timing margin to satisfy Equation 2, however, there is no timing margin in FM+ spec to satisfy Equation 2. This can cause challenges when a repeater that adds propagation delays is used on the I2C FM+ bus.

Table 2. Relationship Between t_{LOW} (min), $t_{VD;DAT}$ and $t_{SU;DAT}$

Parameter	Based on FM Spec Limits	Based on FM+ Spec Limits
LOW period of SCL clock (t_{LOW} (min))	1300 ns	500 ns
Data valid time ($t_{VD;DAT}$ (max))	900 ns	450 ns
Data valid time ($t_{SU;DAT}$ (min))	100 ns	50 ns
Timing margin (= t_{LOW} (min) - $t_{VD;DAT}$ (max) - $t_{SU;DAT}$ (min))	**300 ns**	**0 ns**

3 I2C Bus With a Repeater

Consider an I2C bus system where a repeater is used to isolate the capacitance between the master and slave side similar to Figure 2.

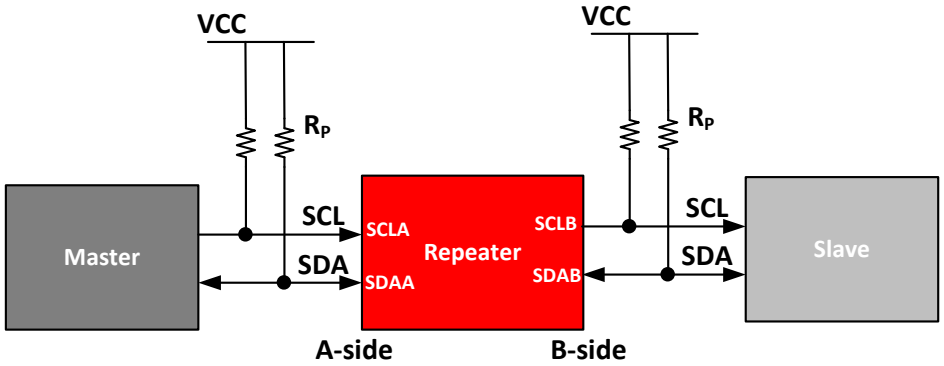

Figure 2. Generic I2C Bus System Showing a Bus Master, Repeater, and a Slave

The worst-case timing delay is seen for the case when the slave is sending the data to the master as in this case the data valid time ($t_{VD;DAT}$) and setup time ($t_{SU;DAT}$) has to be met with the repeater propagation delayed SCL (Figure 3). The master generates the I2C clock signal (SCL) on the A-side of the repeater. This SCL is passed through the repeater and appears at the B-side with the repeater propagation delay added ($t_{PHL;AB}$). The data on the B-side (SDA) must be valid within the data valid time ($t_{VD;DAT}$) as per the I2C spec (note that the $t_{VD;DAT}$ is referenced to the delayed SCL on B-side). After the data becomes valid, it

passes through the repeater from B-side to A-side and a propagation delay ($t_{PHL;BA}$) is added. For simplicity, we have assumed that the rise/fall time on the A- and B-side of the repeater are the same, however, in practice they can differ. The data on the A-side must be available at setup time ($t_{SU;DAT}$) before the rising edge of SCL. For the LOW to HIGH transition on SDA, adding all of the mentioned time corresponds to the LOW period of the SCL as:

$$t_{LOW-LH} = t_{PHL;AB} + t_{VD;DAT} + t_{PLH;BA} + t_{SU;DAT} \quad (3)$$

For the HIGH to LOW transition on SDA adding the previously mentioned timings corresponds to the LOW period of the SCL as:

$$t_{LOW-HL} = t_{PHL;AB} + t_{VD;DAT} + t_{PHL;BA} + t_{SU;DAT} \quad (4)$$

The maximum clock (SCL) frequency that can be used on an I2C bus with a repeater can be calculated as:

$$f_{SCL}(\max) = \frac{1}{t_{LOW} + t_{HIGH} + t_R + t_F} \quad (5)$$

Assuming the HIGH-to-LOW transition on SDA results in greater timing delay compared to the LOW-to-HIGH transition:

$$f_{SCL}(\max) = \frac{1}{t_{LOW-HL} + t_{HIGH} + t_R + t_F} = \frac{1}{(t_{PHL;AB} + t_{VD;DAT} + t_{PHL;BA} + t_{SU;DAT}) + t_{HIGH} + t_R + t_F} \quad (6)$$

Table 3 shows the values for the timing parameters shown in Equation 6 and the calculation result for the f_{SCL} (max) based on I2C FM spec and for I2C FM spec with TCA9617B repeater rise/fall time specs. The calculation shows that it is possible to meet the 400 kHz I2C FM f_{SCL} (max) spec in both cases (f_{SCL} (max) is higher than 400 kHz in both cases).

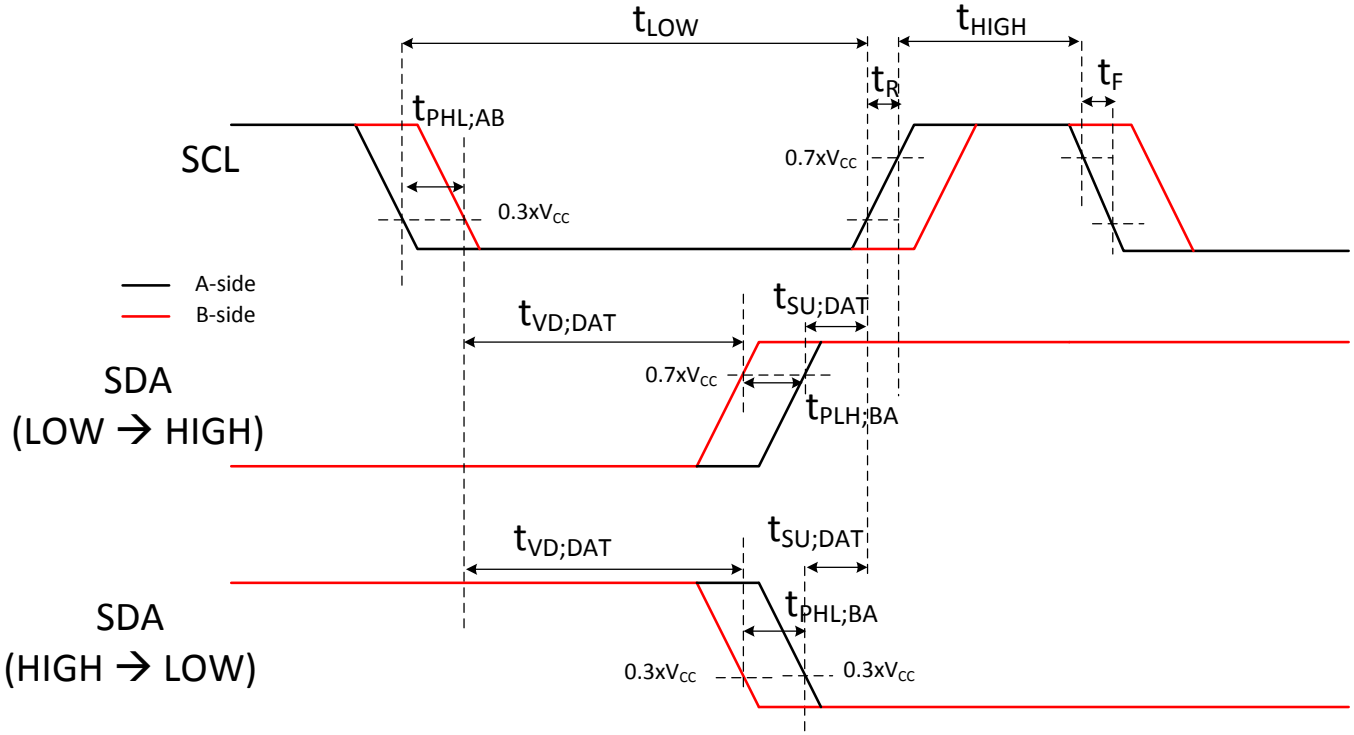

Figure 3. Timing Diagram for an I2C System With the Master Generating the SCL Clock Signal, an I2C Repeater Providing Capacitance Buffering (and Adding Propagation Delay), and a Slave Responding With Data on SDA

Table 3. Maximum Clock Frequency (f_{SCL} (max)) Calculation Based on I2C FM Specifications and for FM Specifications with TCA9617B Repeater Characteristics

Parameter	Based on I2C FM Spec With TCA9617B Propagation Delays	Based on I2C FM Spec With TCA9617B Propagation Delays and Rise/Fall Times
Data valid time ($t_{VD;DAT}$ (max)), from I2C FM spec	900 ns	900 ns
Data setup time ($t_{SU;DAT}$ (min)), from I2C FM spec	100 ns	100 ns
High period of SCL (t_{HIGH} (min)), from I2C FM spec	600 ns	600 ns
Repeater propagation delay from B to A defined as $0.3xV_{CC}$ on A and B side ($t_{PHL;BA}$), from repeater datasheet (TCA9617B)	140 ns	140 ns
Repeater propagation delay from A to B defined as $0.7xV_{CC}$ on A and B side ($t_{PHL;AB}$), from repeater datasheet (TCA9617B)	144 ns	144 ns
Fall time of SCL (t_F (max)), from I2C FM spec or repeater datasheet (TCA9617B)	300 ns	13.8 ns
Rise time of SCL (t_R (max)), from I2C FM spec or repeater datasheet (TCA9617B)	300 ns	88 ns
Maximum clock frequency (f_{SCL} (max))	**402.6 kHz**	**503.6 kHz**

Table 4 shows the values for the timing parameters shown in Equation 6 and the calculation result for the f_{SCL} (max) based on I2C FM+ spec and for I2C FM+ spec with TCA9617B repeater rise/fall time specs. These calculation results show that with the TCA9617B repeater it may not be possible to meet the 1000 kHz I2C FM+ f_{SCL} (max) spec under all loading conditions (f_{SCL} (max) is lower than 1000 kHz in both cases). For smaller loading conditions than those specified in TCA9617B datasheet the repeater propagation delays and rise/fall times are smaller, hence, higher f_{SCL} (max) than those mentioned in Table 4 can be achieved. However, because of no timing margin on the I2C FM+ spec it still is not possible to meet the 1000 kHz f_{SCL} (max) spec.

Table 4. Maximum Clock Frequency (f_{SCL} (max)) Calculation Based on I2C FM+ Specifications and for FM+ Specifications With TCA9617B Repeater Characteristics

Parameter	Based on I2C FM+ Spec With TCA9617B Propagation Delays	Based on I2C FM+ Spec With TCA9617B Propagation Delays and Rise/Fall Times
Data valid time ($t_{VD;DAT}$ (max)), from I2C FM+ spec	450 ns	450 ns
Data setup time ($t_{SU;DAT}$ (min)), from I2C FM+ spec	50 ns	50 ns
High period of SCL (t_{HIGH} (min)), from I2C FM+ spec	260 ns	260 ns
Repeater propagation delay from B to A defined as $0.3xV_{CC}$ on A and B side ($t_{PHL;BA}$), from repeater datasheet (TCA9617B)	140 ns	140 ns
Repeater propagation delay from A to B defined as $0.7xV_{CC}$ on A and B side ($t_{PHL;AB}$), from repeater datasheet (TCA9617B)	144 ns	144 ns
Fall time of SCL (t_F (max)), from I2C FM+ spec or repeater datasheet (TCA9617B)	120 ns	13.8 ns
Rise time of SCL (t_R (max)), from I2C FM+ spec or repeater datasheet (TCA9617B)	120 ns	88 ns
Maximum clock frequency (f_{SCL} (max))	**778.8 kHz**	**872.8 kHz**

If an experiment is carried out in the lab to measure the maximum frequency on SCL when using a repeater, it may be possible to clock the signals at a faster rate than what the calculations in Table 4 show. However, the system designer should take these calculations into consideration as all the slaves on the I2C bus may not be able to support that high frequency over all possible temperature / voltage corners conditions, hence, leading to yield fallout. The system designer has the flexibility to reduce the loading conditions and achieve the highest clock frequency possible.

4 Summary

In this application report we showed a method of calculating the maximum clock frequency of an I2C bus using a repeater. It is shown that the I2C FM spec has timing margin for repeater propagation delays; however, the FM+ spec does not have timing margin for the repeater propagation delay. The 1000-kHz operation of FM+ I2C bus when using repeaters is limited to certain loading conditions on the I2C bus.

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