Application Report
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I²C Solutions for Hot Swap Applications

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ABSTRACT

This document discusses I²C hot insertion/hot swap into live backplanes, the potential problems users could face, and how some devices can add layers of safety for hot insertion applications.

1 What is an I²C "Hot Swap" device?

A device which is capable of hot insertion/hot swap means it can be plugged into a live backplane from an external PCB without the need to power down the backplane. This kind of feature is useful in applications where powering down a system may be undesirable or not possible such as in servers or wireless base stations. Hot insertion devices help to prevent glitches to the downstream devices while trying to minimize the effect of adding parasitic capacitance into a live bus.

2 Hot insertion concerns

Two potential concerns when a hot insertion event occurs on a live bus are false clock edge generation and a bad power on reset for the downstream I²C slave. A false clock edge could be created during insertion when SCL is a logic high due to the initial in rush current from the live backplane going to fill the parasitic capacitance of the external card. This presents a problem because the I²C slave on the bus may see the additional clock edge and it becomes out of sync with the master's actual clock pulses. In the worst case scenario, an I²C stuck bus occurs where the SDA line becomes stuck because the slave is waiting for the last clock pulse to release the SDA line. This can cause major problems in a system which relies on I²C to pass information before executing actions/diagnostics.

If the SCL signal on the backplane is at a logic low, the inrush current would not be a concern and a false clock edge would not be generated. Relying on this to occur each time a hot insertion event occurs is unlikely to happen and doomed to an eventual stuck bus event occurring.

The second concern for a bad power on reset is derived from the power supply ramp up requirements of the downstream I²C device and any parasitic capacitance or inductance on the power trace between the backplane and the I²C device on the external card. I²C devices typically require the V_{CC} ramp rate to be within a certain minimum or maximum to power up correctly. Being outside of that range due to a hot insertion event (parasitic inductance causing ringing on the V_{CC} ramp) could result in the downstream I²C device state machine powering up in an unknown state. If this occurs, the downstream I²C device may power up thinking it is in a read transaction and end up holding the SDA line low or even in a clock stretching event and lock up the SCL line.

3 Discrete hot-insertion implementation on the backplane

A discrete approach to preventing a glitch from occurring during the hot insertion event can be implemented using an I²C switch or I²C buffer with an enable pin. This can be accomplished by designing the I²C switch or buffer to sit on the edge of the backplane. For the I²C switch, a presence detect signal should be placed on the external card and feed into the backplane interrupt detection system. This tells the processor when an external card has been connected to the backplane and can extract data from the downstream I²C slave. Figure 1 shows an example of this being implemented with the presence detection signal feeding into a TCA9555 input. This set up allows for multiple cards to be inserted by using the spare channels on the TCA954x (I²C switch) and TCA9555 (I²C I/O Expander) for the interrupt detection. The TCA9555 is not necessary though if the processor has unused GPIOs available.

In this system, when the external card is inserted, the backplane provides power and a common ground connection to the I²C slave. The backplane I²C pull up resistors on the secondary channel of the I²C switch pulls the slave SDA/SCL pins high. The TCA9555 has its GPI logic changed from a digital HIGH (an internal 100k pullup) to a digital LOW from the GND connection when the external card is connected. This generates the interrupt and signals the processor to check to see which input generated the interrupt and then enable the I²C switch channel that the external card to which it is connected.

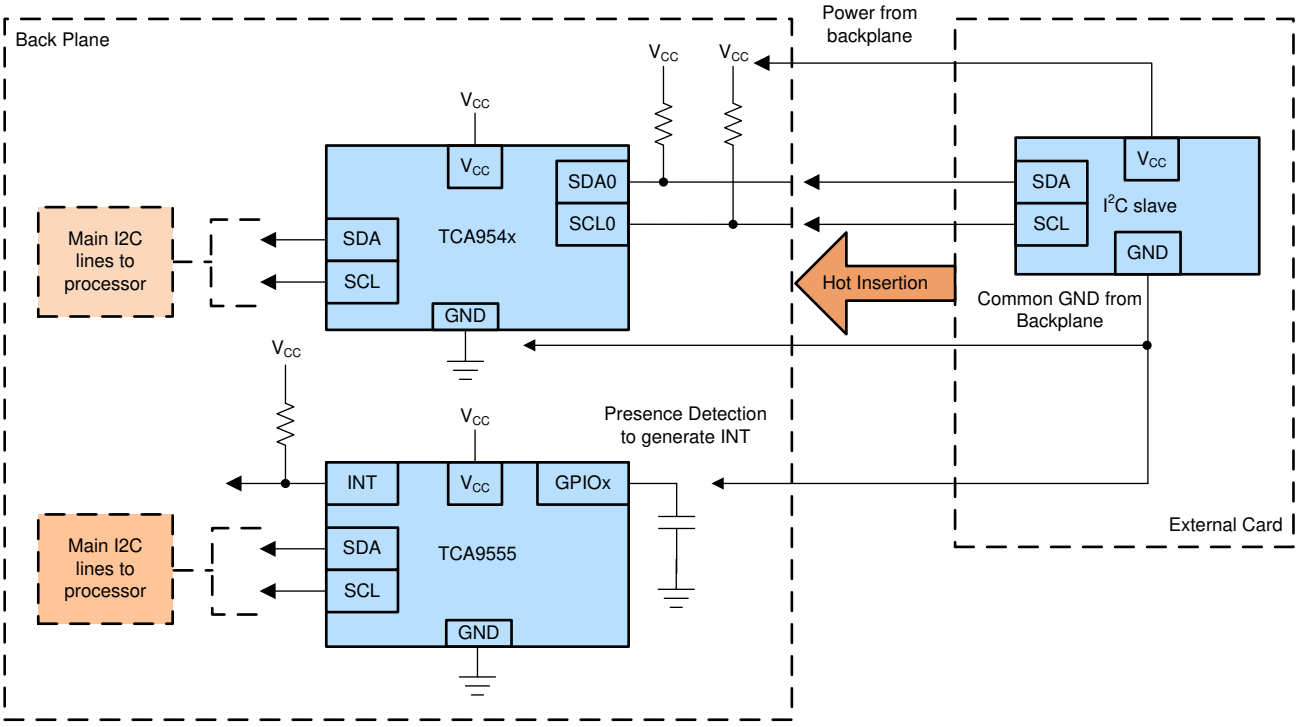

Figure 1. Descrete hot insertion support on a back plane

Additional notes:

- The external card should connect GND and then power before SDA/SCL:
  - This helps prevent any potential back biasing through the SDA/SCL lines if they connect first.
  - Requires a female to male connector which staggers the signals to connect at different times.
- This approach helps to prevent glitches on the main bus but does not protect the I²C slave from a bad POR.
  - In the worst case scenario, the processor connects the I²C slave to the main bus while it holding the SCL/SDA line low..
  - An I²C switch with a reset can be used to disable all I²C channels to regain I²C control. This does require the processor to be programmed to detect the stuck bus and toggle the reset if this occurs.
- The switch in Figure 1 can be replaced with an I²C level shifter or I²C buffer with an enable pin.
- TCA9555 can be replaced with any I²C GPIO expander with an interrupt feature.

4 Designing the External Card for hot insertion

The approach mentioned previously may not be possible if the system designer does not have control over the design of the backplane but instead has control of the external card. In this case, using a hot-insertion buffer on the external card would be an ideal approach. The TCA9511A is a potential device to fit this application. This devices features a 1-V pre-charge circuit, slew rate triggered rise time accelerators, and stop/idle condition detection for 'smart' connection.

The 1-V pre-charge feature helps to limit the inrush current when the external card SDA/SCL connection is made with the backplane. While not foolproof, the 1-V pre-charge can help to mitigate glitches during the hot insertion event into a live bus. In order for the 1-V pre-charge feature to be used during the hot insertion event, two design considerations must be ensured.

The first design set up that needs to be done is the 'IN-side' of the TCA9511A needs to be designed to make connection with the backplane from the external card. This is because the 'IN-side' of the device does its bus idle/stop condition detection only on the 'IN-side' of the device while the 'OUT-side' only looks to see if the voltage is above V_{IH} (Voltage input High). For this reason, pull up resistors should not be populated on the 'IN-side' of the external card's I^2C bus as it would generate a false idle condition to the TCA9511A and also turn off the 1-V pre-charge circuit. Figure 2 points out which side is the 'IN-side' of the TCA9511A and non-populated pullup resistors on the 'IN-side'.

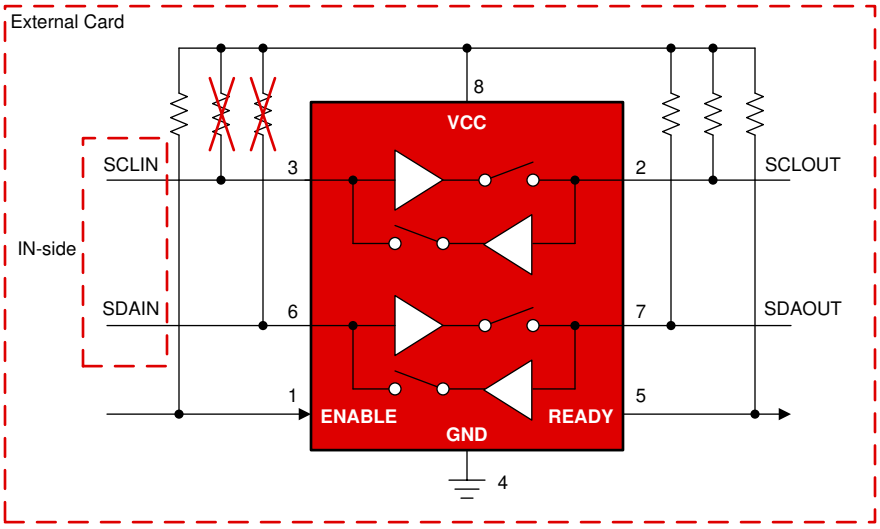

Figure 2. Example of external card design without pull up resistors on TCA9511A IN-side

The second design set up required is the connection from the external card to the backplane must connect the ground and power to the external card first before the SDAIN/SCLIN connects to the backplane I^2C bus. The reason for this is the TCA9511A needs to power up and turn on its 1-V pre-charge circuit before the SCLIN/SDAIN connects to the backplane. If the SDAIN or SCLIN lines connect to the backplane at the same time as the power and ground, then the 1-V pre-charge circuit do not power up in time and the backplane I^2C bus may dip down towards ground momentarily if the SDA/SCL lines on the backplane are HIGH or transitioning HIGH. This means the external card needs to have staggered connection points on its male connector. An example of a staggered male connector is shown in Figure 3. In this example, the GND connects first. V_{CC} is next which is done by making the exposed copper trace for V_{CC} about 25 mils shorter than GND. Afterwards, SDAIN or SCLIN connects to the backplane because their exposed traces are 50 mils shorter than GND and 25 mils shorter than V_{CC}.

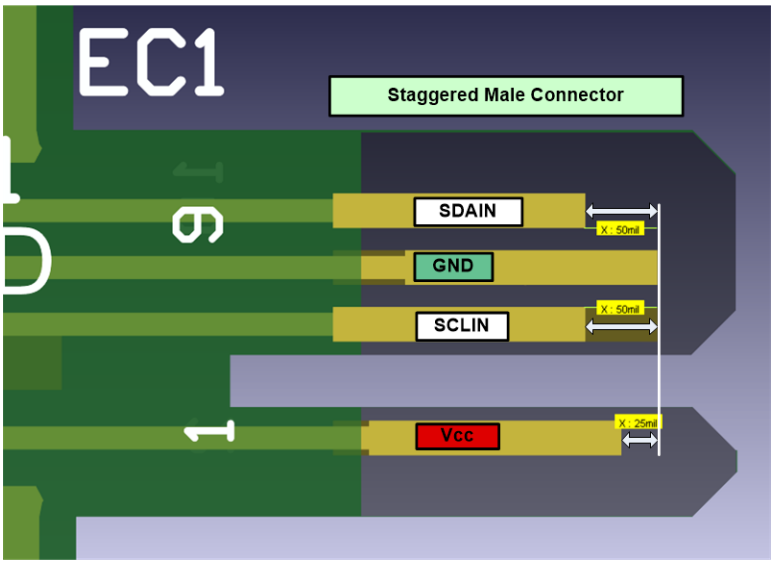

Figure 3. Example of staggering male connector to support hot insertion on external card

Once the connection between the external card and the backplane is made, the TCA9511A checks three conditions:

1. Is the enable pin high?
2. Are the SCLOUT or SDAOUT pins high?
3. Has a stop condition or bus idle been detected on SCLIN or SDAIN?

If all three conditions are met, then the TCA9511A connects the ‘IN-side’ and the ‘OUT-side’ together and the READY pin of the device goes HIGH to signal this.

Condition:

1. Allows the processor to have control over whether or not it wants to connect the downstream slaves on the external card.
2. Check to ensure that the downstream slaves on the external card have powered up correctly, and do not cause a stuck bus. In some cases, the V_{CC} ramp up on the external card may be not be within the slave’s datasheet power up specifications when the hot insertion occurs. In these instances, if the slave powers up and gets the I^2C bus stuck on the ‘OUT-side’, then the main I^2C bus on the backplane does not also become stuck.
3. Make sure that the connection between the ‘IN-side’ and ‘OUT-side’ are not made until the communication on the backplane has stopped. If the two sides connected during communication, the slaves on the ‘OUT-side’ of the external card may see a false I^2C start condition and glitch the state machines of the I^2C slaves.

These three conditions are what make the TCA9511A suitable devices for hot insertion applications.

5 Rise time accelerator

An additional advantage that the TCA9511A provides is the rise time accelerator (RTA) circuit on both sides of the device. This is advantageous because in applications where the capacitive loading of the system upstream from the external card is unknown, the rise time accelerators help to keep the rise time of the bus within I^2C specification when plugged into a heavily loaded system. For reference, version 2.6 of the I^2C specification requires the rise time to be less than 1000 ns for standard mode (100 kHz) and less than 300 ns for fast mode (400 kHz). Rise time is defined as the time for a signal to go from 30% of V_{CC} to 70% of V_{CC}.

Figure 4 shows the rise time of a 360 pF load with an external pull up resistor of 10 kΩ in at V_{CC} of 5 V. The rise time in this system without the TCA9511A rise time accelerator is 3307 ns which is above the required 1000 ns and 300 ns for both standard mode and fast mode. Note that the time scale in Figure 4 is 800 ns per division.

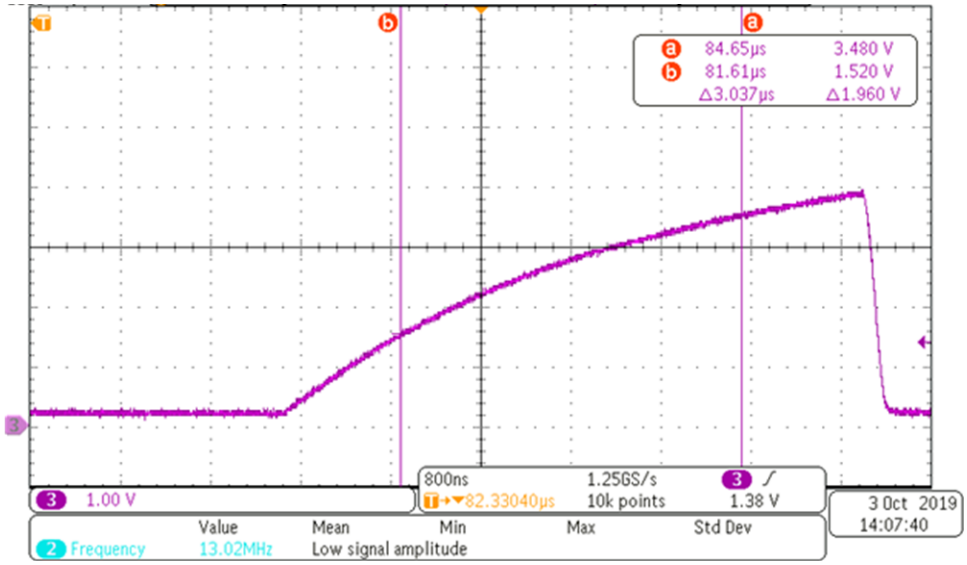

Figure 4. 360 pF loading with an external 10 kΩ pull up and rise time accelerator disabled

Figure 5 shows the same bus loading conditions of 360 pF and a 10 kΩ pull up resistor at 5 V V_{CC} but this time the TCA9511A is enabled and its rise time accelerator is engaged. The rise time in this case is 214.7 ns which now meets the specification for both standard mode and fast mode. The two slew rates in the figure are due to the original RC constant and then by the rise time accelerators pull up. The rise time accelerator for the TCA9511A trigger when two conditions are met on both sides of the device:

1. The rising signal is above 0.6 V.
2. The slew rate of the rising signal is faster than 1.25 V/µs.

Note that the time scale in Figure 5 is 200 ns per division versus 800 ns per division in Figure 4.

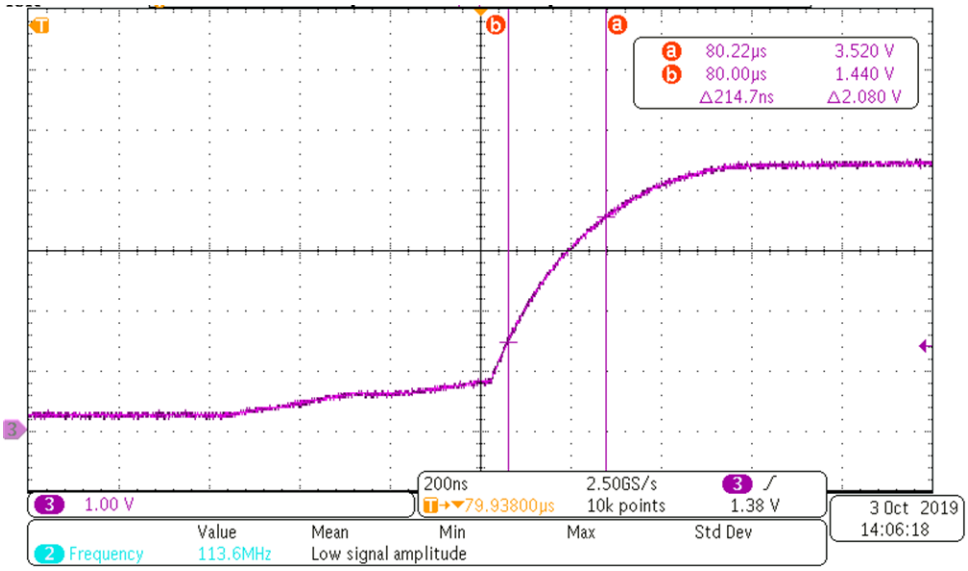

Figure 5. 360 pF loading with an external 10 kΩ pull up with rise time accelerator enabled

6 Conclusion

In systems where hot insertion is required, either the backplane or the external card must be properly designed in order to minimize the effects of hot insertion. Devices like an I^2C switch on the backplane or an I^2C hot insertion buffer on the external card are appropriate devices for such applications. Poor hot insertion designs may result in a stuck bus and preventing key diagnostic information from being extracted to the processor through the I^2C bus.

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