Application Report
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DSS BT656 Workaround for TDA2x

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ABSTRACT

The display subsystem (DSS) in TDA2x has a silicon limitation (Errata) to support the standard BT656 output. This application report explains the limitation and how the DSS can be configured to interface with video encoders such as ADV7393, which supports discrete sync digital video input and convert to NTSC/PAL analog SD video output.

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1 DSS BT656 Limitation in TDA2x

When BT.656 or BT.1120 modes are used on DSS outputs (vout1,2,3), the configuration of the horizontal blanking timing is limited to a value of 256 clocks or less due to the HSW bit field being limited to 8-bit (256 max value) programmed in the `DISPC_TIMING_H1.HSW` register. This register should be programmed in number of clocks and not in number of pixels.

The BT.656 standard requires 280 or 268 bytes to support PAL and NTSC timings, respectively. BT.1120 requires 280, 720, and 830 depending on format. For reference, standard timing for PAL is shown in Figure 1. The DSS cannot support devices requiring such blanking duration due to this limitation. For details of this limitation, see the *TDA2x ADAS Applications Processor Errata* (SPRZ397).

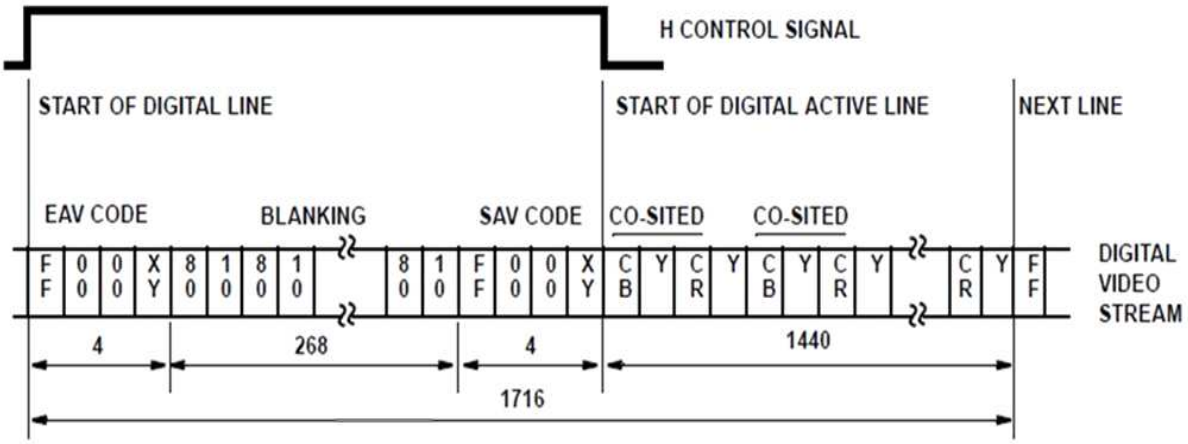


Figure 1. BT656 8-bit Parallel Interface Data Format

When DSS is configured for BT656 mode, the receiver should be able to receive the custom BT656 timings with reduced horizontal blanking. This results in either increase in the frame rate with standard pixel clock or decrease in the pixel clock with the standard frame rate. This may not be supported by most of the video encoders available in the market. This application report discusses other options that can be used to get standard NTSC/PAL output.

2 SD Video Output Using External Encoder

To get standard NTSC/PAL video output using external video encoder, the following two approaches can be used depending on the video encoder feature. This is explained in detailed in the subsequent sections.

- Interfacing with the video encoder that supports 16-bit RGB565 discrete sync input
- Interfacing with the video encoder that supports 16-bit YUV422 discrete sync input

2.1 Interfacing With 16-Bit RGB565 Discrete Sync Video Encoder

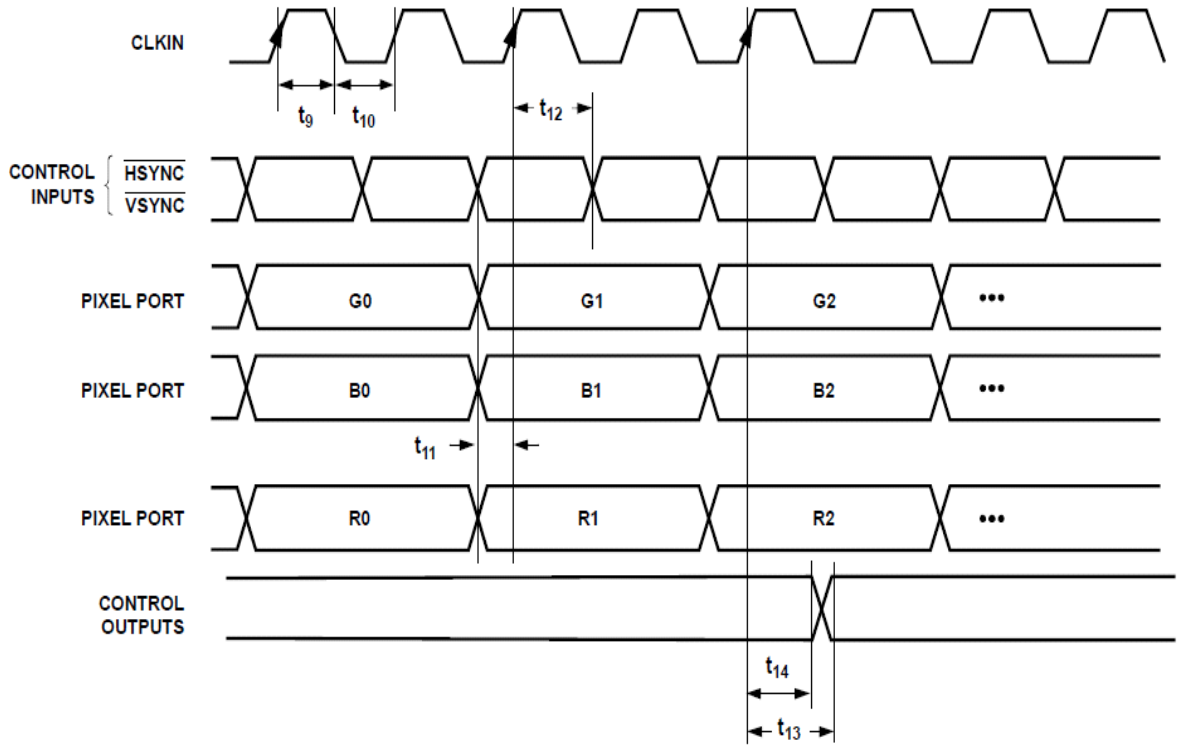
ADV7393 video encoder is taken as an example for the discussion in this section that supports RGB565 discrete sync input.

2.1.1 ADV7393 Video Encoder Overview

ADV7393 is high-speed digital-to-analog video encoders providing composite, S-Video or component analog outputs in SD or HD video formats. ADV7393 has a 16-bit (P0 to P15) digital video data input and video control signal (HSync/VSync) inputs.

In 16-bit input mode, the encoder can support 4:4:4 RGB format. In this mode, Red pixel data is input on P4 to P0, Green pixel data is input on P10 to P5 and Blue pixel data is input on P15 to P11. The input pixel clock expected is 27 MHz, but the pixel data is updated at half the rate of the clock at 13.5 MHz.

Figure 2 shows the timing diagram for this mode.



t9 = clock high time
t10 = clock low time
t11 = data setup time
t12 = data hold time
t13 = control output access time
t14 = control output hold time

Figure 2. SD Input, 16-Bit 4:4:4 RGB (Input Mode 000)

2.1.2 Interfacing DSS With ADV7393 Video Encoder

To interface with the ADV7393 encoder, configure the DSS for the RGB565 format discrete sync output. The lower 16 data lines, pixel clock and video sync pins are connected between the DSS and encoder. Figure 3 shows the interfacing diagram.

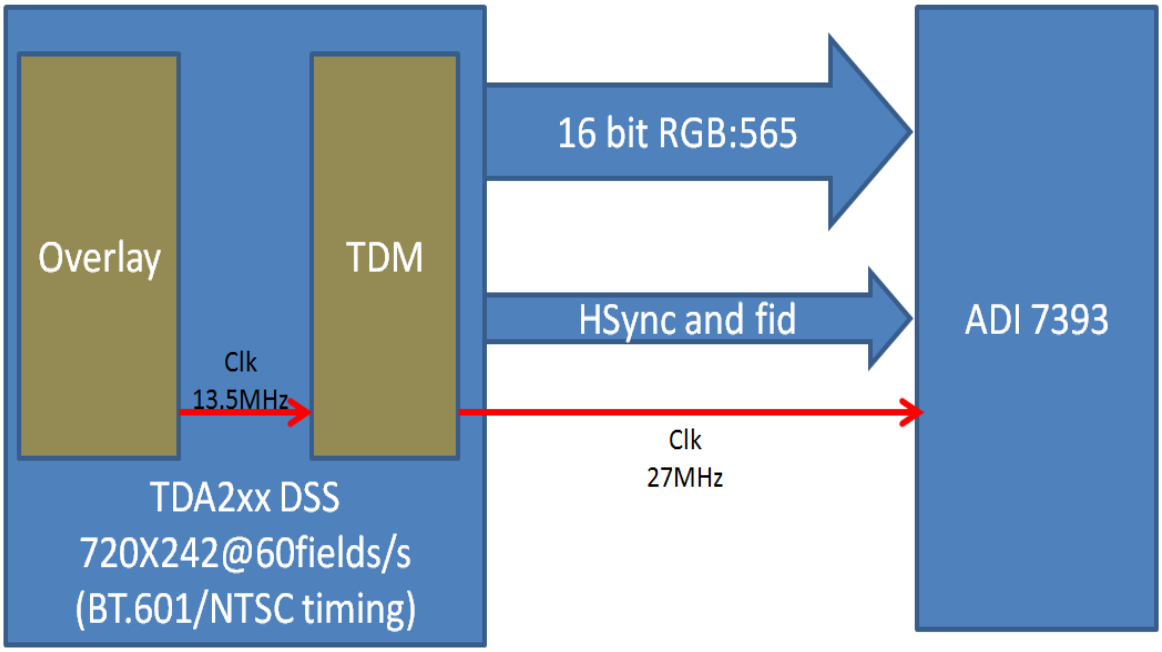


Figure 3. Interfacing DSS With ADV7393

The pixel clock for the 16-bit parallel data output for the NTSC/PAL resolution is 13.5 MHz at Display controller. The Encoder can work only at 27 MHz as there is no internal clock converter and as shown in Figure 2. In order to match the pixel clock, configure the DSS in TDM mode with pixel repetition. When this is enabled, the pixel clock from DSS doubles to 27 MHz. And the ADV7393 encoder can sample the data every other clock cycle.

If the encoder can work with 13.5 MHz pixel clock, then this TDM mode configuration can be disabled and a normal RGB656 discrete sync output can be used.

2.1.3 DSS Configuration

To comply with the timing requirements of the encoder as mentioned in Section 2.1.2, configure DSS using the settings below:

- Pixel clock of LCD is configured at 27 MHz.
- Output data format configured as RGB565
- TDM configuration to support 27 MHz clock
  - Enable TDM mode in DISPC with 2 cycles per pixel, 16-bit output interface, state of unused bits configured to Unchanged from previous state. First cycle outputs all the 16-bit data and the second cycle will have dummy data.
  - TDM configuration is not required in case video encoders support internal clock converters and support 13.5 MHz input clock. In this case, disable the TDM.

2.1.3.1 DSS Register Configuration

- Setting output data format to RGB565

```
DISPC_CONFIG1.COLORCONVENABLE = 0x0
DISPC_CONTROL1.TFTDATALINES = 0x1: 16-bit output aligned on the LSB of the pixel data interface
```

- TDM configuration (required only for getting 27 MHz output depending on the encoder)

```
DISPC_CONTROL1.TDMENABLE = 0x1: TDM enabled
DISPC_CONTROL1.TDMPARALLELMODE = 0x3: 16-bit parallel output selected
DISPC_CONTROL1.TDMCYCLEFORMAT = 0x1: 2 cycles for 1 pixel
DISPC_DATA1_CYCLE1 = 16
DISPC_DATA1_CYCLE2 = 0
DISPC_DATA1_CYCLE3 = 0
```

2.1.3.2 DSS Driver Programming

- Setting output data format to RGB565

  In IOCTL, `IOCTL_VPS_DCTRL_SET_VENC_OUTPUT`, pass the parameter `Vps_DctrlOutputInfo` by using the settings below to configure output to 16 bits discrete sync.

```
Vps_DctrlOutputInfo.videoIfWidth = FVID2_VIFW_16BIT;
Vps_DctrlOutputInfo.dvoFormat = VPS_DCTRL_DVOFMT_GENERIC_DISCSYNC;
```

- TDM configuration (required only for getting 27 MHz output depending on the encoder)

  In IOCTL, `IOCTL_VPS_DCTRL_DSS_SET_ADV_VENC_TDM_PARAMS`, pass the parameter `Vps_DssDispcAdvLcdTdmConfig` by using the settings below for enabling the TDM mode.

```
Vps_DssDispcAdvLcdTdmConfig with below setting for enabling the TDM mode.
Vps_DssDispcAdvLcdTdmConfig.tdmEnable = TRUE;
Vps_DssDispcAdvLcdTdmConfig.tdmCycleFormat = 0x1;
Vps_DssDispcAdvLcdTdmConfig.tdmParallelMode = 0x3;
Vps_DssDispcAdvLcdTdmConfig.noBitsPixel1Cycle1 = 16;
Vps_DssDispcAdvLcdTdmConfig.noBitsPixel2Cycle1 = 0;
Vps_DssDispcAdvLcdTdmConfig.noBitsPixel3Cycle1 =0
```

2.1.4 Interfacing DSS With the ADV7343 Encoder in Interlaced Mode

DSS outputs three sync signals for the discrete sync output, ie HSYNC, VSYNC and FID signals. For the interlaced display, VSYNC typically is expected to toggle at the start of the line for the even field display and for the odd field, it is expected to toggle in the middle of the line. DSS always outputs VSYNC aligned with the HSYNC, so it cannot generate VSYNC at the middle of the line.

Due to this issue, HSYNC and FID signal outputs from DSS are used to interface with the ADV7343 encoder.

ADV7343 encoder supports interlaced input using HSYNC and FID signals in the Mode-1 Slave operation. This mode has specific requirement that FID should toggle only when HSYNC is active. But DSS always generates FID toggle aligned to either rising or falling edge of the HSYNC. This FID toggle may not get detected by the ADV7343. This requires additional HW cirtuit to delay FID signal by few clock cycles in order to get it detected correctly by the ADV7343 encoder.

There are two D-flops suggested here to delay the FID signal: SN74LVC1G374A-Q1 and SN74LVC74A-Q1. Each of these D-flops can delay FID line by a clock cycle. These D-flops has sufficient setup and hold time to get FID signal detected in ADV7343 encoder.

Figure 4 shows an example of delay circuit to delay FID by two clock cycles using SN74LVC1G374A.

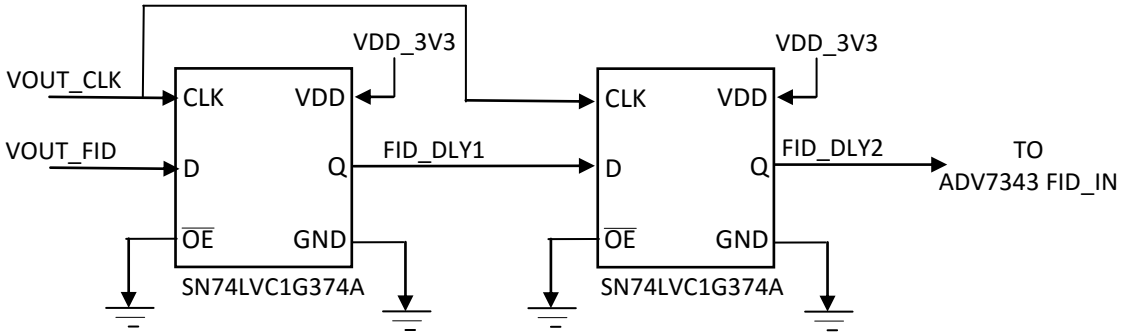


Figure 4. Sample FID Delay Circuit Using SN74LC1G374A FlipFlop

2.2 Interfacing With 16-Bit YUV422 Discrete Sync Video Encoder

If the video encoder supports only 16-bit YUV422 input then, the DSS directly does not support output in YUV422 format with 16-bit interface. Use the workaround below for this.

The input to the DSS should be YUV422 format with NTSC/PAL video size. DSS should be configured to bypass all the processing blocks inside and send the bit exact output on the 16 bit output interface. For more information, see the "*Bit matching with 16-bit output interface*" section in *DSS Bit Exact Output* . Enable the TDM module as mentioned in Section 2.1.3 if the video encoder expects the pixel clock to be 27 MHz.

3 References

- *Display Subsystem* chapter in the *TDA2x SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 2.0, 1.x Technical Reference Manual* (SPRUHK5)
- *TDA2Ex SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 1.0* (SPRZ428)
- *TDA2x ADAS Applications Processor Errata* (SPRZ397)
- *ADV7390/ADV7391/ADV7392/ADV7393 Low Power, Chip Scale, 10-Bit SD/HD Video Encoder Data Sheet* (http://www.analog.com/media/en/technical-documentation/data-sheets/ADV7390_7391_7392_7393.pdf)
- *DSS Bit Exact Output*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2016) to A Revision	Page
• Added new Section 2.1.4.	5

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