Application Report
SLLA452–April 2019

TDP158 Schematic Checklist

ABSTRACT

This schematic checklist provides a brief explanation of each TDP158 device pin and the recommended configuration of TDP158 device pins for default operation. The TDP158 device is an AC-Coupled HDMI signal to transition-minimized differential signal (TMDS) redriver supporting digital video interface (DVI) 1.0 and high-definition multimedia interface (HDMI) 1.4b and 2.0b output signals. The TDP158 supports four TMDS channels and Digital Display Control (DDC) interfaces. The TDP158 has the ability to be configured via pin strap or I2C. Use this information to check the connectivity for each TDP158 device on a system schematic.

This document is intended to aid design at the system level for general applications, but must not be the only resource used. In addition to this list, use the information in the *TDP158 6-Gbps AC-Coupled to TMDS™/HDMI™ Redriver Data Sheet*, *TDP158 RSB Evaluation Module User's Guide*, and associated documents to gain a full understanding of device functionality.

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Trademarks

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PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
Main Link Input Pins				
IN_D[0:2]p/n	1, 2, 4, 5, 6, 7	Main link differential input		100 nF AC coupled from sink connector/GPU to TDP158
IN_CLKp/n	9, 10	Main link clock differential input	100 nF AC coupled from sink connector/GPU to TDP158	

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
Main Link Output Pins				
OUT_D[0:2]p/n	24, 25, 26, 27, 29, 30	TMDS data differential output	Direct connection from TDP158 to source connector/sink	
OUT_CLKp/n	21, 22	TMDS clock differential output	Direct connection from TDP158 to source connector/sin	
Configuration and Miscellaneous Pins				
SDA_SRC	39	Source side TMDS bidirectional DDC data line	Snoop mode, tie it to GND.	
SCL_SRC	38	Source side TMDS bidirectional DDC clock line	Snoop mode, tie it to GND	
SDA_SNK	33	Sink side TMDS bidirectional DDC data line	SDA/SCL from the source is connected directly to the SDA/SCL sink. The TDP158 needs its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Sink application: 47 k pullups to 5 V Source application: 2 k pullups to 5 V	Consider adding an external I2C buffer for DDC capacitance isolation.
SCL_SNK	32	Sink side TMDS bidirectional DDC clock line	SDA/SCL from the source is connected directly to the SDA/SCL sink. The TDP158 needs its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Sink application: 47 k pullups to 5 V Source application: 2 k pullups to 5 V	Consider adding an external I2C buffer for DDC capacitance isolation.
HOT PLUG DETECT PINS				
HPD_SNK	28	Hot plug detect input from sink side	Connect to HPD output of the display or source connector. For snoop mode: Connect directly to GPU of the sink (check GPU supported voltage) directly connected HPD line HPD_SNK has internal 190 k pulldown. Consider adding an external switch to isolate potential leakage voltage from sink HPD when sink is off.	Consider adding an external switch to isolate potential leakage voltage from sink HPD when sink is off.
HPD_SRC	3	Hot plug detect output to source side	If HPD_SRC goes to the source connector, a level shifter from 3.3 V to 5 V is needed. If HPD_SRC goes to GPU, check the supported GPU voltages. If HPD snoop mode is implemented, leave HPD_SRC floated.	
CONTROL PINS				
OE	36	Enable/reset pin	Start with 0.2 µF, tune depending on the RC time constant delay (Tr) requirement in regard to power ramp up time.	See Table 1 for different timing values based on capacitance.
V_{sadj}	18	TMDS-compliant voltage swing control resistor	Start with 6.49 k resistor to ground, resistor value tuning depends on compliance result	
SCL_CTL/SWAP	13	I2C clock signal or lane swap control	For pin strap mode, 1 k Ω pullup/pulldown. SWAP = L, normal operation SWAP = H, lane swap Refer to Table 2 of the datasheet for lane swap mapping.	2 k pullups to 3.3 V or value required by I2C master in I2C mode
SDA_CTL/PRE	14	I2C data signal or transmitter pre-emphasis control.	For pin strap mode Pre = L, 0 dB pre-emphasis Pre = H, 3.5 dB pre-emphasis	2 k pullups to 3.3 V or value required by I2C master in I2C mode.
I2C_EN	8	I2C control mode	1 k pulldown for pin strap mode 1 k pullup for I2C mode	
A0/EQ1	17	I2C address bit 0 or receiver equalization control	For pin strap mode EQ1, refer to Table 3 of the datasheet for RX EQ programming and values	Set address bit 0 in I2C mode
A1/EQ2	23	I2C address bit 1 or receiver equalization control	For pin strap mode EQ1, refer to Table 3 of the datasheet for RX EQ programming and values	Set address bit 1 in I2C mode
SLEW	34	Transmitter slew control	For pin strap mode, 1 kΩ pullup/pulldown or NC SLEW = L: Slowest ~ 203 ps SLEW = NC (Default): Mid-range 1 ~ 180 ps SLEW = H: Fastest ~ 122 ps	Leave it floating when I2C_EN/PIN = high, control through I2C
TERM	16	Transmitter termination control	For pin strap mode, 1 kΩ pullup/pulldown or NC TERM = L, 150 Ω–300 Ω (HDMI1.4b) TERM = NC, no termination (HDMI1.4b) TERM = H, 75 Ω–150 Ω (HDMI2.0)	If the TMDS_CLOCK_RATIO_STATUS bit = 1, the TDP158 automatically switches in 75 Ω ~ 150 Ω termination.
NC	19	No connect	NC, optionally connect 0.1 µF to GND for noise reduction	
POWER PINS				
VCC	11, 37	3.3 V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
VDD	12, 20, 31, 40	1.1 V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
GND	15, 35	Ground	Connect to board ground	
Thermal Pad	41	Ground	Connect to board ground	

Table 1. Enable (OE) Pin Timing Based on Capacitance

RISE TIME (T_r) (ms)	CAPACITOR VALUE (µF)
25	0.1
50	0.2
100	0.4
200	0.8
500	2

2 References

- *TDP158 6-Gbps, AC-Coupled to TMDS™ or HDMI™ Level Shifter Redriver Datasheet*
- *TDP158 RSB Evaluation Module User's Guide*

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