TFPxxx FAQ

ABSTRACT

The purpose of this document is to answer frequently asked questions about Texas Instrument's TFPxxx devices.

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1   Frequently Asked Questions

1. Can you use the TFP401 and TFP410 as HDMI transmitters/receivers?
   a. Yes, but the HDMI stream cannot include audio.
2. Is it possible to de-skew the data inputs DK[3:1] with the TFP410? Does the de-skew also apply to HSYNC, VSYNC, and DE?
   a. Yes, de-skew is applied to all data inputs including DE, DK[3:1], HSYNC, and VSYNC.
3. What is the timing of HSYNC and VSYNC in relation to the data during active and inactive periods for the TFP410?
   a. When the DE generator is used, the active data location is determined by the counts from HSYNC and VSYNC as described in the "DE Generator" section of the datasheet and the register description.
   b. The TFP410 and TFP510 does not move the pixel data to the defined edge of DE; it simply selects between the sync and control inputs and the pixel data inputs for DVI encoding. Note that the total line pixel count is limited by the register sizes when using DE generator (see the errata for details).
4. Do you need to reset the TFP410 and TFP510 when using I2C mode?
   a. Yes, both devices require a reset. A reset signal held low during power up or a low-going pulse after power is stable works. If the power line experiences unusual transients, a low-going pulse is preferred.
5. Do you need I2C to operate the TFP410?
   a. No, the TFP410 can be configured manually by connecting pins high or low to select the desired mode. I2C simply provides more functionality, particularly in the use of the MSEN output.
6. Do you need I2C top operate the TFP510?
   a. Yes, to make use of the HDCP features of the TFP510, I2C is required. If manually configured, the TFP510 outputs DVI, but HDCP functionality is not available.
7. What is the part number for TI's 48-bit input transmitter?
   a. TI currently does not offer a 48-bit input DVI transmitter.
8. How do you implement a dual link transmitter with the TFP410?
   a. The TFP410 was not intended to be used for a dual link transmitter and has no features to implement such a transmitter.

9. Where is the pipeline delay in the TI receiver?

    a. The pipeline delay of a DVI receiver is defined by the DVI specification as 64 pixels maximum. This parameter is not typically shown in receiver data sheets. The TI receivers select a pipeline delay based on the de-skew calculations each time the DVI signal is acquired. This may vary from connection to connection with the same setup.

10. How do you implement a dual link receiver using the TFP401?

    a. The TFP401 was not designed to function as part of a dual link receiver. With dual link DVI, only one clock is transmitted with the six data channels. A single link receiver de-skews the three data channels it receives and output these with the ODCK signal to clock the output data into a register in the next device. To use two single link receivers for dual link, the DVI clock must be distributed to both receivers. The outputs of the two receivers must be recovered using their appropriate ODCK (with any skew between the receivers removed), and converted to a single clock domain.

11. How do you turn on HDCP functionality of the TFP501?

    a. The HDCP functionality of the TFP501 is always available. Decryption is signaled to the HDCP receiver by the CTL3 signal encoded in the DVI signal. This encoding is accomplished by the transmitter and does not require intervention by the receiver. For proper HDCP operation, the TFP501 must have appropriate keys loaded in an external EEPROM and encrypted by the device.

12. Does the TFP501 operate with a non-HDCP transmitter?

    a. Yes, the TFP501 behaves like a standard DVI receiver unless the CTL3 signal is asserted by the transmitter. CTL3 is reserved in DVI and is not asserted by a properly designed DVI only transmitter.

13. Does the TFP510 operate with a non-HDCP receiver?

    a. Yes, if the transmitter system does not turn on encryption.

14. How does the transmitter know the receiver is HDCP capable?

    a. The transmitter can read the BKSV from the receiver address over the DDC lines. A non-HDCP transmitter has no need to read this value. A HDCP transmitter must read this value to determine if the KSV is valid and check if it is revoked. To determine whether the key sets are compatible, authentication must be accomplished.

15. Does HDCP test keys operate with production keys?

    a. No. To operate HDCP with an identifiable image transfer between the transmitter and receiver, the key sets must be compatible. The test keys and production keys do not interoperate.

16. Do you need a different HDCP device for the test keys?

    a. No. The TI HDCP devices use keys stored in external EEPROM. Only the EEPROM contents need to be changed when changing from test to production keys. This can be accomplished in-circuit with various board design methods.

17. Should you write protect the HDCP key EEPROM?

    a. Yes. The TI device reads from the EEPROM, checks an indicator value, and then decides whether to read and use the keys stored there or encrypt them. There is only one 64 bit value of the indicator which causes the device to re-write the EEPROM. Improper writes to the EEPROM by the device is unlikely, however, the EEPROM can possibly interpret power transients as a write command and alter its memory. Write protecting the EEPROM is advised after the TI device has encrypted the keys.

18. Do you need an EEPROM for HDCP keys with the TFP510?

    a. The TFP510 has a provision to use keys stored elsewhere in memory and sent to it. The keys are still encrypted uniquely to the device. See related documents for more details.

19. Do you need an EEPROM for HDCP keys with the TFP501?

    a. Yes, the TFP501 has no other user interface over which keys can be transferred.

20. How does the TI device differentiate between the key EEPROM and other I2C EEPROMs in the system?

    a. The TI devices use an isolated I2C bus for the EEPROM load. The device is always bus master, but talks to the EEPROM only at a well defined time after reset, so access to the EEPROM for factory programming or re-programming is easy.

21. Can you use the extra space or use a larger EEPROM and store other system data in the key EEPROM?

   a. There is no path in the devices to go from the key EEPROM to an external user interface. Any bus sharing or switching has to be implemented in a manner not to damage the HDCP key exchange.

22. Do TI offer a DVI buffer?

   a. There are DVI repeaters like the DS16EV5110A available.

23. Can you operate HDCP through a buffer made up of a receiver and transmitter?

   a. While this works well in concept, the TFP403 and TFP410 are both aware of HDCP and do not provide external access to CTL3. A buffer made with either of these devices is not able to pass the CTL3 signal and does not operate HDCP properly. The TFP401 does provide CTL3 and can be used with another transmitter to provide a buffer function.

24. Can the TFP501 be used in a HDCP repeater application?

   a. No, the 501 is designed to be a HDCP receiver only. It does not provide the necessary data structures for a HDCP repeater.

25. Can the TFP510 be used to talk to HDCP repeaters?

   a. Yes, with limitations. HDCP requires confidentiality of many values. One of the values required for authentication of the repeater needs to be sent on the I2C bus, which would violate its confidentiality. When used in a repeater capable transmitter, the transmitter must securely calculate this value independent of the TFP510.

26. The received data LSB appears to be inverted from what I sent in the transmitter. What is wrong?

   a. Check to see if the DVI pairs have been swapped. This is one reported phenomena of this problem.

27. Can the TFP401 be used to determine compliance of the DVI transmitter?

   a. The TI receivers do not provide the test standard bandwidth required for determining transmitter compliance with the DVI standard. They were designed to provide good performance with a compliant transmitter, not to be a test standard. Use a proper reference PLL for compliance testing of a DVI transmitter.

28. The eye pattern across the DVI receiver looks poor, but the image still looks good. Why?

   a. ODCK is a digital signal generated to latch the data from the output of the receiver. It is subject to influence of the internal operation of the receiver as well as the outputs. The eye pattern across a receiver varies depending on the device, operating mode, and data sent. The proper test for a DVI receiver is not the in-circuit eye, but bit error rate when provided with a DVI compliant eye determined by a test standard. Note that the TPA board provided by DDWG does not use ODCK to generate the eye and does not route data channels to the receiver device.

29. Do you need to connect the PowerPAD of the TI device to ground?

   a. The device functions without the power pad grounded, and in most applications, connection to a thermal plane is not required for power dissipation. However, it is recommended that the power pad be grounded. Refer to SLMA002H for details on the PowerPAD technology and installation.

30. What is the difference between the TFP401 and TFP401A?

   a. The TFP401A includes HSYNC regeneration circuitry. This was required to be interoperable with the Sil154 that exhibited HSYNC jitter. However, the Sil154 is no longer on the market so most customers are now buying the TFP401.

31. Does the DVI connector cause an impedance mismatch? What can be done to minimize this?

   a. Yes, the DVI connectors deviate from the DVI impedance. Allowances for the connector are made in the DVI specification. Different techniques help reduce reflections caused by the connector. The plane clearance cutouts at the DVI connector must be large enough to minimize capacitance from the through holes while still providing a good ground path through the pin array. Trace length between the transmitter and DVI connector may impact where a reflection and re-reflection from the transmitter shows up in the signal. Shorter traces may be better. Good impedance control on the traces is important of course, and stubs on the traces must also be avoided.

32. Can terminations be used on the DVI transmitter to minimize reflections?

   a. Parallel termination of the DVI line at the transmitter either through termination of each line to the transmitter power supply or between the differential pair reduces reflections in the system by

absorbing whatever reflects back to the transmitter. This often improves system performance but reduces signal swing and may cause the transmitter to be non-compliant to DVI 1.0, even if the signal swing is adjusted.

b. If the termination is to the transmitter supply voltage, the termination resistors at the transmitter end provide a current path through the DVI connection and DVI terminations in the receiver to the receiver power supply. This may prevent the DVI receiver from powering off. If 50-Ω resistors are used, the resistance between the transmitter and receiver supplies is approximately 12.5 Ω. The DVI specification requires both the transmitter off state voltage (VOFF) and the high-level output voltage (VH) to be AVcc +/-10 mV. AVcc is the termination voltage at the receiver. If the voltage between the receiver and transmitter differs by more than 20 mV nominal, the terminated transmitter is non-compliant to the specifications.

c. Termination between the pairs eliminates the possibility of the transmitter powering the receiver. VOFF may not be an issue, however, the termination causes current to be drawn from both lines of the DVI pair when either side drives the line. This shifts the common-mode operating point of the differential pair and the VHspec may not be met.

d. Series termination do not alter VOFFor VH, but may not provide much benefit. The DVIdriver is a current sink, so it has a high impedance in the off state. The series resistor reduces swing voltage and can reduce the edge speed on the signal. The series resistance adds to the high impedance when the driver is in the off state and does not likely reducere flections from the transmitter IC. If the series resistor is effective in reducing the edge speed, this can reduce the reflections from the connector coming back to the transmitter.

33. When you turn off the DVI display system, it does not power off, or does not act properly when you turn it back on. What are the likely causes?

a. A probable cause is installation of termination resistors on the DVI lines in the DVI source (transmitter) product. This allows connection of the transmitter and receiver power supplies with a parallel combination of the series of the termination resistors. A common result is 12.5 Ω (8 sets of 100 Ω in parallel). See the termination question above.

34. When you turn off the DVI source (transmitter), it does not power off or does not act properly when you turn it on again. What is the likely cause?

a. It is possible that the design of the transmitter provides a current path from the receiver power supply to the transmitter power supply. On the receiver side, the termination resistors are built into the receiver chip as required by the DVI specification. On the transmitter side, two possible causes are termination resistors or protection diodes.

b. Termination resistors to the transmitter power supplies provide a path between the power supplies of 12.5 Ω if 50-Ω resistors are used. This can prevent the transmitter system from powering off. See the transmitter termination resistor question above for additional discussion of those issues.

c. Protection diodes designed to clamp the DVI signals to the transmitter supply also clamp the transmitter supply to the DVI signals. The effect of these diodes and the receiver termination resistors is 8 parallel circuits of 50 Ω (receiver termination resistance inside IC) in series with a diode between the receiver and transmitter supplies. If the current requirement in the transmitter is low, the transmitter (3.3 V) supply likely goes to a diode drop below the receiver voltage. Nominally this might be 3.3 - .7 = 2.6 V. Other similar paths can exist through the 5 V, DDC, or hotplug pins of the DVI connector. Note that this issue can exist with any DVI system and is not unique to any part.

35. Why does the TFP410 not display an image on the HDMI device, but works fine on the DVI device?

a. This is likely an issue with HTPLG. Some monitors power their EDID circuit internally, leaving HPD always high. Others require 5 V from the connector before pulling HPD high–that is the one that is probably not working. You can try tying HTPLG high on your board or providing 5 V to the connector.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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