Application Report
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High-Speed ADC THS1041and FPGA Interface Considerations

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ABSTRACT

The Texas Instruments THS1041 is a 10-bit, 40-MSPS, high-speed analog-to-digital converter (ADC). For many years because of its low power dissipation and extended life, it has been used in various applications such as programmable gain amplifier and built-in clamp[1]. With recent FPGA development, some application systems have been upgraded with a direct interface of the THS1041 to an FPGA, for example, by connecting I/O pins of the THS1041 to the I/O pins of Xilinx™ Spartan-3 or Altera™ program logic device (PLD). For such an interface, a power-on initial state should be considered in the interface design. Otherwise, the power-on initial state of the FPGA can affect the initial state of THS1041 and in some cases, affect the entire application system. In order to ensure the successful interfacing of the THS1041 to an FPGA, a test was conducted, and this application report presents those results.

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1 Mode Control of THS1041

The THS1041 can be configured to have different operating modes with either internal reference or external reference. For the user's convenience, this is summarized by a flow chart shown in Figure 1. Basically, by connecting the MODE pin to either GND, AV_{DD}, or $AV_{DD}/2$, the internal or external reference mode can be determined, and the current direction at the reference pin is defined. By setting a different voltage level on the Refsense pin, the voltage at the reference pin will be different and the input full-scale range is determined. In addition, the THS1041 has three registers for controlling internal functions (PGA gain, DAC voltage, and Clamp disable) and one reserved register for future use. All the modes in Figure 1 have the same digital data input or output (I/O) control that is described in the next section.

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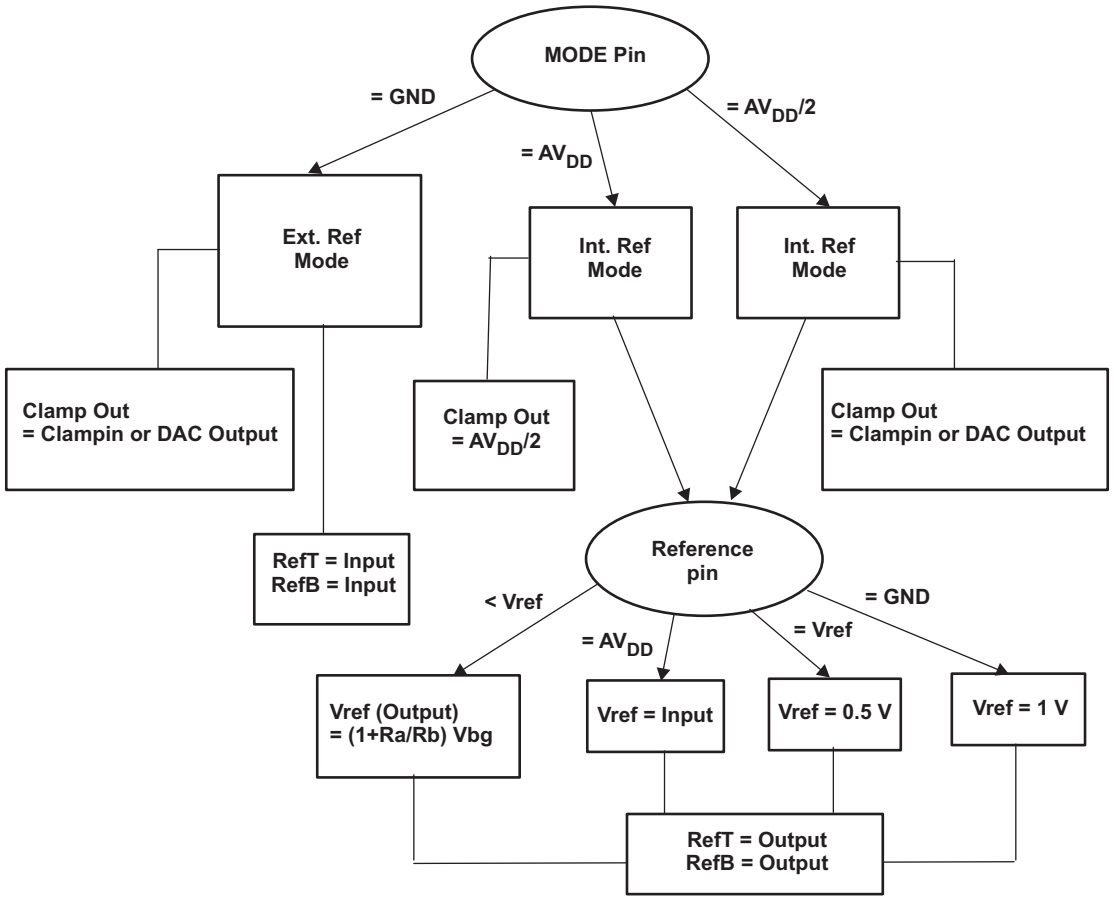

Figure 1. THS1041 Mode Setting

2 I/O Control of THS1041

The THS1041 has two pins for controlling the input/output (I/O) state, sending ADC conversion data out or receiving ADC control data from other logic devices. This digital input and output activity is controlled by pin $\overline{OE}$ and pin WR through the I/O bus, bit 0 to bit 9. At the data output state, bits 0 to 9 on the I/O bus hold a 10-bit ADC data word. At the data input state, bit 9 and bit 8 (two MSBs) on the I/O bus are the address bits for accessing the registers, whereas the rest of the bits on the I/O bus (bit 0 to bit7) are used for loading control data to the register. When $\overline{OE}$ is held low, the I/O bus is ready for sending ADC data out. When $\overline{OE}$ is pulling to high, the internal output drive is in a high-impedance state and the I/O bus is ready for data input. After $\overline{OE}$ is high for at least 12 ns, pulsing WR goes high and then low to latch the data on the I/O bus into the chosen register. The logic timing of register-writing is shown in Figure 2.

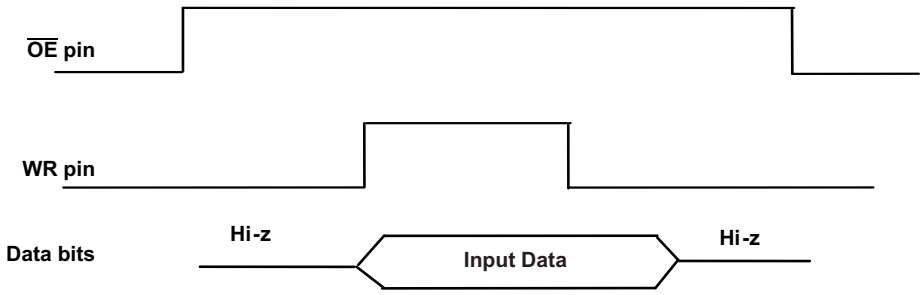

Figure 2. THS1041 Register-Writing Logic Timing

Specific timing of the register-writing is that time between the rising edge of $\overline{OE}$ and the rising edge of

WR, i.e., $t_{d(OEW)}$ and should be longer than 12 ns. The time between the falling edge of WR and the falling edge of $\overline{OE}$ should be longer than 12 ns. The duration of WR should be longer than 15 ns. The data setup time, i.e., data valid to center of the falling edge of WR, should be longer than 5 ns and the data hold time, i.e., center of the falling edge of WR to data invalid, should be longer than 5 ns. Delay between the rising edge of WR and the edge of the input data is not required. The control of $\overline{OE}$ and WR can be from hardware or software switches. The timing is also described in the timing table of the data sheet, THS1041 (SLAS289).

3 Observation on Interface Between THS1041 and FPGA

In an application system, the $\overline{OE}$ and WR pins of the THS1041 can be connected to GND for fixed I/O state or connected to the digital I/O pins of other device for flexible control. The data I/O bus of the TH1041 is generally connected to the data I/O bus of other devices for data driving or loading. In general, the THS1041 can communicate well with other devices without being affected by the interface of the other devices; but in some cases, it can be affected by the I/O stage of those devices after two devices power on. Two such cases from applications are described as follows.

- **Case a:** in this application, the THS1041 I/O bus, including $\overline{OE}$, WR, and the data pins, is connected to the I/O pins of Xilinx FPGA, Spartan 3. Sometimes, the ADC shows a constant output 0x3FF at the data bus after power on; the analog input has no signal in this case. So, the ADC is not in a *wake up* mode.
- **Case b:** In this application, the THS1041 I/O bus, including $\overline{OE}$, WR, and the data pins, is connected to the I/O pins of a PLD, Altera Acex EPLD. After the power-up and after waiting for a time, for example, 100 ms, the FPGA switches to a user mode; then, some ADCs outputs stay at a constant data 0x31F with any analog input signal. In this case, reprogramming register 0, 1, and 2 does not change the output state of the THS1041.

These two cases have a common configuration, that is, the THS1041 interfaces to the FPGA, which resulted in a weak pull-up in the I/O stage. Also, both of these cases occurred at the power-on initial time, and an accidental invalid code was on the I/O bus of the THS1041. This invalid code is relative to the reserved register, register 3. In the next section, a detailed analysis and test for these cases are presented.

4 Application Analysis and Test

When all ADC digital signal pins (data bits, OVR, WR, $\overline{OE}$, and CLAMP, even CLK) are directly connected to the I/O pin of FPGA, they are weakly pulled up to logic high by the FPGA after power on. This is because the FPGA I/O stage is at a high-impedance state or has a weak pull-up internally after power on. As mentioned in a previous section, when $\overline{OE}$ is logic high, the I/O bus of the THS1041 is ready for receiving data. In this case, if two MSBs are logic high, the reserved register, register 3, is open for new data. If WR is falling from logic high to low for any reason, register 3 is written with 1s; this is undesirable because the default value of this register should be 0s. For further verification, register 3 was tested and that test is described as follows.

A small pattern was created to verify the case on tester A580. Basically, either a HIGH or LOW signal is applied to the analog input to check if the ADC is working while the reserved register 11 is filled with varied values through I/O pins. If it functions correctly, then all I/O pins should be HIGH when the input is High; the same applies when the logic is LOW. The verification process can be expressed by a flow chart as shown in Figure 3.

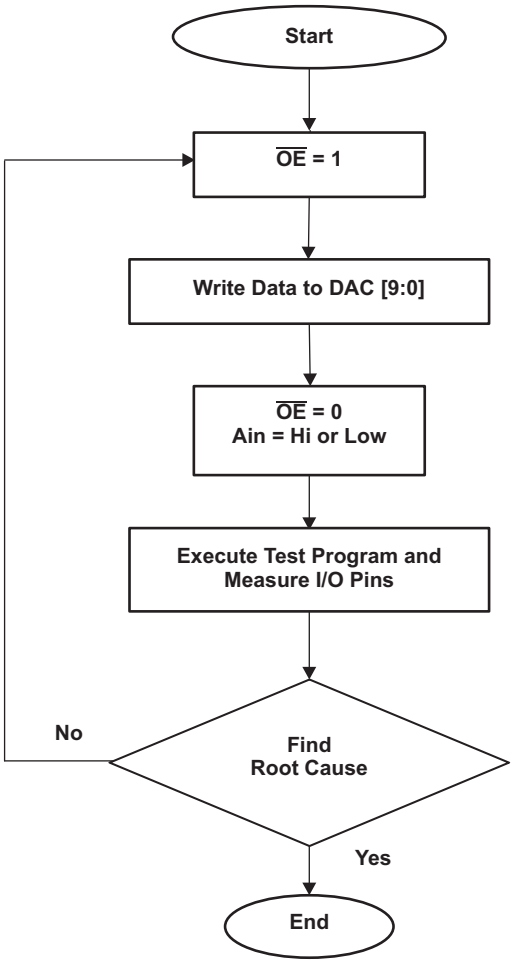

Figure 3. Process to Find Root Cause

The following test results show how an ADC responds to different initial statuses of the I/O bits.

Test 1: write all 1s in I/O bit 0~7 (i.e., 1111111111) to reserved register 11 (register 3) as shown in Table 1, and then test ADC units. In this test, all 10 good units tested failed.

Table 1. Setup and Results With all 1s in I/O Bit 0~7

ADDRESS I/O		DATA I/O								STATUS
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	1	1	Failed

Test 2: reset units, i.e., write all 0s in bits 0~7 (i.e., 1100000000) to reserved register 11 (register 3) as shown in Table 2. All 10 units passed that failed in test 1. Test results reveal that ADC units are able to work normally after register 3 is written with 0s.

Table 2. Setup and Result With All 0s in I/O Bits 0~7

ADDRESS I/O		DATA I/O								STATUS
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
1	1	0	0	0	0	0	0	0	0	Passed

Further testing: Tests 1 and 2 are an initial survey to discover if the units still function well with an unknown initial status at the I/O port; but they are inadequate to find the root cause and reveal the specific bit that makes the units become stuck. Hence, a more detailed experiment is conducted at this point. This is a complete bit-by-bit investigation. Writing 1 to reserved register 11 begins with bit 7, i.e., 1110000000 and so on and executes the A580 test program. Table 3 is the summary of this test.

Table 3. Setup and Result With Different Combination of All 0s and 1s in I/O Bits 0~7

ADDRESS I/O		DATA I/O								STATUS
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	0	0	0	0	0	0	Passed
1	1	1	1	1	0	0	0	0	0	Passed
1	1	1	1	1	1	0	0	0	0	Failed
1	1	0	0	0	0	1	1	1	1	Passed
1	1	1	1	1	0	1	1	1	1	Passed
1	1	0	0	0	0	0	0	0	0	Passed
1	1	0	0	0	1	0	0	0	0	Failed

Experiments show that failure or passing of the tested ADC units is determined by bit 4 of the reserved register. It has nothing to do with the condition of the other bits. That is why the ADC failed at Case a and b previously mentioned if the I/O bus stays steady 0x31F or 0x3FF at the receiving state after power up. The test shows that all units are able to recover to normal operation after the writing of 0s to reserved register has occurred after they were stuck.

4.1 Solution

Based on the preceding analysis and test, two solutions can be used to solve this problem. The first solution is a hardware solution, which is to add a small pulldown resistor (about 5 kΩ) at the WR line to pull down the voltage at the WR pin initially after the power on. This can avoid the generation of a WR falling edge before the WR pin receives a write signal from the FPGA and avoids initial data from the ADC data bus to be written into the register 3. This is the simplest way to avoid the initial invalid code being written to register 3, but if the board is already laid out, this method is impractical.

The second solution is by software in which 0x00 is sent to register 3. This creates a device initial reset or real time reset after the problem has occurred. Testing confirmed that sending 0x00 into register 3 as a reset command is safe to all operating condition. Also, accessing register 3 is safe at any time. For more accuracy, bit 4 of the reserved register 3 cannot be "1" at any time; so, when issuing the WR signal, one has to make sure that bit 4 of reserved register is set as "0". By applying these two solutions, the problem is gone and ADC works well with real systems.

4.2 Conclusion

In some applications, the I/O pins of the THS1041 are connected directly with I/O pins of the FPGA (Xilinx Spartan3, Altera Acex EPLD). In these cases, after the system power up, some THS1041 devices stay at a fixed state at its output sometimes, for example, 0x31FF forever. This is because the I/O stage of FPGA has an internal weak pull up, about 35 kΩ, and it pulls the $\overline{OE}$ and WR pins of the THS1041 to logic high; therefore, the data bus of the ADC appears as a high-impedance state. When this happens, the ADC is actually in write-mode and the falling edge (issued by the FPGA or accidentally happened) of WR sends the data on the data bus into the register. The initial bits on the data bus are sometimes all logical high due to internal pull up of the FPGA, and it could cause the reserved register (register 3) to be written with 1s. The register 3 is invalid for use in the current IC, and it should be set to “0” at all times. Two solutions can solve this problem. One is to add a pulldown resistor (about 5 kΩ) at the WR line and another is to send 0s into the reserved register. These two solutions make the THS1041 work safely with the interface of FPGA. The test data, application analysis, and the solution in this application report are also useful to other ADCs in the same family.

5 Reference

[1] Liu, Hui-Qing; *Clamp Function of High-Speed ADC THS1041*; Analog Application Journal 4Q06.

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