Application Report
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Wideband Complementary Current Output DAC to Single-Ended Interface: Improved Matching for the Gain and Compliance Voltage Swing

ABSTRACT

High-speed digital-to-analog converters (DACs) most often use a transformer-coupled output stage. In applications where this configuration is not practical, a single op amp differential to single-ended stage has often been used. This application note steps through the exact design equations required to achieve gain matching from each output as well as a matched input impedance to each of the DAC current outputs. An example high-speed design is shown using the very wideband, current feedback OPA695 op-amp with additional suitable parts included in a summary table.

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1 Typical High-Speed DAC Output Interface Circuits

Emerging high speed DACs use a complementary current-steering output structure. This design generates a differential signal current determined by the input coding sitting on top of an average common-mode current determined by one-half of the maximum tail current (which is sometimes an adjustable feature in the DAC). Most data sheet characterizations are taken with a very simple transformer output interface. A typical circuit from the DAC5675A (a 14-bit, 400-MSPS device) is shown in Figure 1.

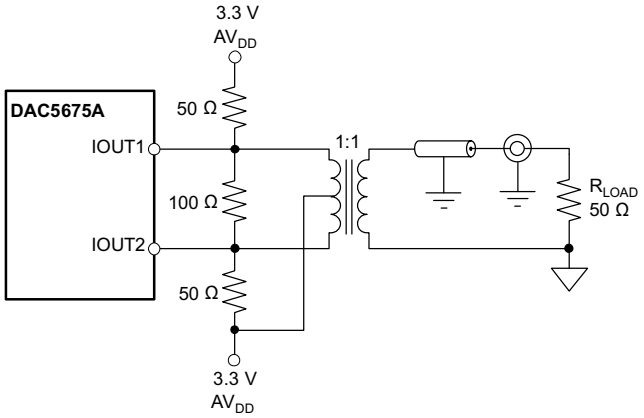


Figure 1. Typical Output Interface for a High-Speed, Current Steering Output DAC

This particular DAC wants to sink current from a supply voltage that is equal to the positive supply voltage of the DAC. It also has limited compliance voltage below that level — in this case, only a 1-V swing below AV_{DD} is allowed. Other DACs drive current into ground and look for a ground-referenced external load to convert the current to a voltage. A circuit similar to that shown in Figure 1 is nearly always used to develop the DAC performance specifications.

Where a transformer interface is not suitable, a single amplifier differential to single-ended conversion may be implemented. This configuration would be useful where lower frequencies, or a DC-coupled interface, are required out of the DAC. Additionally, a single SOT23 amplifier is more suitable where minimal board area for the interface is desired. Figure 2 illustrates a typical interface shown in some DAC datasheets.

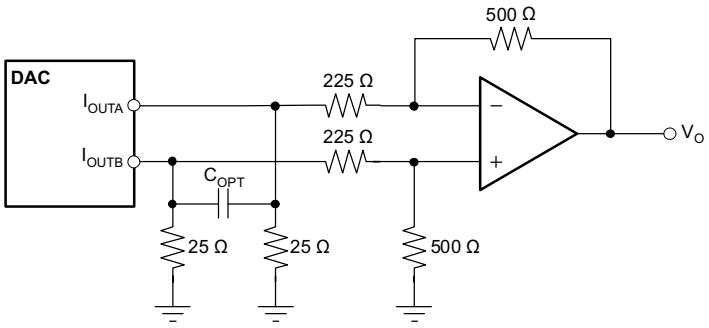


Figure 2. DC-Coupled, Differential to Single-Ended DAC Interface

This 20-mA peak output current DAC is looking for a 25-Ω termination impedance and is driving current into ground — thus, the ground-referenced load resistors. This relatively simple-looking circuit is, however, not giving a matched gain nor a matched input impedance for the two current source outputs. As DAC speeds have increased, the resistor values around this amplifier stage need to be relatively low in order to avoid parasitic bandlimiting. This condition causes this simple equal resistor design approach to be increasingly in error if matched voltage swings at the DAC outputs are desired. C_{OPT} is used to slow the DAC update edge rates as an optional element.

While this design may still yield acceptable results in the application, it is a simple matter to adjust these resistor values slightly to get perfect gain match from the two output currents to the amplifier output and also provide exactly the same apparent resistive load to each output. Implementing this adjustment also moves in the direction of giving better channel linearity and, therefore, lower distortion. Achieving matched gain magnitudes also moves the mid-scale DC output (when both output currents are equal to I_P / 2) closer to 0 V at the op-amp output. The designs here assumed bipolar supplies for the op-amp where a 0-V output is desired when each DAC channel is at (I_P / 2), midscale. While there might be other, more dominant, distortion mechanisms that mask this improvement, it is preferable to remove this unmatched output voltage swing as a possible source of imbalance.

To balance this design, start with the full design circuit of Figure 3, and write the gain and input impedance equations looking into each port. Define the desired gain as G (which will be an impedance) and input impedance Z_i (which will also be an impedance).

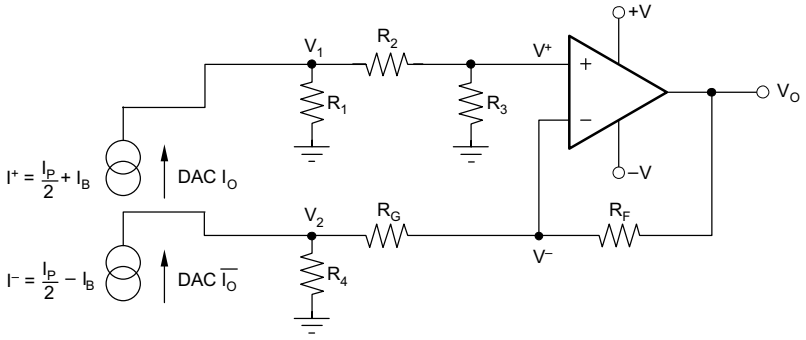


Figure 3. Analysis Circuit for Single Amplifier (Differential to Single-Ended Conversion)

From a solution standpoint, there are six resistors to find here and only four design targets. Consequently, a single unique solution is not possible without two more targets. To simplify this design, select a feedback resistor value and then also simply select R_2 as a scaled version of R_1. An alternative condition on the non-inverting network might be to get matched source impedances for the op-amp bias current to reduce output DC offset (if the op-amp is a voltage feedback type). Because a current feedback amplifier was anticipated here, with unmatched input bias currents, no *source matching* constraint was imposed.

The feedback resistor is a common gain element to both DAC current outputs and needs to be selected for best bandwidth if a current feedback amplifier is used in the circuit of Figure 3. Even if a voltage feedback amplifier is used, R_F needs to be set at a relatively low value for high-speed designs in order to minimize interaction with inverting input parasitic capacitance. On the non-inverting input side, the DAC I^+ current sees a relatively simple input impedance to generate the voltage at R_1. This voltage is then attenuated to the V^+ input by R_2 and R_3. Getting from the voltage at R_1 (V_1) to the V^+ input also needs to be done with relatively low resistor values to avoid parasitic bandlimiting due to the input capacitance at V^+.

The design proceeded with an assumption that R_2 will be set to a ratio of R_1. An added consideration in scaling the R_2 to R_3 divider is that these resistor values must be low enough that the apparent source impedance looking out of V^+ does not become a dominant noise contributor, either because of the Johnson noise of the resistors or the gain provided to the non-inverting input noise current by the equivalent source impedance (R_3 || [R_1 + R_2]).

2 Detailed Design Equations

Starting at the I^+ input, the input impedance will be:

$$Z_i = R_1 \parallel (R_2 + R_3) \tag{1}$$

Once we have that impedance, and set it equal to the target value of Z_i, there will be a simple resistor divider to the V^+ input that we will define as $\alpha = R_3 / (R_2 + R_3)$.

$$\frac{V^+}{I^+} = \alpha Z_i \tag{2}$$

A simple approach would then assume that $V^- = V^+$. For a voltage feedback amplifier, that is normally a good assumption if the loop gain is high. For a current feedback amplifier, there is a buffer between the two inputs that has a gain slightly less than 1.00 (1). That slight gain loss is included in this analysis as a β term; therefore, the gain from the current source at the non-inverting input to the op-amp output will be:

Non-inverting gain:

$$\frac{V_o}{I^+} = \alpha Z_i \beta \left(1 + \frac{R_F}{R_G + R_4}\right) = G \tag{3}$$

where

- G is the desired gain in Ω.

The approximate value of this buffer gain can be derived from the reported CMRR for the current feedback amplifier chosen. Equation 4 gives the conversion from CMRR to buffer gain for a current feedback amplifier:

$$\beta = \left(1 - 10^{\left(\frac{-CMRR}{20}\right)}\right) \tag{4}$$

Note that this non-inverting gain includes the termination resistor to ground on the inverting input side (R_4). This term has often been neglected in setting up these circuits because R_4 is often << R_G. In higher speed circuits, this becomes less true as R_G becomes lower and R_4 needs to be included in the equation for the I^+ gain.

On the inverting side, the gain for I^- is relatively simple. By superposition, we get a current divider to set the current into R_G, then the R_F resistor as the gain to the output. This value will again be set to the target gain of **G**; note also that this value is actually an inverting gain, where a current into the input gives a negative-going output. Equation 5 assumes this condition, and works only with the gain magnitude.

Inverting gain:

$$\frac{V_o}{I^-} = \frac{R_4}{R_4 + R_G} R_F = G \tag{5}$$

The inverting input impedance is a more interesting question. At first look, it would appear to simply be the parallel combination of $R_4 \parallel R_G$. However, if we think about what voltage will be generated at this DAC output pin (V_2), we need to consider that an inverted current version is simultaneously going into the other side of the circuit, producing an inverted voltage swing at V^-. This dependent source will have the effect of slightly reducing the apparent impedance of the R_G resistor when we realize that V^- is moving simultaneously in the opposite direction of V_2. Figure 4 shows the analysis circuit for this inverting input impedance.

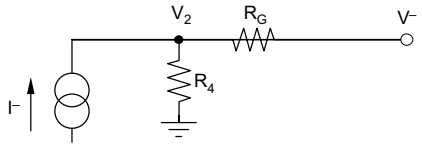


Figure 4. Inverting Z_i Analysis Circuit

Steps to resolve the apparent input impedance looking into R_4:

$$I_B = \frac{V_2}{R_4} + \frac{V_2 - V^-}{R_G}$$

where

- I_B is the signal portion of I^- in Figure 3 (6)

but:

$$V^- = -I_B Z_i \alpha\beta \quad \text{[non-inverting input } Z_i\text{]} \tag{7}$$

from the non-inverting side. Grouping terms, we get:

$$I_B\left(1 - \frac{Z_i \alpha\beta}{R_G}\right) = V_I\left(\frac{1}{R_4} + \frac{1}{R_G}\right) \tag{8}$$

Then:

$$\text{Inverting } Z_i = \frac{V_2}{I_B} = \left(R_4 \parallel R_G\right)\left(1 - \frac{Z_i \alpha\beta}{R_G}\right) \tag{9}$$

with the non-inverting Z_i assumed equal to the inverting (as a design goal), and after some manipulations to isolate Z_i:

$$Z_i = \frac{R_G}{1 + \frac{R_G}{R_4} + \alpha\beta} \tag{10}$$

Using the two gain equations and the inverting input impedance Equation 10, a solution for R_G may be derived as the solution to the quadratic Equation 10 (see Appendix B).

$$R_G{}^2 + R_G\left(R_F - 2G - \frac{Z_i R_F}{G}\right) - Z_i R_F\left(\frac{R_F}{G} - 1\right) = 0 \tag{11}$$

Once R_G is determined to simultaneously satisfy the two gain and inverting input impedance equations (Equation 11), work backwards to calculate values for the remaining elements. Specifically, set R_4 to get the desired gain for the inverting input current, according to Equation 12, by solving Equation 5 for R_4:

$$R_4 = \frac{R_G}{\frac{R_F}{G} - 1}$$

- (from Appendix B, Equation 21). (12)

Then set $\alpha\beta$ to get the non-inverting gain by solving Equation 3 for $\alpha\beta$:

$$\alpha\beta = \frac{G}{Z_i\left(1 + \frac{R_F - G}{R_G}\right)} \tag{13}$$

Using the known value for β (or set $\beta = 1$ for a voltage feedback amplifier), we can solve for α by dividing the result above by β.

Then from α and Z_i:

$$R_1 = Z_i\left(1 + \frac{1 - \alpha}{\lambda}\right) \tag{14}$$

This calculation finds the necessary resistor to ground at I^+. Then, to set R_2 and R_3, simply pick R_2 = some ratio of R_1 (typically, 2 or lower, defined as λ):

$$R_2 = \lambda R_1 \quad \text{just pick } \lambda \tag{15}$$

Choose $\lambda < 1$ to reduce the apparent source impedance for the V^+ input; choose $\lambda > 1$ if R_1 as the dominant portion of the non-inverting input Z_i is desired.

$$R_3 = \frac{\lambda \alpha R_1}{1 - \alpha} \tag{16}$$

3 Example Design Using Very Wideband Current Feedback Amplifiers

To see the difference that this more detailed design approach gives, consider a design using the OPA695 wideband current feedback amplifier where the DAC wants to see a 25-Ω load impedance to ground on each output, and we want 50-Ω gain to the op-amp output for each half of the output signal. This design should give a 100-Ω total gain from the I_B (as defined here) to the output voltage. The OPA695 is looking for a feedback resistor in the 500-Ω region and quotes a typical CMRR of 56 dB. That 56-dB CMRR translates into a $\beta = 0.99842$ for the buffer gain across from V^+ to V^- (Equation 4). With a 500-Ω feedback, the OPA695 will give > a 600-MHz bandwidth.

As an initial design, consider the more typical approach shown in Figure 5. Here, the termination resistors (R_1 and R_4) are simply set to 25 Ω ; the amplifier resistors are set to 500 Ω and 250 Ω to achieve a gain of 2 × 25 Ω = 50 Ω to the output for both I^+ and I^- (approximately, as we will see).

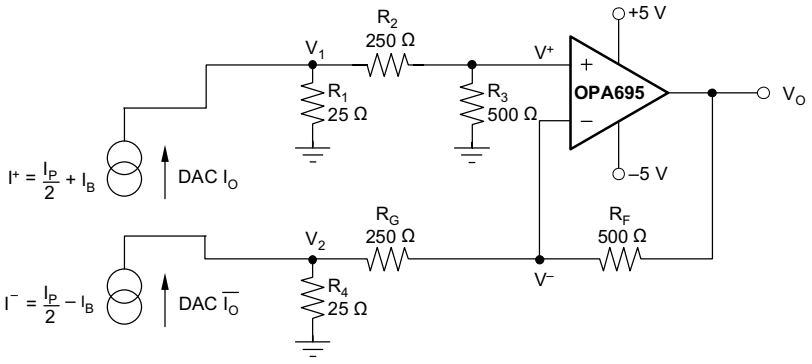


Figure 5. Initial Design Using the OPA695

Now, use the equations developed above to adjust the resistors slightly to improve the gain match and input impedance match to the desired targets. This adjustment is shown in Figure 6, where the feedback resistor stays at 500 Ω ; all the other values have adjusted slightly. This new design is showing resistor values to two decimal places. This precision is not possible in practice, but was carried through here to allow a comparative simulation to be made showing ideal conditions. Here, $R_2 = 2 \times R_1$ was selected.

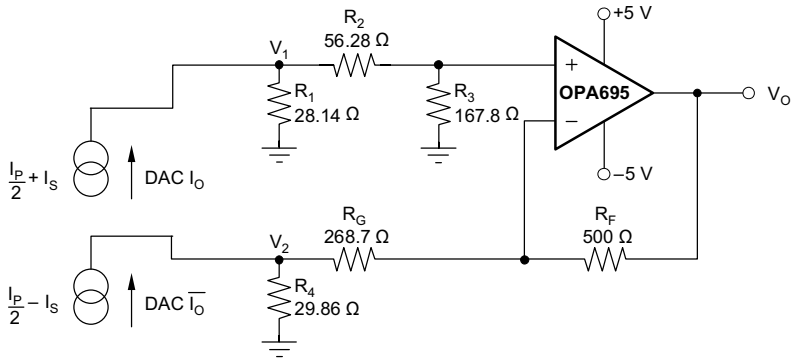


Figure 6. Improved Design Using the OPA695

The ideal gain for I_B to V_O should be 100 Ω, or 40 dB in log terms. Figure 7 illustrates the simulated gain for the designs in Figure 5 and Figure 6, showing that the values of Figure 6 approach the desired 40-dB gain much more closely.

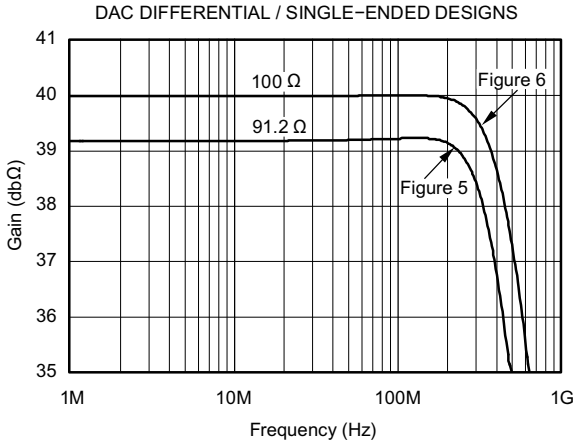


Figure 7. Simulated Frequency Response Comparison

If the two input impedances are matched, adding V_1 and V_2 should yield 0 V (recognizing that with matched magnitudes of input Z, the signal voltages will be inverted from each other at V_1 and V_2). Figure 8 compares the swept frequency addition of (V_1 + V_2) in log terms. This value is simply the difference in the apparent input impedance at each current source output. The 9 dB of the initial design translates into a 2.8-Ω difference, while the –46 dB of the improved design at low frequencies translates into a 0.005-Ω difference. For a 20-mA output DAC, the design of Figure 5 would see a 56-mV difference in the V_{PP} on the output current sources, while the result of Figure 6 would only be a 0.1-mV difference in the voltages (V_{PP}) appearing at each DAC output. As we can see, the improved design of Figure 6 does a much better job of achieving matched input impedances at the two DAC outputs. To the extent that a small portion of the final distortion might be a result of an unmatched voltage swing on the two DAC outputs, this improved design should remove that unmatched voltage swing as a possible source of distortion.

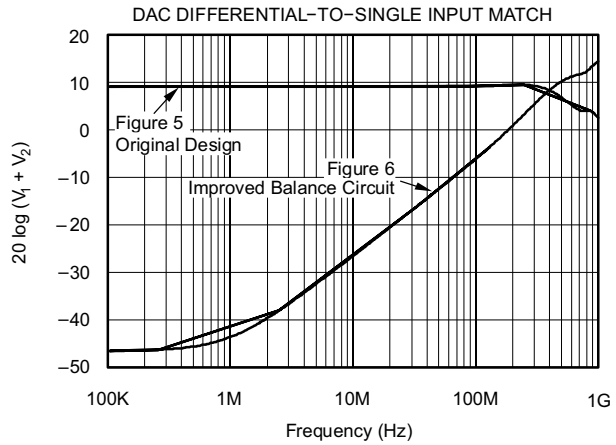


Figure 8. Simulated Difference in the Input Voltage

The improved design is showing a low frequency delta of –46 dB, which translates into a 0.005-Ω difference in the input impedances. The increasing slope of the improved curve of Figure 8 traces out the rolloff in the open loop transimpedance gain for the OPA695 (a current feedback amp). As frequency increases, more inverting error current is required to generate the output voltage. This error current increase also acts to increase the apparent input impedance looking into V_2. This effect is very slight, and only becomes significant at very high frequencies. The improved plot in Figure 8 only shows a delta input impedance that rises above 1 Ω (0 dB) beyond 200 MHz.

Another way to look at this input impedance match is to simply look at the apparent impedance at V_1 and V_2 over frequency. We can see a frequency dependence as a result of the parasitic input capacitances on the two op-amp input pins and the loop gain rolloff at very high frequency. Figure 9 shows the input impedance for the simple design of Figure 5.

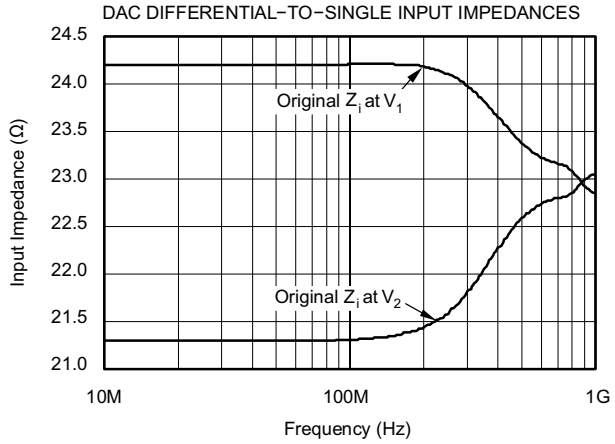


Figure 9. Input Impedance at V_1 and V_2 for Original Design

This plot clearly indicates that the two input impedances are quite mismatched — even at low frequencies. Figure 10 shows the input impedance for the improved design of Figure 6.

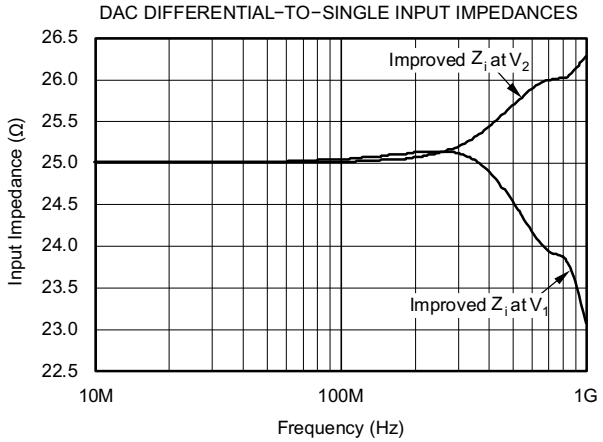


Figure 10. Improved Design Impedance at V_1 and V_2

This plot illustrates a better match on each side to the 25-Ω target, with an increasing deviation above 300 MHz.

4 Bandwidth and Noise Considerations

So far, this discussion has been directed at improving the input impedance match and getting the target gains from each DAC output current to the amplifier output. The specific resistor values chosen also influence the AC characteristics for the final design. In general, higher resistor values produce more noise to the output pin of the op-amp. If the amplifier is a current feedback type, the value of the feedback resistor always controls the bandwidth. Increasing R_F from its recommended value bandlimits the design, while decreasing it peaks the frequency response up, thereby extending the bandwidth.

Figure 11 shows the spot-noise calculation circuit for any op-amp.

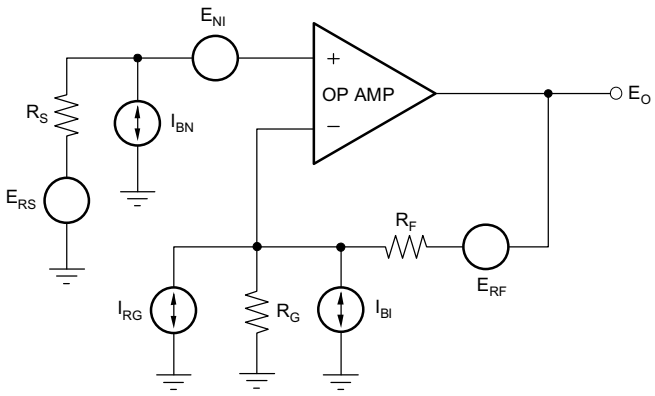


Figure 11. Output Noise Analysis Circuit

For the design of Figure 3, the R_S resistor is (R_3 || [R_1 + R_2]), and the R_G resistor for this noise calculation is the sum of the R_G + R_4. The other term needed is the noise gain, G_N. This term is the non-inverting voltage gain, and is equal to:

$$1 + \frac{R_F}{(R_G + R_4)} = G_N \tag{17}$$

for the circuit of Figure 3. With all of these terms known, the total spot output noise density is given by Equation 18 (2):

$$E_o = \sqrt{\left(E_{NI^2} + (I_{BN}\, R_S)^2 + 4k\,T R_S\right) G_{N^2} + (I_{BI}\, R_F)^2 + 4kT\, R_F\, G_N} \tag{18}$$

All current feedback op-amps have a relatively high inverting input current noise, while most (but not all) have a relatively high non-inverting input current noise. To limit the contribution of these current noise terms, it is preferable to use relatively low resistor values for both the feedback resistor and the terms that make up R_S in Equation 18. To reduce the source R_S on the non-inverting input, the next design scales the R_2 resistor to target a lower value than R_1 and still achieve the required impedance and gain targets.

5 Improved Component Selection and Results With Standard 1% Values

Let us repeat the design above and extend the bandwidth by picking a lower value for R_F; then reduce the noise as well, by selecting an $R_2 = 0.2 \times R_1$ (instead of $R_2 = 2 \times R_1$ that was used previously). Then, adjust the resistors to standard 1% values and repeat the input impedance and gain simulations over frequency.

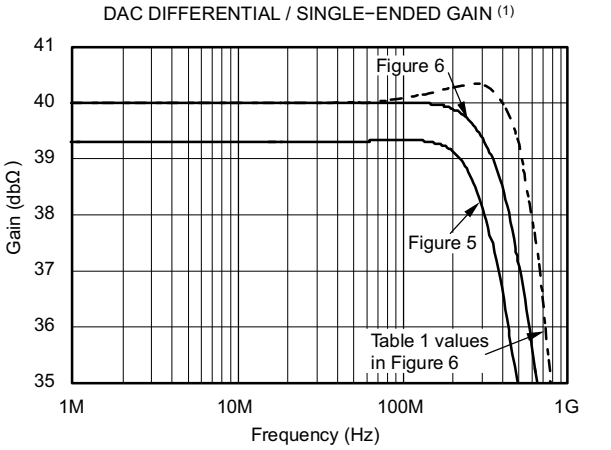
Select $R_F = 402\ \Omega$. Continue to target a gain of 50 Ω for each output and 25-Ω input impedance. Table 1 shows the exact values for the design and the standard 1% values used in simulation.

Table 1. Reduced Resistor Design With Standard Values Chosen

RESISTOR	EXACT VALUE (Ω)	ENTER STANDARD 1% (Ω)	COMPUTED RESULTS USING 1% VALUES
R1	53.63	53.6	Non-inverting Z_i = 24.87 Ω Equation 1
R2	10.73	10.7	Non-inverting gain = 49.51 Ω Equation 3
R3	36.11	35.7	Inverting input Z_i = 25.22 Ω Equation 10
R4	31.28	31.6	Inverting gain = 50.29 Ω Equation 5
R_G	220.24	221	
R_F	402.00	402	

The total output noise for the OPA695 interface alone is 11 nV/√Hz, using these reduced resistor values from Table 1. The total output noise for the circuit values shown in Figure 6 ($R_F = 500\ \Omega$ and $R_2 = 2 \times R_1$) is 13.4 nV/√Hz using the analysis of Figure 11.

Substitute the 1% values shown above into the circuit of Figure 3, then simulate the frequency response and input impedance difference over frequency. Figure 12 shows the frequency response (together with the earlier frequency responses) with this reduced R_F design. Figure 13 shows the 20 log ($|V_1 + V_2|$) for the two earlier designs and this 1% standard value design superimposed.



NOTE (1): 40 dB is 100-Ω gain from a single I_B output from the DAC.

Figure 12. Frequency Response Curves

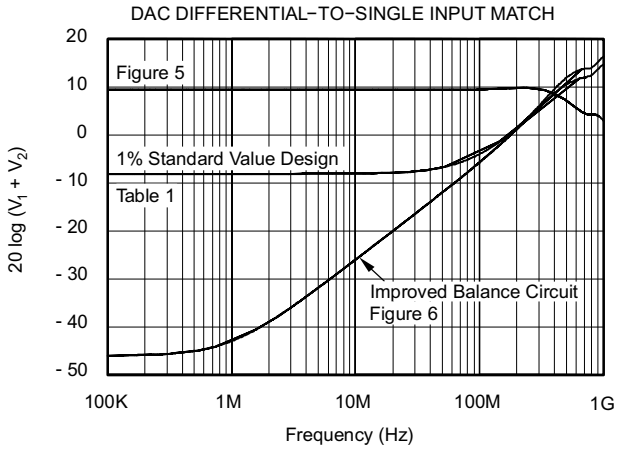


Figure 13. Difference in Input Impedances over Frequency

Working with this lower 40-Ω feedback has extended the bandwidth quite a bit with minimal peaking. The upper curve in Figure 12 is showing less than ± 0.5-dB deviation from 40-dB gain through 500 MHz, with a – 3-dB bandwidth of 700 MHz.

As for input impedance matching, this 1% standard value design comes in at a – 9-dB level — this translates into the approximate 0.3-Ω input impedance mismatch shown in Table 1. It then follows the high frequency curve of the ideal valued design above 100 MHz.

6 Conclusions

Using a bit more effort to design the single amplifier differential to single-ended interface for a DAC output can yield a more balanced design. The equations shown here adjust the resistor values slightly and balance the voltage swing seen by the DAC, thereby removing an imbalanced voltage swing as a possible source of spurious-free dynamic range (SFDR) degradation. From the exact values shown in Figure 6, standard values should be selected that are close to the specified values and still produce an improved performance over the simple design of Figure 5. Table 2 summarizes the key specifications for a range of high-speed amplifiers that may be used in this application. The table is sorted in ascending $2V_{PP}$ output bandwidth order. A design spreadsheet implementing the equations in this application note is available for download with this application note.

The spreadsheet, set to the values used for the reduced R_F and 1% standard value design of Table 1, is shown in Appendix B.

7 References

1. National Semiconductor, Steffes, M. (1993). *Current Feedback Amplifier Loop Gain Analysis and Performance Improvements*, Application Note OA-13
2. Texas Instruments, Steffes, M. (1996). *Noise Analysis for High-Speed Op Amps*, Application Note (SBOA066)

Table 2. Typical High-Speed Amplifiers for High-Speed DAC Interface Requirements(1)

PART NO.	VFB OR CFB	RECOM'D RF (Ω)	GAIN OF 2 BANDWIDTH (MHz)	SUPPLY CURRENT (mA)	CMRR (dB)	BUFFER GAIN (β) (2)	SLEW RATE (V/µs)	APPROX. $2V_{PP}$ BW (MHz)	INPUT NOISE TERMS			POWER SUPPLY RANGE $V_{S+} - (-V_{S-})$		COMMENTS
									E_N (nV)	I_{BN} (pA)	I_{BI} (pA)	MIN (V)	MAX (V)	
THS4031	VFB	330	100	7.5	95	1	100	23	1.60	1.20	1.20	9.00	32.00	Low noise, ±15 V capable
OPA820	VFB	402	250	5.6	85	1	240	54	2.50	1.70	1.70	4.00	12.60	Low noise, good DC precision
OPA355	VFB	604	170	8.3	80	1	300	68	5.80	0.05	0.05	2.70	5.501	CMOS Rail-to-rail output
THS3111	CFB	1000	90	4.8	68	0.9996	900	90	3.00	2.00	10.00	9.00	32.00	Low noise, ±15 V capable
OPA842	VFB	402	150	20.2	95	1	400	90	2.60	2.80	2.80	8.00	12.60	Very low distortion
OPA830	VFB	750	120	4.3	80	1	600	120	9.50	3.70	3.70	2.90	10.50	Rail-to-rail output
THS3121	CFB	649	120	7.0	70	0.9997	900	120	2.50	1.00	10.00	9.00	32.00	High output, ±15 V capable
OPA683	CFB	1200	150	0.94	60	0.9990	540	122	4.40	5.10	11.60	3.50	12.60	Very low quiescent power
OPA684	CFB	1000	160	1.7	60	0.9990	820	160	3.70	9.40	17.00	3.50	12.60	Low quiescent power
THS4304	VFB	250	1000	18.0	95	1	800	180	2.80	3.80	3.80	2.70	5.50	High bandwidth VFB
THS3091	CFB	1210	210	9.5	78	0.9999	7300	210	2.00	14.00	17.00	9.00	32.00	High slew rate, ±15 V capable
OPA690	VFB	402	220	5.5	65	1	1800	220	5.50	3.30	3.30	4.00	12.60	High slew rate VFB
OPA691	CFB	402	225	5.1	56	0.9984	2100	225	1.70	12.00	15.00	4.00	12.60	High output current (> 150 mA)
THS4271	VFB	250	390	22.0	72	1	1000	225	3.00	3.00	3.00	9.00	16.00	Very low distortion
OPA694	CFB	402	690	5.8	60	0.9990	1700	383	2.10	22.00	24.00	4.00	12.60	High slew rate on low power
OPA695	CFB	500	1200	12.9	56	0.9984	2900	653	1.80	18.00	22.00	4.00	12.60	High 3rd-order intercept

(1) Sorted according to ascending $2V_{PP}$ output bandwidth.
(2) CFB amplifiers only.

Derivation of the Quadratic in R_G

A.1 Derivation of the Quadratic in R_G

To solve for R_G:

$$\frac{R_4}{R_G + R_4} = \frac{G}{R_F}$$

[from inverting gain] (19)

Invert this to:

$$1 + \frac{R_G}{R_4} = \frac{R_F}{G} \quad (20)$$

And solve:

$$R_4 = \frac{R_G}{\frac{R_F}{G} - 1}$$

- (Use this as Equation 12) (21)

$$\alpha\beta Z_i\left(1 + \frac{G}{R_4}\right) = G$$

[from non-inverting gain]

- where (22)

$$\frac{R_F}{R_G + R_4} = \frac{G}{R_4} \text{ replaces: } \frac{R_F}{R_G + R_4}$$

- (from Equation 3) (23)

Substituting Equation 21 in place of R_4 in Equation 22 gives:

$$\alpha\beta Z_i\left(1 + \frac{G}{\frac{R_G}{\left(\frac{R_F}{G} - 1\right)}}\right) = G \quad (24)$$

$$\alpha\beta Z_i\left(1 + \frac{R_F - G}{R_G}\right) = G \text{ solve for } \alpha\beta \quad (25)$$

$$\alpha\beta = \frac{G}{Z_i\left(1 + \frac{R_F - G}{R_G}\right)} \quad (26)$$

Using the expression for inverting Z_i (Equation 9):

$$\frac{R_G}{1 + \frac{R_G}{R_4} + \alpha\beta} = Z_i \quad (27)$$

Putting Equation 20 and Equation 26 into this calculation produces:

$$\frac{R_G}{\frac{R_F}{G} + \frac{G}{Z_i\left(1 + \frac{R_F - G}{R_G}\right)}} = Z_i \tag{28}$$

We can now solve for R_G from Equation 28. From Equation 28, multiply denominator through:

$$R_G = Z_i\frac{R_F}{G} + \frac{G}{\left(1 + \frac{R_F - G}{R_G}\right)} = Z_i\frac{R_F}{G} + \frac{R_G G}{R_G + R_F - G} \tag{29}$$

Multiply:

$$\left(R_G + R_F - G\right) \tag{30}$$

through both sides:

$$R_G\left(R_G + R_F - G\right) = R_G G + Z_i\frac{R_F}{G}\left(R_G + R_F - G\right) \tag{31}$$

Expand the terms:

$${R_G}^2 + R_G\left(R_F - G\right) = R_G G + R_G\left(\frac{Z_i R_F}{G}\right) + {R_F}^2\frac{Z_i}{G} - Z_i R_F \tag{32}$$

Group the terms for a polynomial solution:

$${R_G}^2 + R_G\left(R_F - 2G - \frac{Z_i R_F}{G}\right) - \left(\frac{Z_i {R_F}^2}{G} - Z_i R_F\right) = 0 \tag{33}$$

Taking the positive solution to the quadratic in R_G:

$$R_G = G - \frac{R_F}{2}\left(1 - \frac{Z_i}{G}\right) + \sqrt{\left(G - \frac{R_F}{2}\left(1 - \frac{Z_i}{G}\right)\right)^2 + Z_i R_F\left(\frac{R_F}{G} - 1\right)} \tag{34}$$

One constraint from Equation 26 is that $\alpha\beta$ must be < 1. Solve for Equation 26 to equal 1:

$$\frac{G}{Z_i\left(1 + \frac{R_F - G}{R_G}\right)} = 1 \tag{35}$$

$$G = Z_i\left(1 + \frac{R_F - G}{R_G}\right) \tag{36}$$

Isolate on G:

$$\frac{G}{Z_i} + \frac{G}{R_G} = 1 + \frac{R_F}{R_G} \tag{37}$$

$$G\left(\frac{1}{Z_i} + \frac{1}{R_G}\right) = 1 + \frac{R_F}{R_G} \tag{38}$$

To get a solution:

$$G < \left(1 + \frac{R_F}{R_G}\right)\frac{R_G Z_i}{R_G + Z_i} = \frac{R_F + R_G}{1 + \frac{R_G}{Z_i}} = Z_i\left(\frac{R_F + R_G}{Z_i + R_G}\right) \tag{39}$$

To get a larger G, increase R_F.

Design Spreadsheet (Example)

B.1 Design Spreadsheet (Example)

The bold numeric entries indicate where design targets need to be entered, while the green cells are computed values.

To use the spreadsheet, follow this procedure:

- Select the part number from the table on the part list sheet.
- Enter the gain for each DAC output (in Ω), the desired input impedance for each DAC, the desired feedback resistor value, and then the ratio of R_2 / R_1.
- Select if the buffer gain loss should be considered.

All resistor values are then computed, and the total output noise (for the amplifier design only) is shown. Then, enter the closest standard resistor values and the actual design results will be re-computed.

DAC Complementary to single ended design spreadsheet. Design procedure and Assumptions
MICHAEL STEFFES - MAY, 2005
Define Target design elements. Select Part Number OPA695 Must be exactly as it appears in the first column of the Part Data.

Design Entry Cells

Desired single ended gain(G) ==>	G =	50 ohms	Non-inverting input network has too many R's for conditions - just need to set
Desired single ended input Zi =>	Zi =	25 ohms	Input Zi and attenuation from that Zi to the V+ input voltage - define that as alpha.
Feedback resistor value ==>		402 ohms	Recommended values is ==> 500 ohms
Set arbitray ratio of R2/R1 ===>	λ =	0.2	The lower this is the lower the total output noise will be.

Now compute some intermediate computation variables
Zi*Rf 10050

Do you want to account for CFB buffer gain loss across the input stage
Y Enter Y/N
CMRR for the selected amplifier 56 dB (this will give another loss from V+ to V- that can be accounted for in the R3/(R3+R2) design
Compute buffer gain from CMRR if it's a CFB device 0.99842 V/V

Now set up the coefficients for the 2nd order Rg polynomial

B0	B1	B2		Solve the quadratic for Rg
-70752	101	1	Rg ==>	220.244 ohms

Approximate maximum G given Rg, Rf &Zi ==> 63.4311 ohms Use this to iterate up or down on G to get a solution with non-negative resistors.

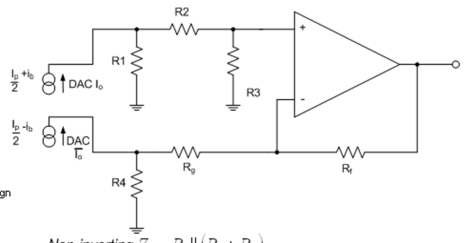
Now use this Rg value to continue solution

Inverting input termination Resistor R4 ==> 31.2846 ohms
Non-inverting attenuation from Zi, alpha ==> 0.77098 Alpha > 1 will yield no solution
Then, non-inverting input termination R1 ==> 53.6278 ohms
Then, arbitrarily set R2 = λ * R1 R2 ==> 10.7256 ohms This ratio can be changed if desired without impacting solutions
Then solve for R3 to the desired Alpha, R3 36.1063 ohms Change up above if desired.

Now go back and compute each sides input Z and gain to output pin
This is using the exact values and is just a check that nothing is going wrong.
On the non-inverting side -

Zi ===>	25 ohms		SUMMARY DESIGN VALUES		NOISE TERMS FOR AMPLIFIER
Gain to Vo	50 ohms		R1= 53.63 Ohms	En (nV)	1.80 nV
			R2= 10.73 Ohms	Ibn(pA)	18.00 pA
On the inverting side -			R3= 36.11 Ohms	Ibi (pA)	22.00 pA
			R4= 31.28 Ohms	Rs	23.13 ohms
			Rg= 220.24 Ohms	Eq. Rg	251.53 ohms
			Rf= 402.00 Ohms	Ngain	2.60 V/V
Zi ===>	25 ohms		Total Spot Output Noise for design	Total Eo =	10.98 nV/rootHz
Gain to Vo	50 ohms				

	Exact	Enter Standard1%		Computed results using 1% values	
R1=	53.63	53.6	Ohms	Non-inverting Zi =	25.10 Ohms
R2=	10.73	10.7	Ohms	Non-inverting Gain =	50.22 Ohms
R3=	36.11	36.5	Ohms	Inverting input Zi =	25.21 Ohms
R4=	31.28	31.6	Ohms	Inverting Gain =	50.29 Ohms
Rg=	220.24	221	Ohms		
Rf=	402.00	402	Ohms		



Non-inverting $Z_i = R_1 \| (R_2 + R_3)$

Define gain to V+ as αZ_i

Noninverting gian to $V_O = \alpha Z_i \beta \left(1 + \frac{R_f}{R_g + R_4}\right) \equiv G$

Where beta is the buffer gain loss given by $\beta = \left(1 - 10^{\frac{-CMRR}{20}}\right)$

Inverting gain to $V_O = \frac{R_4}{R_4 + R_g} R_f \equiv G$

Inverting input impedance $Z_i = \frac{R_g}{1 + \frac{R_g}{R_4} + \alpha\beta}$

Including V- as a driven node
Solution for R_g becomes

$$R_g^2 + R_g\left(R_f - 2G - \frac{Z_i R_f}{G}\right) - Z_i R_f\left(\frac{R_f}{G} - 1\right) = 0$$

then $R_4 = \frac{R_g}{\left(\frac{R_f}{G} - 1\right)}$ $\alpha\beta = \frac{G}{Z_i\left(1 + \frac{R_f - G}{R_g}\right)}$

then from α & Z_i

$R_2 = \lambda R_1$, just pick λ & $R_3 = \frac{\lambda \alpha R_1}{1 - \alpha}$

$R_1 = Z_i\left(1 + \frac{1 - \alpha}{\lambda}\right)$

Also, to get a solution $G < \frac{R_f + R_g}{1 + \frac{R_g}{Z_i}}$

Figure 14. Design Spreadsheet Example

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