THS6302 Dual Port, G.Fast and G.mgFast DSL Line Driver

1 Features

- Designed for G.Fast 106-MHz, 212-MHz DSL Profiles
- G.mgFast 424-MHz Compatible
- Supports legacy VDSL and ADSL2+ Applications
- Excellent MTPR for G.Fast and Legacy Applications (Line Power = 8 dBm):
  - ADSL2+ = 75 dB
  - VDSL-17a = 74 dB
  - VDSL-30a = 70 dB
  - G.Fast 106-MHz = 60 dB
  - G.Fast 212-MHz = 48 dB
- Multiple Power Modes for Different Profiles
- Adjustable Bias Current with External Resistor
- Differential Gain: 11 V/V
- Linear Output Current: 80 mA (Minimum)
- Low-Power Line Termination Mode: <7 mA
- Power-Down Mode
- 12-V Technology to Support High-Power Output
  - 12.6-V Maximum Operational Voltage

2 Applications

- G.Fast and Legacy DSL Line Drivers
- G.mgFast Compatible Line Drivers
- Generic Wideband Line Drivers

3 Description

The THS6302 is a dual port, current-feedback architecture, differential line driver designed for G.Fast and a variety of digital subscriber line (DSL) systems. The device is targeted for use in G.Fast digital subscriber line systems that enable native discrete multitone modulation (DMT) signals and supports an 8-dBm line power up to 212 MHz with good linearity.

The unique architecture of this device allows quiescent current to be minimal and still achieve very high linearity. Internally-fixed bias settings of the amplifiers offer enhanced power savings for line-driving modes where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, the overall quiescent current for both ports is adjustable by a single external bias resistor connected to one of the device pins. The device also features two line-termination modes to maintain impedance matching at very low power consumption.
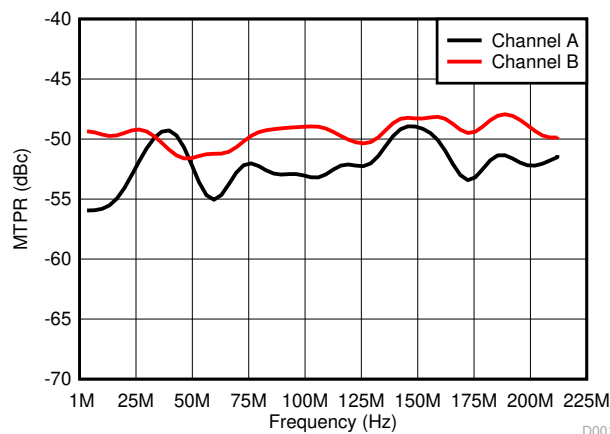
The THS6302 is a dual port device suitable for CO (Central Office) applications in DSL systems and is similar to the single port THS6301 device that is suitable in CPE (Customer-Premises Equipment) DSL applications.

THS6302 device is available in a 4-mm × 5-mm, 28-pin, VQFN package.

Device Information [(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS6302	VQFN (28)	4.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Multitone Power Ratio (MTPR) Profile (G.Fast, 212 MHz, 8 dBm)

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4 Revision History

Changes from Revision * (June 2016) to Revision A (February 2021)   **Page**
• First public release of production data sheet...1

5 Pin Configuration and Functions
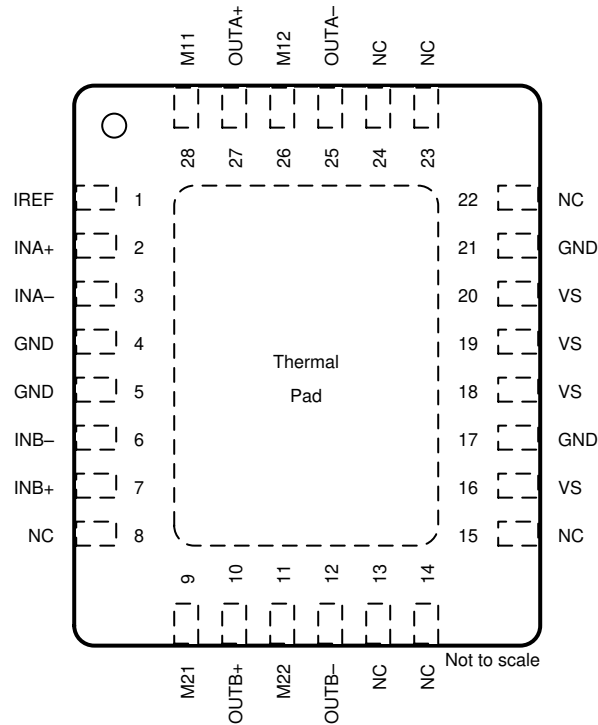
Figure 5-1. RHF Package 28-Pin VQFN Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IREF	1	—	Bias current reference pin
INA+	2	I	Positive input for channel A
INA–	3	I	Negative input for channel A
INB+	7	I	Positive input for channel B
INB–	6	I	Negative input for channel B
OUTA+	27	O	Positive output for channel A
OUTA–	25	O	Negative output for channel A
OUTB+	10	O	Positive output for channel B
OUTB–	12	O	Negative output for channel B
M11	28	I	Most significant bit (MSB) of channel A
M12	26	I	Least significant bit (LSB) of channel A
M21	9	I	MSB of channel B
M22	11	I	LSB of channel B
VS	16, 18, 19, 20	—	Positive supply voltage connection
GND	4, 5, 17, 21	—	Ground
NC	8, 13, 14, 15, 22, 23, 24	—	Not connected
Thermal pad		—	Device thermal pad, connected to ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1].

		MIN	MAX	UNIT
Supply voltage	VS pin to GND (all modes)		13.2	V
Digital inputs to GND	M11, M12, M21, M22	−0.3	5.5	V
Analog inputs to GND	VINA+, VINA−, VINB+, VINB−	−0.3	12	V
Continuous power dissipation		See *Section 6.4*		
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
	Power-supply voltage range	11.4	12	12.6	V
T_J	Operating junction temperature	−40		125	°C
T_A	Operating ambient temperature	−40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		THS6302 RHF (VQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = 25°C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IREF} = 75 kΩ, C_{IREF} = 100 pF, G.Fast 106-MHz bias mode, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
LSBW	Large-signal bandwidth	V_{OUT} = 15 V_{PP}, ADSL2+ bias mode		140		MHz
		V_{OUT} = 15 V_{PP}, VDSL 17a bias mode		180		
		V_{OUT} = 15 V_{PP}, G.Fast 106-MHz bias mode		220		
		V_{OUT} = 15 V_{PP}, G.Fast 212-MHz bias mode		320		
	Gain flatness referenced to 1 MHz	ADSL2+ bias mode, 4 kHz to 2.208 MHz		±0.001		dB
		VDSL2-17a bias mode, 4 kHz to 17.6 MHz		±0.02		
		VDSL2-30a bias mode, 4 kHz to 30 MHz		±0.02		
		G.Fast 106-MHz bias mode, 4 kHz to 106 MHz		±0.02		
		G.Fast 212-MHz bias mode, 4 kHz to 212 MHz		±0.2		
SR	Slew rate	ADSL2+ bias mode, 10%-90% 15-V_{PP} pulse		5100		V/µs
		VDSL2-17a bias mode, 10%-90% 15-V_{PP} pulse		6600		
		VDSL2-30a bias mode, 10%-90% 15-V_{PP} pulse		6600		
		G.Fast 106-MHz bias mode, 10%-90% 15-V_{PP} pulse		7400		
		G.Fast 212-MHz bias mode, 10%-90% 15-V_{PP} pulse		10600		
e_n	Input-referred voltage noise	f > 100 kHz, ADSL2+ bias mode		4.3		nV/√$\overline{Hz}$
		f > 100 kHz, VDSL2-17a bias mode		3.9		
		f > 100 kHz, VDSL2-30a bias mode		3.9		
		f > 100 kHz, G.Fast 106-MHz bias mode		3.7		
		f > 100 kHz, G.Fast 212-MHz bias mode		3.5		
	Noise floor (line-termination mode)	Output-referred, bias 00 and bias Z0		−152.5		dBm/√$\overline{Hz}$
	ADSL2+ MTPR	Line power = 8 dBm, f ≤ 552 kHz		66		dB
		Line power = 8 dBm, f ≤ 1.104 MHz		66		
		Line power = 8 dBm, f ≤ 2.208 MHz		66		
	VDSL2-17a MTPR	Line power = 8 dBm, f ≤ 14 MHz		72		dB
		Line power = 8 dBm, f ≤ 17.6 MHz		72		
	VDSL2-30a MTPR	Line power = 8 dBm, f ≤ 30 MHz		70		dB
	G.Fast 106-MHz MTPR	Line power = 4 dBm, f ≤ 106 MHz		67		dB
		Line power = 8 dBm, f ≤ 106 MHz		58		
	G.Fast 212-MHz MTPR	Line power = 8 dBm, f ≤ 212 MHz, bias 10		50		dB
	Crosstalk	ADSL2+ bias mode		127		dB
		VDSL2-17a bias mode		92		
		VDSL2-30a bias mode		82		
		G.Fast 106-MHz bias mode		85		
		G.Fast 212-MHz bias mode		75		

6.5 Electrical Characteristics (continued)

At T_A = 25°C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100-Ω load, R_{SERIES} = 47.5 Ω, R_{IREF} = 75 kΩ, C_{IREF} = 100 pF, G.Fast 106-MHz bias mode, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).

|	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
A_V	Differential gain	At dc, no load, all modes	10.5	11	11.5	V/V
	Differential output offset	G.Fast 106-MHz bias mode	−100		100	mV
	Maximum output swing	Differential, at dc, 200-Ω load at amplifier output	18			V_{PP}
	Linear output current	ADSL2+ bias mode, sourcing, output offset < 20-mV deviation	40			mA
		ADSL2+ bias mode, sinking, output offset < 20-mV deviation	40			
		G.Fast 212-MHz bias mode, sourcing, output offset < 20-mV deviation	80			
		G.Fast 212-MHz bias mode, sinking, output offset < 20-mV deviation	80			
COMMON MODE						
	Input CM bias voltage		5.9	6.0	6.1	V
	Output CM bias voltage		5.9	6.0	6.1	V
POWER SUPPLY						
	Maximum supply voltage	All modes			12.6	V
PSRR	Power-supply rejection ratio	f = dc	60			dB
I_Q	Quiescent current per channel	ADSL2+ bias mode		14.5	16.5	mA
		VDSL2 bias mode		19.5	22.0	
		VDSL2 high-power bias mode		28.0	32.0	
		G.Fast 106-MHz bias mode		23.0	25.5	
		G.Fast 106-MHz low-power bias mode		17.8	20.0	
		G.Fast 212-MHz bias mode		39.0	44.5	
		Line-termination high-power mode		9.5	10.5	
		Line-termination low-power mode		6.3	7.0	
		Power-down bias mode		1.35	1.7	
	Dynamic power consumption	ADSL2+ bias mode, line power = 8 dBm		219		mW
		VDSL2 bias mode, bias Z1		298		
		G.Fast 106-MHz bias mode, line power = 8 dBm		340		
		G.Fast 212-MHz bias mode, line power = 8 dBm		525		
		G.Fast 212-MHz bias mode, line power = 7 dBm		525		
		Line-termination high-power mode		115		
		Line-termination low-power mode		77		
		Power-down bias mode		19		

6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Minimum logic high level	All digital pins, high	2.3			V
V_{IL}	Maximum logic low level	All digital pins, low			0.6	V
V_{MID}	Logic mid range	All digital pins, driven externally	1.2		1.6	V
V_{Float}	Logic self-bias voltage	All digital pins, floating	1.3	1.4	1.5	V
I_{IH}	Logic high-level leakage current	All digital pins, logic level = 3.6 V		110	135	µA
I_{IL}	Logic low-level leakage current	All digital pins, logic level = ground	−95	−75		µA
	Turn-on switching time	Line-termination mode (bias 00) to G.Fast 212-MHz mode (bias 10)		64		ns
		Line-termination mode (bias Z0) to G.Fast 212-MHz mode (bias 10)		50		
		Power-down mode (bias ZZ) to G.Fast 212-MHz mode (bias 10)		60		
	Turn-off switching time	G.Fast 212-MHz mode (bias 10) to line-termination mode (bias 00)		76		ns
		G.Fast 212-MHz mode (bias 10) to line-termination mode (bias Z0)		400		
		G.Fast 212-MHz mode (bias 10) to power-down mode (bias ZZ)		380		

Product Folder Links: *THS6302*

6.7 Typical Characteristics

At T_A = 25 °C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100 Ω Load, R_{SERIES} = 47.5 Ω, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).
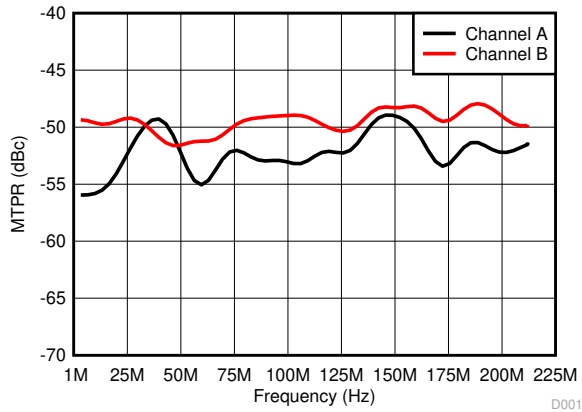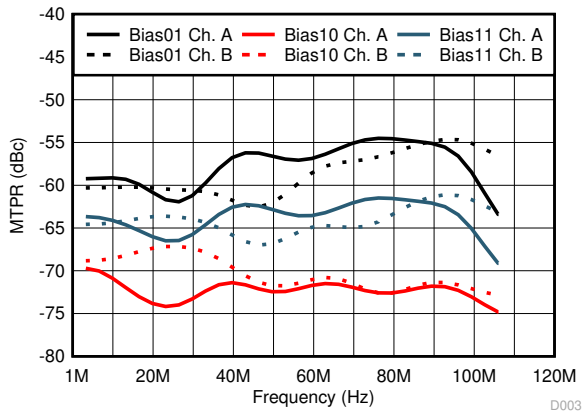
Line power = 8 dBm

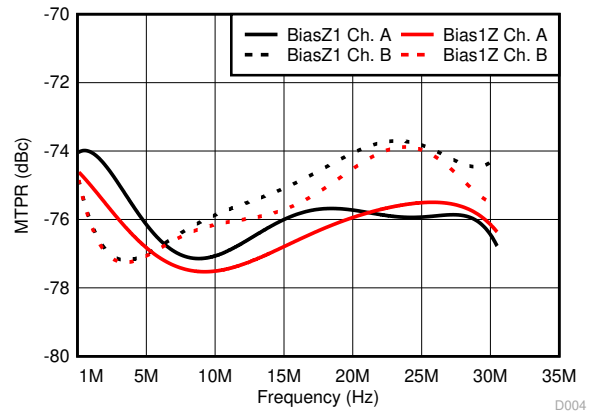**Figure 6-1. MTPR G.Fast 212-MHz Mode**
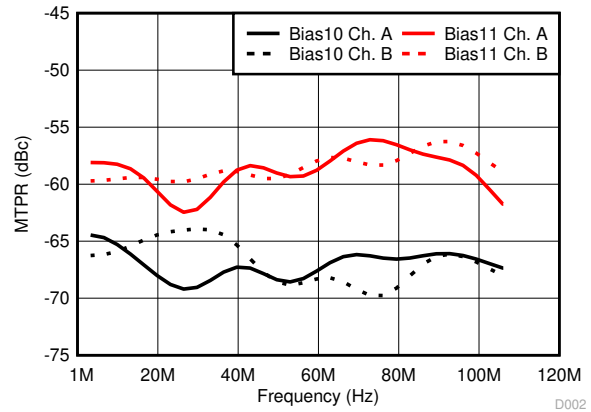
Line power = 8 dBm
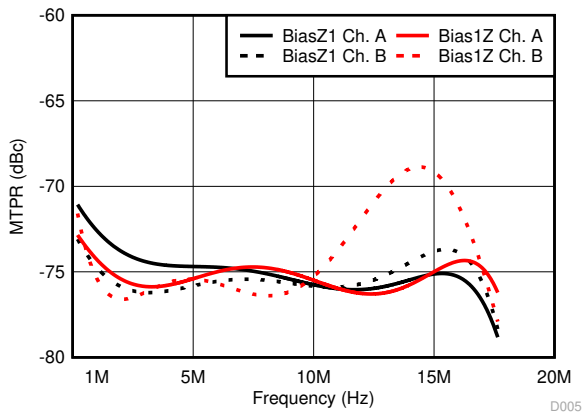
Figure 6-2. MTPR G.Fast 106-MHz Mode
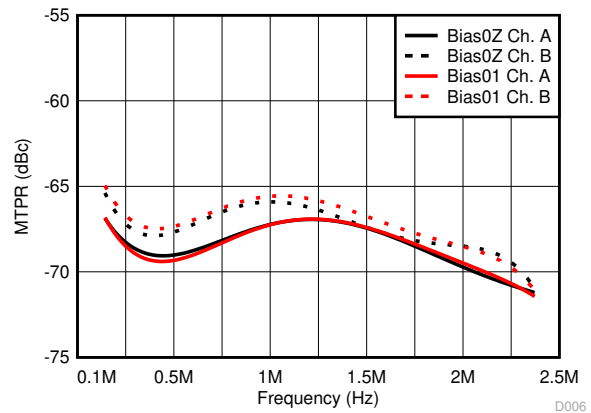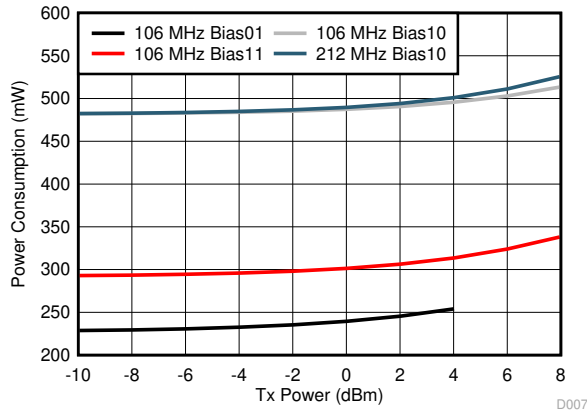
Line power = 4 dBm

Figure 6-3. MTPR G.Fast 106-MHz Mode

Line power = 8 dBm

Figure 6-4. MTPR VDSL-30a Mode

Line power = 8 dBm

Figure 6-5. MTPR VDSL-17a Mode

Line power = 8 dBm

Figure 6-6. MTPR ADSL2+ Mode

Product Folder Links: *THS6302*

6.7 Typical Characteristics (continued)

At T_A = 25 °C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100 Ω Load, R_{SERIES} = 47.5 Ω, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).

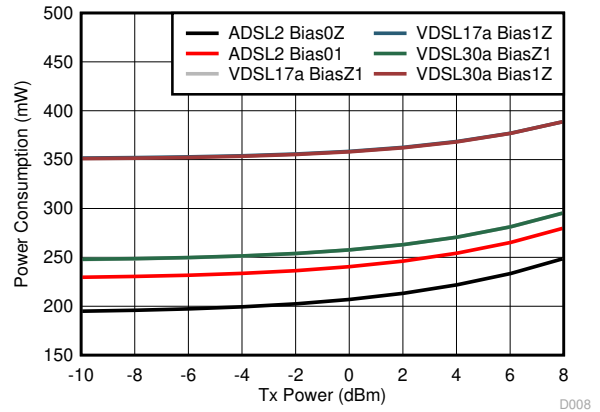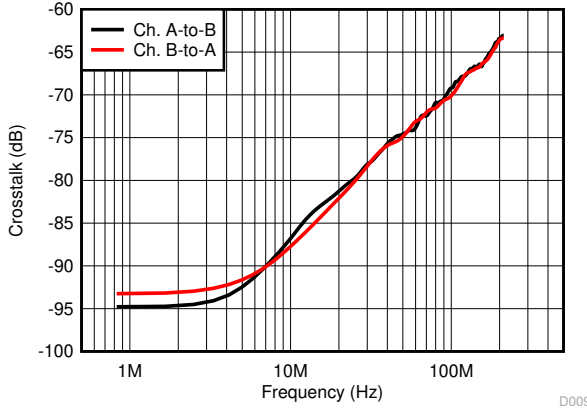Figure 6-7. G.Fast Modes Power Consumption

Figure 6-8. xDSL Modes Power Consumption
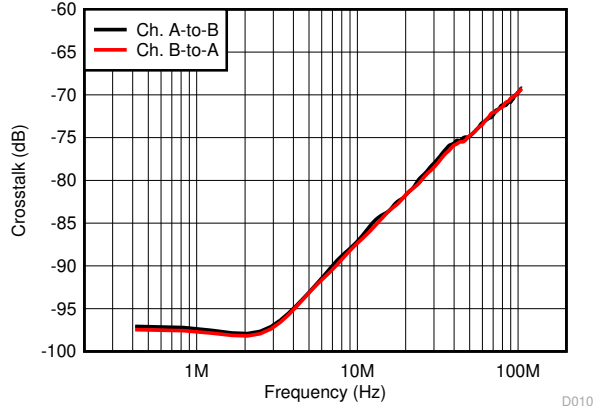

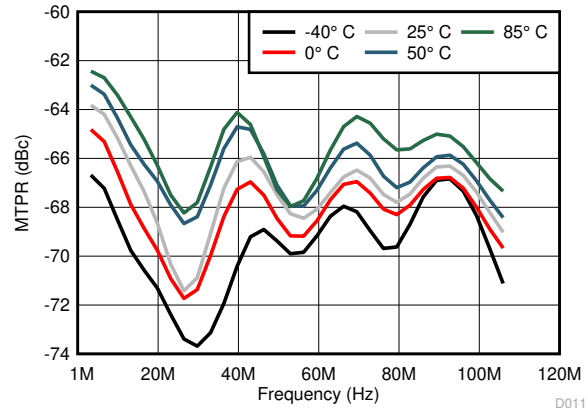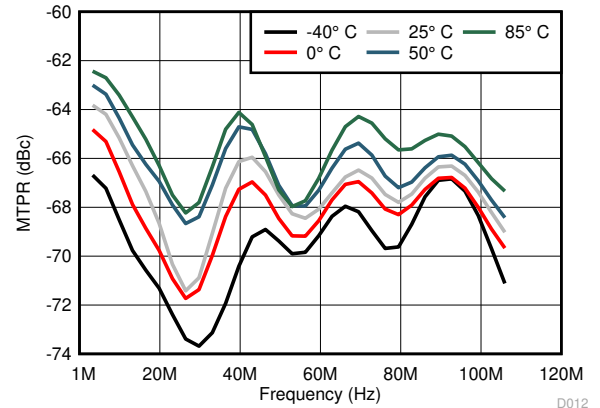Figure 6-9. Crosstalk G.Fast 212-MHz Mode

Figure 6-10. Crosstalk G.Fast 106-MHz Mode

G.Fast 106-MHz channel A, line power = 8 dBm

Figure 6-11. MTPR vs Temperature

G.Fast 106-MHz channel B, line power = 8 dBm

Figure 6-12. MTPR vs Temperature

Product Folder Links: THS6302

6.7 Typical Characteristics (continued)

At T_A = 25 °C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100 Ω Load, R_{SERIES} = 47.5 Ω, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).

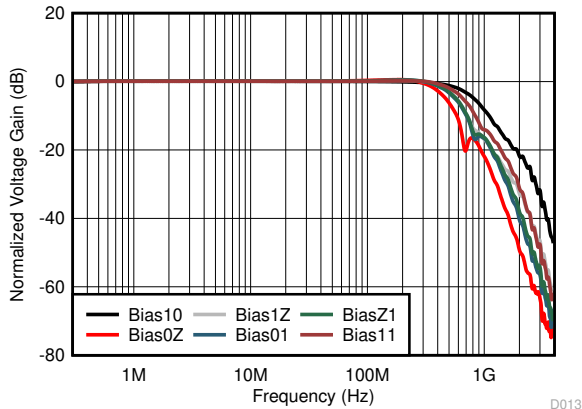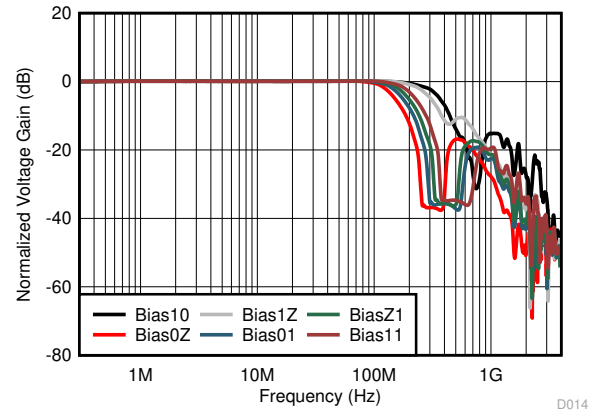**Figure 6-13. Normalized Small-Signal Frequency Response**

V_{OUT} = 13 V_{PP}

Figure 6-14. Normalized Large-Signal Frequency Response
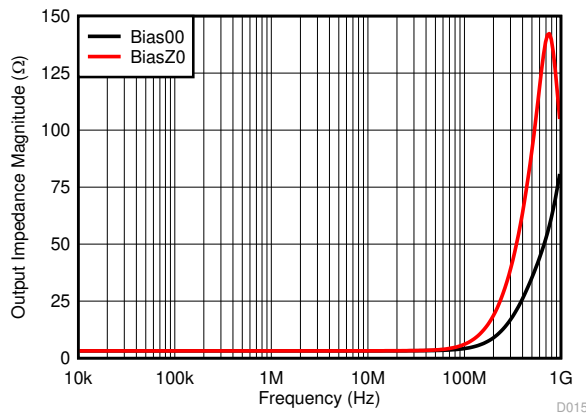
Figure 6-15. Terminal Modes Output Impedance
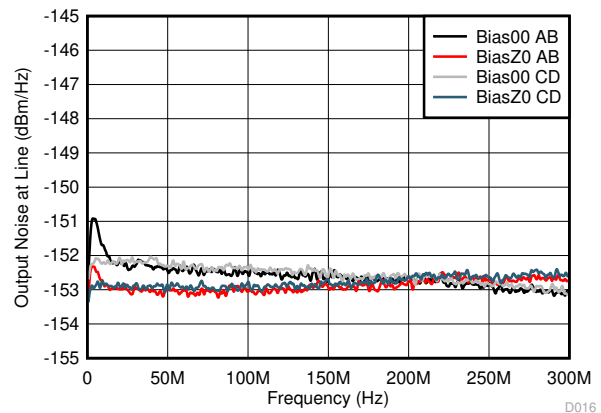
Figure 6-16. Terminal Modes Noise Floor

Full-scale input
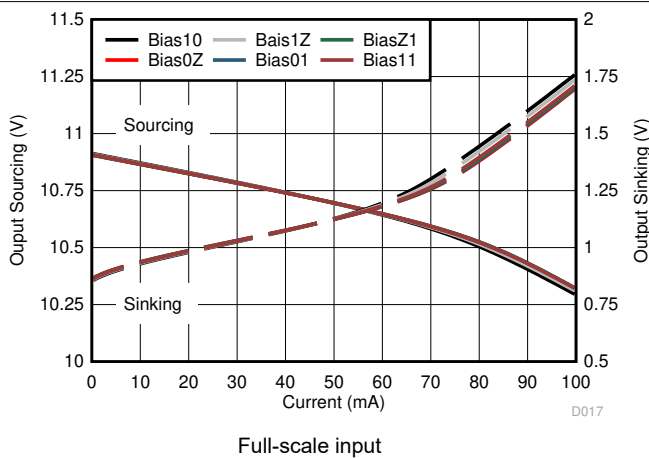
Figure 6-17. Output Voltage vs Current

Mid-scale input
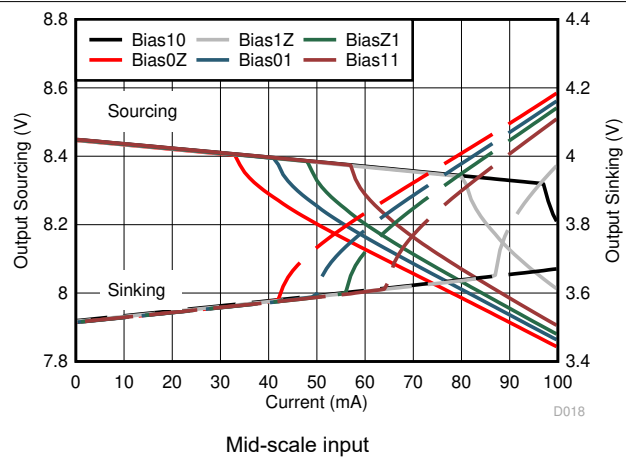
Figure 6-18. Output Voltage vs Current

Product Folder Links: *THS6302*

6.7 Typical Characteristics (continued)

At T_A = 25 °C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100 Ω Load, R_{SERIES} = 47.5 Ω, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).

Zero input

Figure 6-19. Output Voltage vs Current

Terminal modes
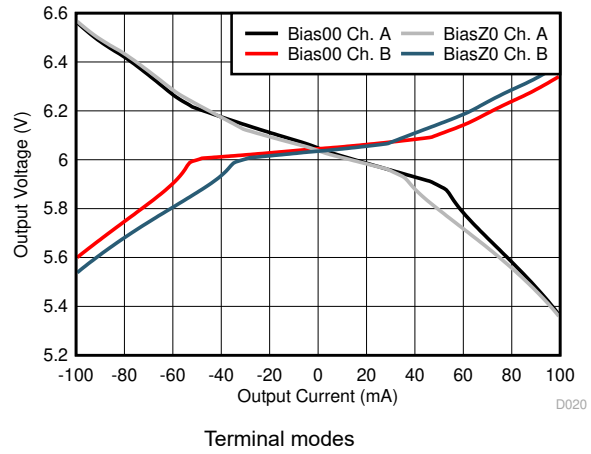
Figure 6-20. Output Voltage vs Current

Bias mode 00 to mode 10
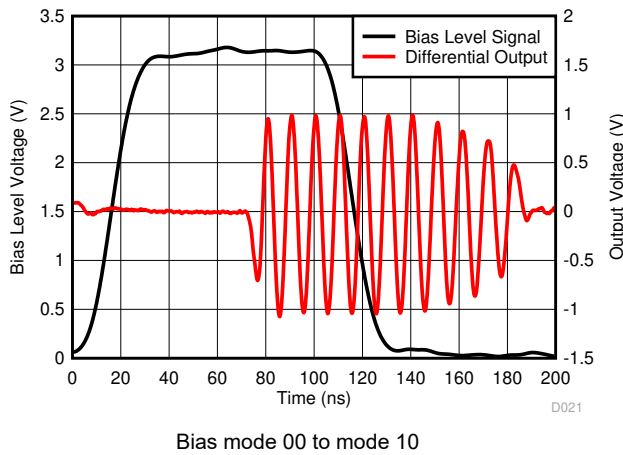
Figure 6-21. Mode Switching Time

Bias mode Z0 to mode 10
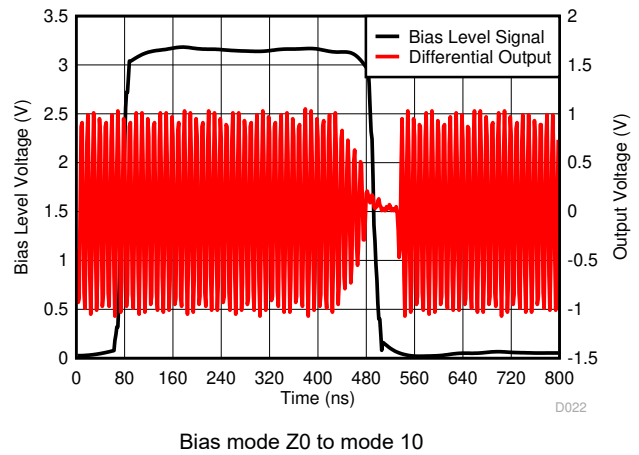
Figure 6-22. Mode Switching Time

Bias mode ZZ to mode 10
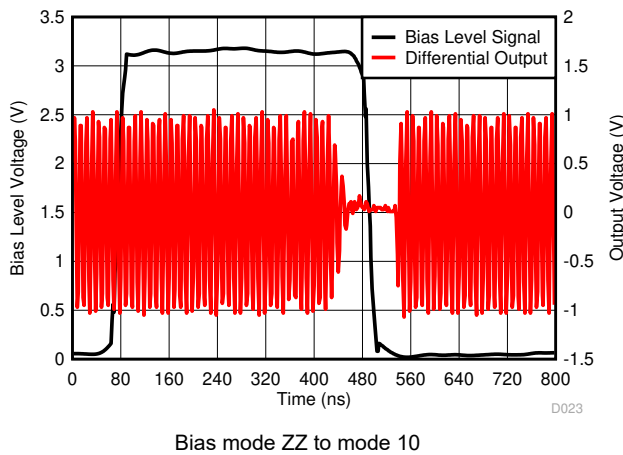
Figure 6-23. Mode Switching Time
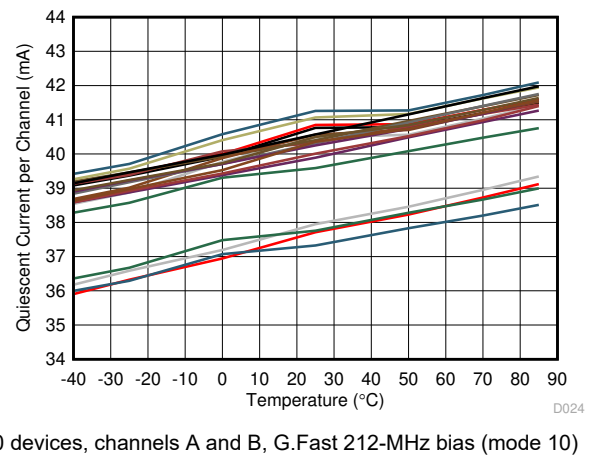
10 devices, channels A and B, G.Fast 212-MHz bias (mode 10)

Figure 6-24. Quiescent Current vs Temperature

Product Folder Links: THS6302

6.7 Typical Characteristics (continued)

At T_A = 25 °C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100 Ω Load, R_{SERIES} = 47.5 Ω, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).
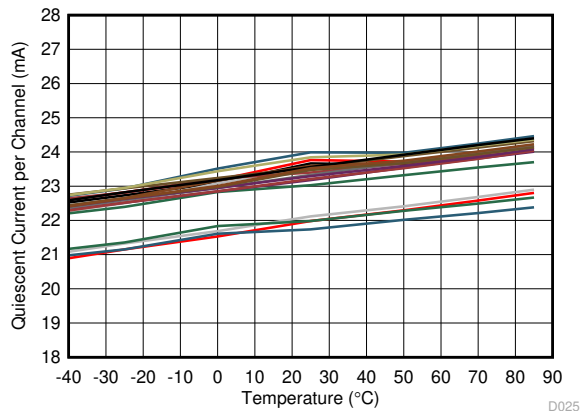
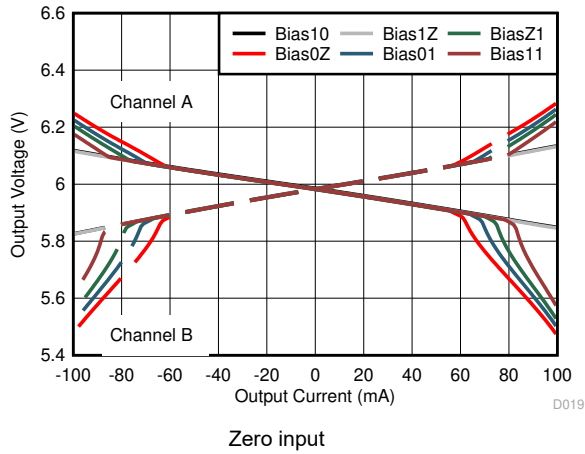10 devices, channels A and B, G.Fast 106-MHz bias (mode 11)

Figure 6-25. Quiescent Current vs Temperature
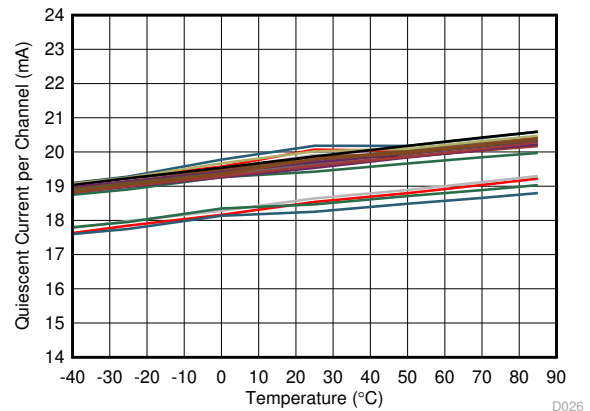
10 devices, channels A and B, VDSL bias (mode Z1)

Figure 6-26. Quiescent Current vs Temperature
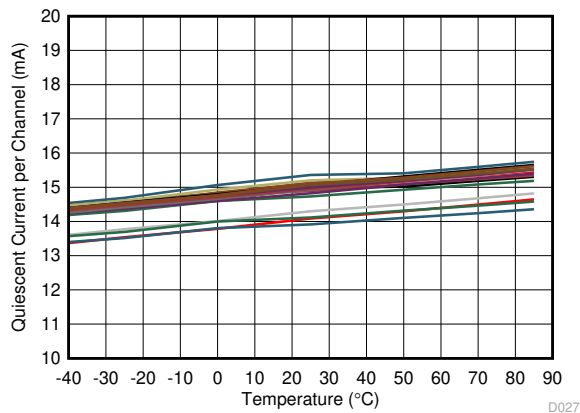
10 devices, channels A and B, ADSL bias (mode 0Z)

Figure 6-27. Quiescent Current vs Temperature
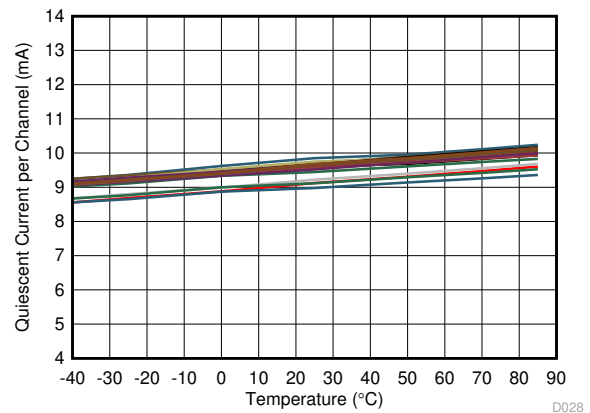
10 devices, channels A and B, line-termination high-power bias (mode 00)

Figure 6-28. Quiescent Current vs Temperature
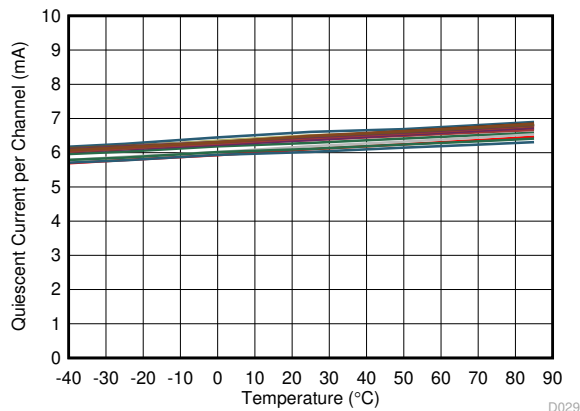
10 devices, channels A and B, line-termination low-power bias (mode Z0)

Figure 6-29. Quiescent Current vs Temperature
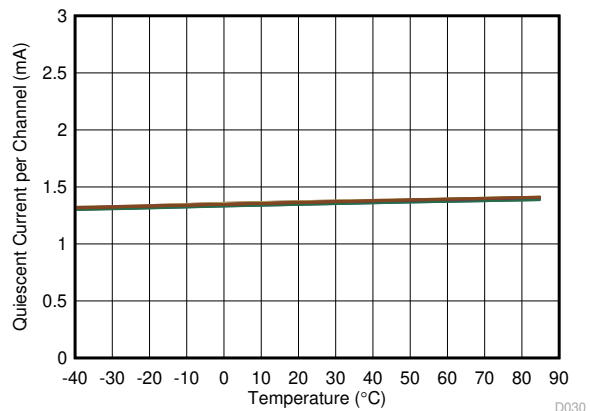
10 devices, channels A and B, power-down (mode ZZ)

Figure 6-30. Quiescent Current vs Temperature

Product Folder Links: *THS6302*

6.7 Typical Characteristics (continued)

At T_A = 25 °C, VS pin = 12 V, GND = 0 V, gain = 11 V/V, 100 Ω Load, R_{SERIES} = 47.5 Ω, PAR = 15 dB, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted).
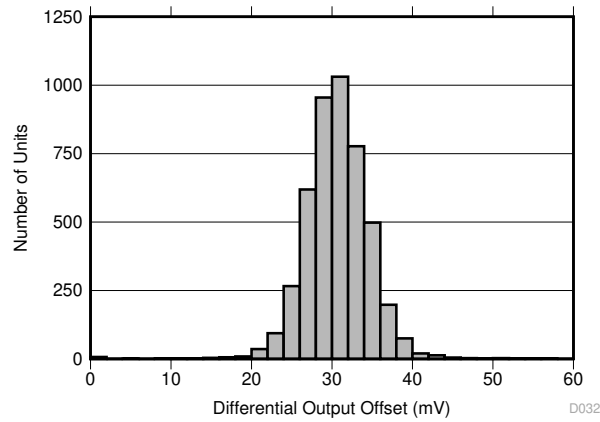
Figure 6-31. Output Offset Voltage

Product Folder Links: *THS6302*

7 Detailed Description

7.1 Overview

The THS6302 is a dual-port, current-feedback architecture, differential line driver designed for G.Fast and xDSL systems. The device is targeted for use in G.Fast digital subscriber line (DSL) systems that enable native discrete multitone modulation (DMT) signals and supports an 8-dBm line power up to 212 MHz with good linearity.

The device consists of a unique architecture consisting of two amplifiers per channel in a noninverting configuration with an internally-fixed gain of 11 V/V. The THS6302 is designed to drive the high-performance G.Fast 212-MHz DSL profile, but is also backwards-comparable to drive lower frequency profiles. The device features selectable bias modes for the G.Fast 106-MHz profile, VDSL profiles, and ADSL profiles. These modes reduce the quiescent current of the device based on the frequency requirements of the various DSL profiles to maximize power efficiency. Along with adjustable bias modes, the device features two line-termination modes that maintain an output impedance match with low power consumption. The line-termination modes allow for the device to be in a low-power state without causing distortion on a shared signal line.

For further flexibility, the THS6302 features an IREF pin that is used to further adjust the quiescent current of the device. A resistor connected to this pin can be changed to increase or decrease the device current to meet performance requirements and uses the lowest amount of power possible.

7.2 Functional Block Diagram
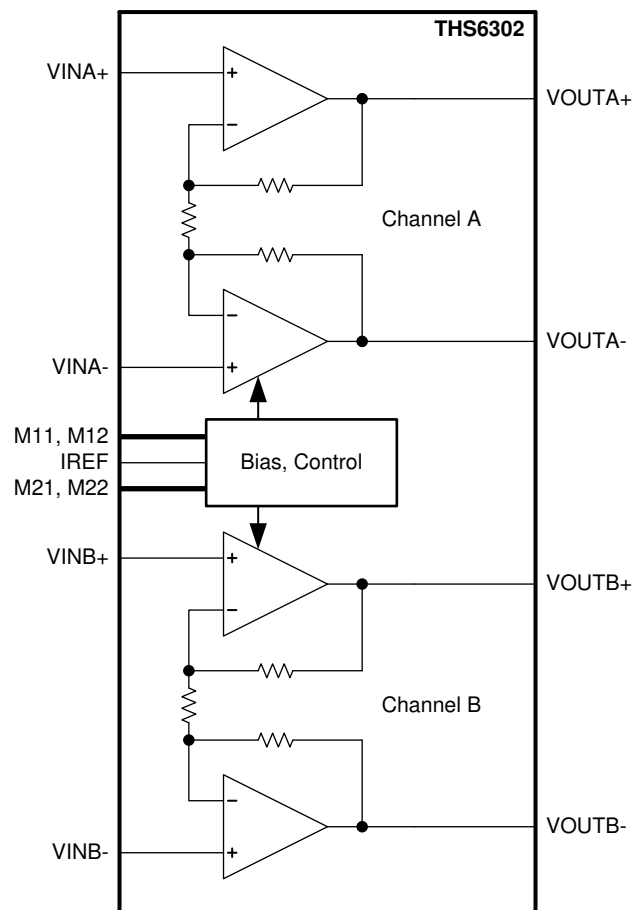
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7.3 Feature Description

The THS6302 is a dual-channel line driver that has a high current drive and a differential input and output amplifier in each channel. Figure 7-1 shows an example circuit for channel A of the THS6302 configured to drive the G.Fast 212-MHz DSL profile. The bias control pins (M12 and M11) are set to ground and 3.3 V, respectively, to put the device in the G.Fast 212-MHz bias mode. This bias optimizes the internal power consumption of the device to meet performance specifications of the G.Fast 212-MHz profile and can be changed to meet several different DSL profiles and other modes listed in Table 7-1. The IREF pin is biased with a 75-kΩ (R_{IREF}) resistor that adjusts the device quiescent current to a nominal state. R_{IREF} can be increased to lower the quiescent current or deceased to raise the quiescent current of the device for fine-tuning. C_{IREF} provides decoupling for the IREF pin and is typically 100 pF.

The THS6302 has a 10-kΩ, internally-set differential input impedance and low output impedance. In Figure 7-1 the input impedance is matched to 100 Ω by using a 100-Ω resistor connected differentially across the inputs. This value can easily be changed by using a different resistor to create the desired impedance at the input. Remember that the impedance in the device is actually the parallel combination of 10 kΩ and the external input resistor. For low impedances, this effect is minimal, but must be considered if the matched input impedance is increased. The output impedance of the THS6302 in Figure 7-1 is set by the two R_{SERIES} resistors to match 100 Ω. The internal output resistance is very low (< 2 Ω per output), so the output impedance is primarily set by the R_{SERIES} resistors. These resistors can be adjusted to match various output impedance values.
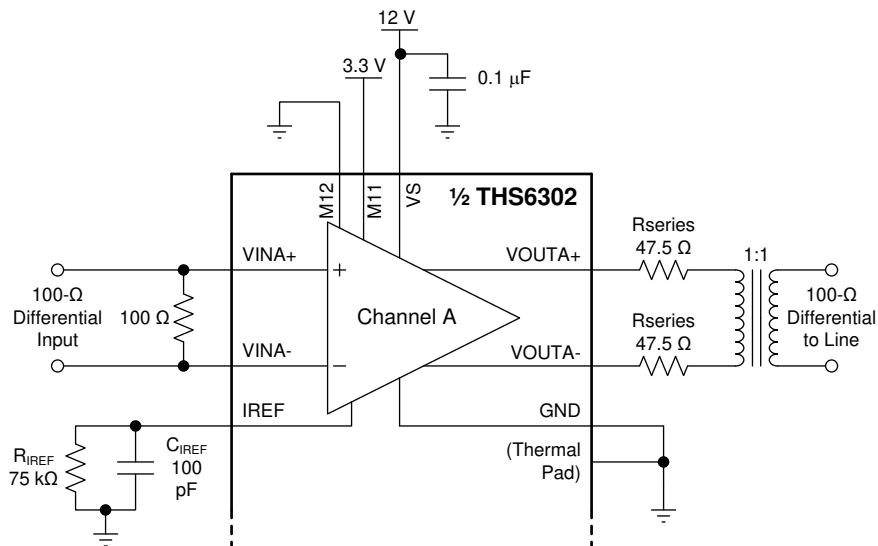
Copyright © 2016, Texas Instruments Incorporated

Figure 7-1. G.Fast 212-MHz Driving Mode Example Circuit

7.4 Device Functional Modes

The THS6302 features nine different device operational modes to accommodate the G.Fast, xDSL, line termination, and power-down scenarios, as listed in Table 7-1. Each channel of the device is controlled by a 2-pin parallel interface that uses three-level logic to control the device state. The G.Fast and xDSL modes change the quiescent current of the device to meet signal performance requirements and maintain the lowest power possible, which allows for legacy DSL compatibility with maximum power efficiency. The two line-termination modes maintain a low impedance at the output when placing the device in a low-power state. The line-termination modes allow for the muxing of multiple devices to one output line by putting the non-driving devices in a state that does not add distortion to the line. A power-down mode is also included to digitally shut down the device for the highest level of power savings. Table 7-1 lists the device power modes and the typical quiescent currents for each mode.

Product Folder Links: THS6302

7.5 Programming

The THS6302 programming is controlled by two pins for each channel. These pins use three-level logic to create nine different combinations for each pair of pins. The pins have a high state (*1*) when the pin voltage is greater than 2.3 V, a low state (*0*) when the pin voltage is less than 0.6 V, and an open state (*Z*) where the pin floats at approximately 1.4 V or can be driven between 1.2 V and 1.6 V. The pins are labeled Mxy where x is the channel number that the pin is associated with and y is the pin number. Table 7-1 shows the logic combinations for the two pins and the corresponding power modes.

Table 7-1. Bias Modes Truth Table

BIAS CONTROL PINS		BIAS MODE DESCRIPTION	TYPICAL QUIESCENT CURRENT
Mx1	Mx2		
0	0	Line termination, high power	9.5 mA
Z	0	Line termination, low power	6.3 mA
1	0	G.Fast 212 MHz	39 mA
0	Z	ADSL2+	14.5 mA
Z	Z	Power down	1.35 mA
1	Z	Alternate VDSL (high power)	28.0 mA
0	1	Alternate G.Fast 106 MHz (low power)	17.8 mA
Z	1	VDSL	19.5 mA
1	1	G.Fast 106 MHz	23.0 mA

8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

THS6302 is a dual-port, very-high-bit-rate linear xDSL, G.Fast, and G.mgFast differential line driver where the device drives a twisted pair cable. The signal is typically generated by a DAC in the DSL ASIC at low signal swings that is amplified by the G.Fast line driver.

The G.Fast system is ac-coupled when transmitting information above the audio band. On the input of the line driver, this ac-coupling translates into the series capacitors to isolate the dc voltage coming from the DAC output common-mode voltage. On the output, a transformer is used to help isolate the 48 V present between the tip and ring of the telephone line.

The transformer can be set to any useful ratio. In practice, the transformer-turn ratio is set between 1:1 and 1:1.4 for the device. Synthetic impedance at the output of the line driver is common in many xDSL applications. However, to support high AC performance needed for typical G.Fast and G.mgFast applications, THS6302 is an internally fixed-gain device and often synthetic impedance configuration is not recommed to maintain the AC performance.

Note: the resulting load detected by the amplifier may affect the amplifier linearity or output voltage swing capabilities.

8.2 Typical Application

Figure 8-1 shows a typical application circuit for THS6302. Only one channel circuit of THS6302 is shown; the other channel is often a duplicate of this channel in most applications.
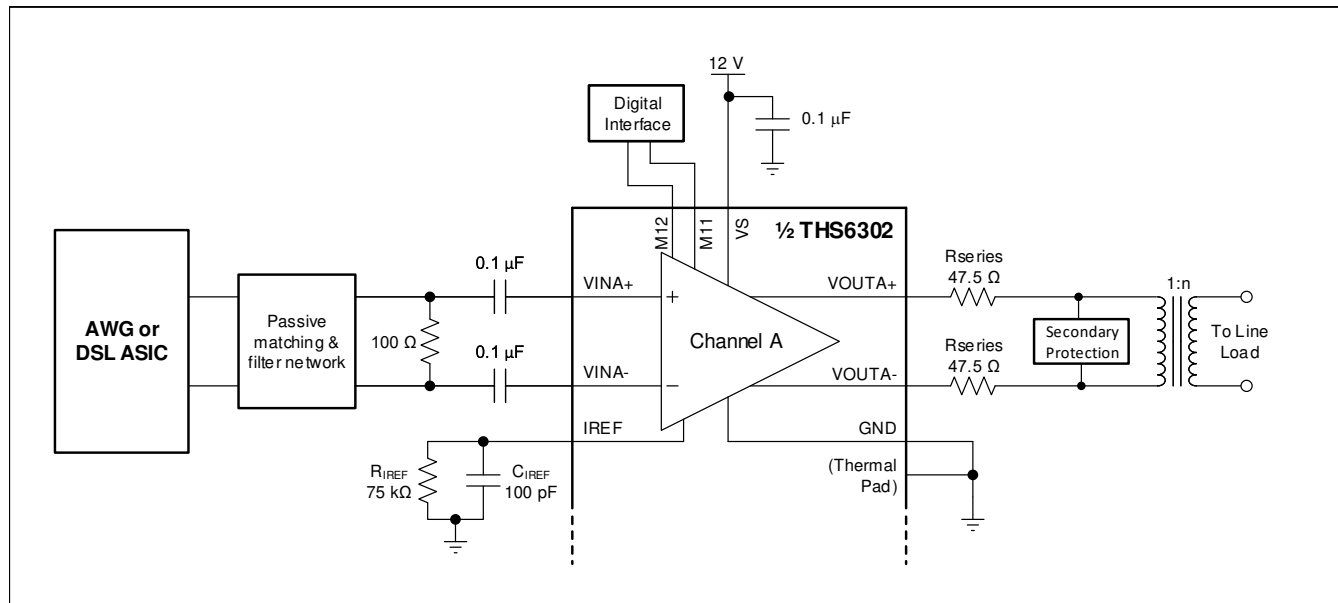

Figure 8-1. Typical G.Fast Line Driver Configuration

8.2.1 Design Requirements

Table 8-1 provides design requirements for a G.Fast line driver, which is met by the THS6302 device.

Table 8-1. Design Requirements

PARAMETER	CONDITION
G.Fast, 212-MHz and 106-MHz transmit profile	MTPR information using bias control for line power = 8 dBm and PAR = 15 dB
Legacy DSL profile support	Yes
Supply voltage	12 V
Input interface	AC coupled
Output transformer ratio	1:1
Surge protection	External as needed

8.2.2 Detailed Design Procedure

The G.Fast signal input to the THS6302 comes from a high-speed DAC in the DSL ASIC whose interleaving spurs are filtered out using either a 3rd- or 5th-order filter. Digital pre-emphasis can be employed in the DAC output such that the differential line driver compensates for the transmission line cable losses at long distance and high frequency. The THS6302 is operated on a 12-V single supply. Resulting from the single-supply operation, the device input is AC-coupled using a capacitor that blocks any DC current flowing out of the inputs to the adjacent circuitry. The AC-coupling capacitor forms a high-pass filter with the device input impedance. This pole must be set at a frequency low enough to not interfere with the desired xDSL or G.Fast signal.
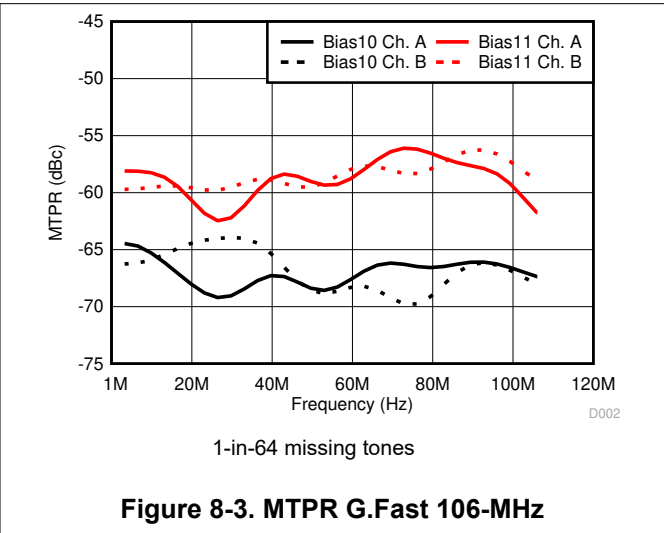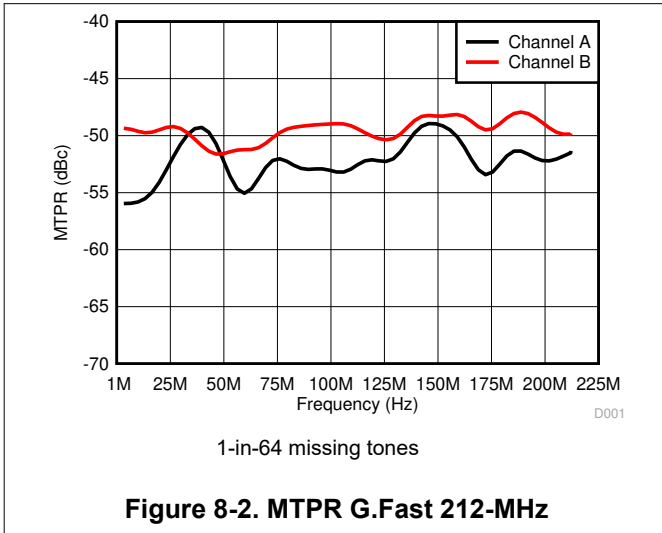
The THS6302 differential outputs usually drive a 1:n output transformer with a transformer turns ratio that can be changed depending upon the application. The output transformer selected must have low insertion loss in the desired frequency band in order to maintain good multi-tone power rejection (MTPR) for a given line power. The load is expected to be a transmission line with 100-Ω characteristic impedance on the primary side (line load side) of the transformer. Referred to the transformer secondary, the load seen by the amplifier is $1/n^2$ with 1:n being the transformer turn ratio. Practical limitations force the transformer-turn ratio to be between 1:1 and 1:1.6. At the lighter load seen by the amplifier (1:1), the voltage swing is limited by the class AB output stage and the maximum achievable swing of the amplifier. At the heaviest load (1:1.6), the voltage swing is limited by the current drive capability of the amplifier.

For surge protection, consider adding a gas discharge tube (GDT) on the primary side of the output transformer. The gas discharge tube is required to shunt the large current that could flow through the cables during lightning surge, and protect the device outputs. The secondary protection is also normally added after the series resistance on the secondary transformer side. The secondary protection could be in the form of back to back switching diodes, which also help limit the residual surge current flowing into the device outputs.

For the power-supply bypass, consider using X7R or X5R because of the better stability of these materials over temperature.

Product Folder Links: *THS6302*

8.2.3 Application Performance Plots

Figure 8-2 and Figure 8-3 show the MTPR results for 212-MHz and 106-MHz G.Fast profiles, respectivley.

1-in-64 missing tones

Figure 8-2. MTPR G.Fast 212-MHz

1-in-64 missing tones

Figure 8-3. MTPR G.Fast 106-MHz

9 Power Supply Recommendations

The THS6302 is recommended to operate using a total supply voltage of 12 V. If a lower or higher supply voltage is required, select one that is between 11.4 V and 12.6 V for optimal performance. Use supply decoupling capacitors on the power-supply pins to minimize distortion caused by parasitic signals on the power supply. This usage is especially important in applications where many devices share a single power-supply bus.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6302 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Excessive parasitic capacitance on the input pin can cause instability. In the line driver application, the parasitic capacitance forms a pole with the load detected by the amplifier and can reduce the effective bandwidth of the application circuit, thus leading to degraded performance. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

2. Minimize the distance (< 0.25 in.) from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors.

3. Careful selection and placement of external components preserves the high-frequency performance of the device. Use very-low reactance-type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and printed circuit board traces as short as possible. Never use wire-wound type resistors in a high-frequency application.

4. Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.

5. Do not socket a high-speed part such as the THS6302. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the device onto the board.
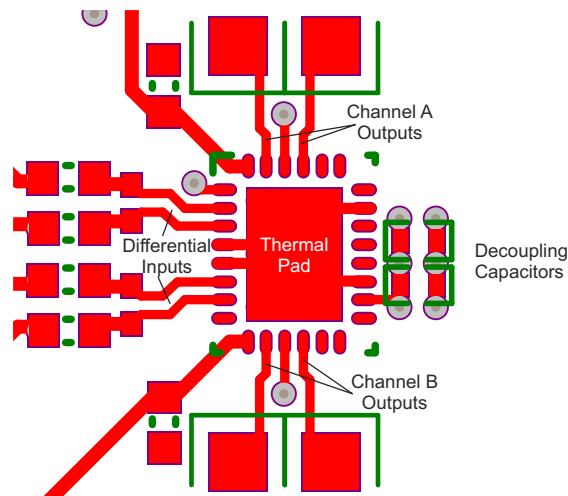
10.2 Layout Example

Figure 10-1. Example Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6302IRHFR	ACTIVE	VQFN	RHF	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6302 IRHF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6302IRHFR	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6302IRHFR	VQFN	RHF	28	3000	367.0	367.0	35.0
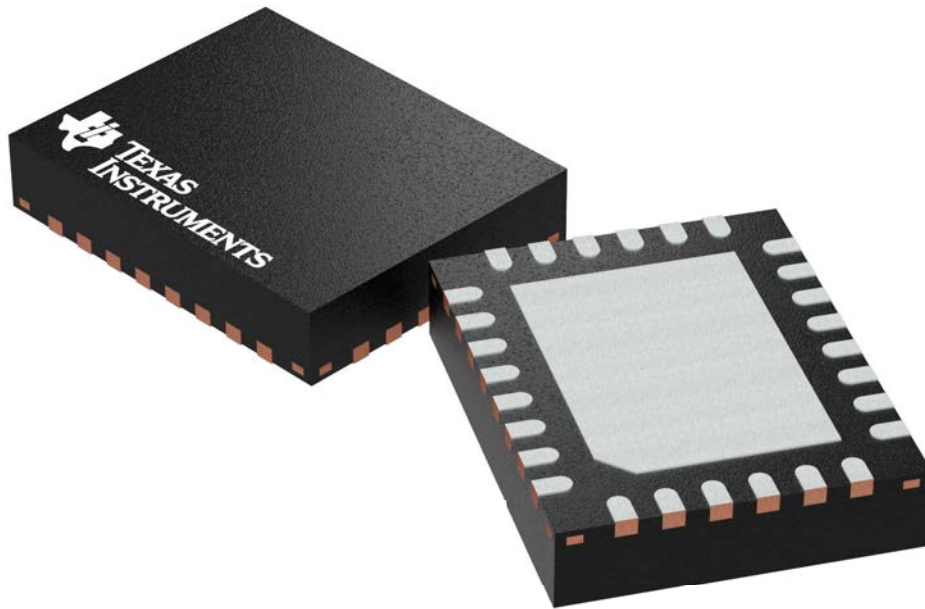
Images above are just a representation of the package family, actual package may vary.
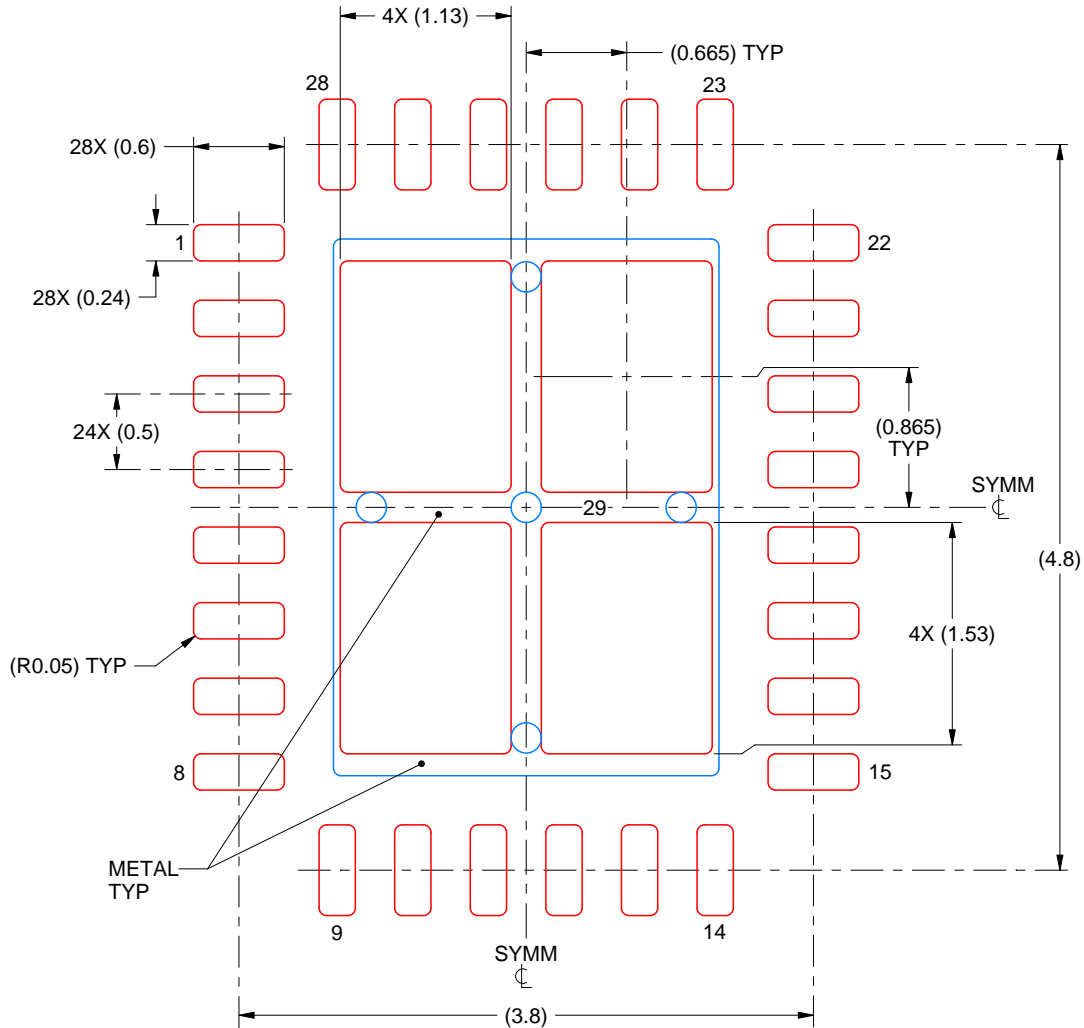Refer to the product data sheet for package details.

4204845/J

TEXAS
INSTRUMENTS

A

4.1
3.9

B

PIN 1 INDEX AREA

5.1
4.9

0.5
0.3

0.30
0.18

DETAIL
OPTIONAL TERMINAL
TYPICAL

1 MAX

0.05
0.00

C

SEATING PLANE

$\bigcirc$ | 0.08 | C

2.55 ± 0.1

2X | 2.5

9   14

EXPOSED
THERMAL PAD

24X | 0.5

8   15

(0.2) TYP

2X
3.5

29

3.55 ± 0.1

SYMM ℄

SEE TERMINAL
DETAIL

1   22

28X | 0.30
      0.18

PIN 1 ID
(OPTIONAL)

28   23

$\oplus$ | 0.1 Ⓜ | C | A | B
         0.05 Ⓜ

SYMM ℄

28X | 0.5
      0.3

4220383/A   11/2016
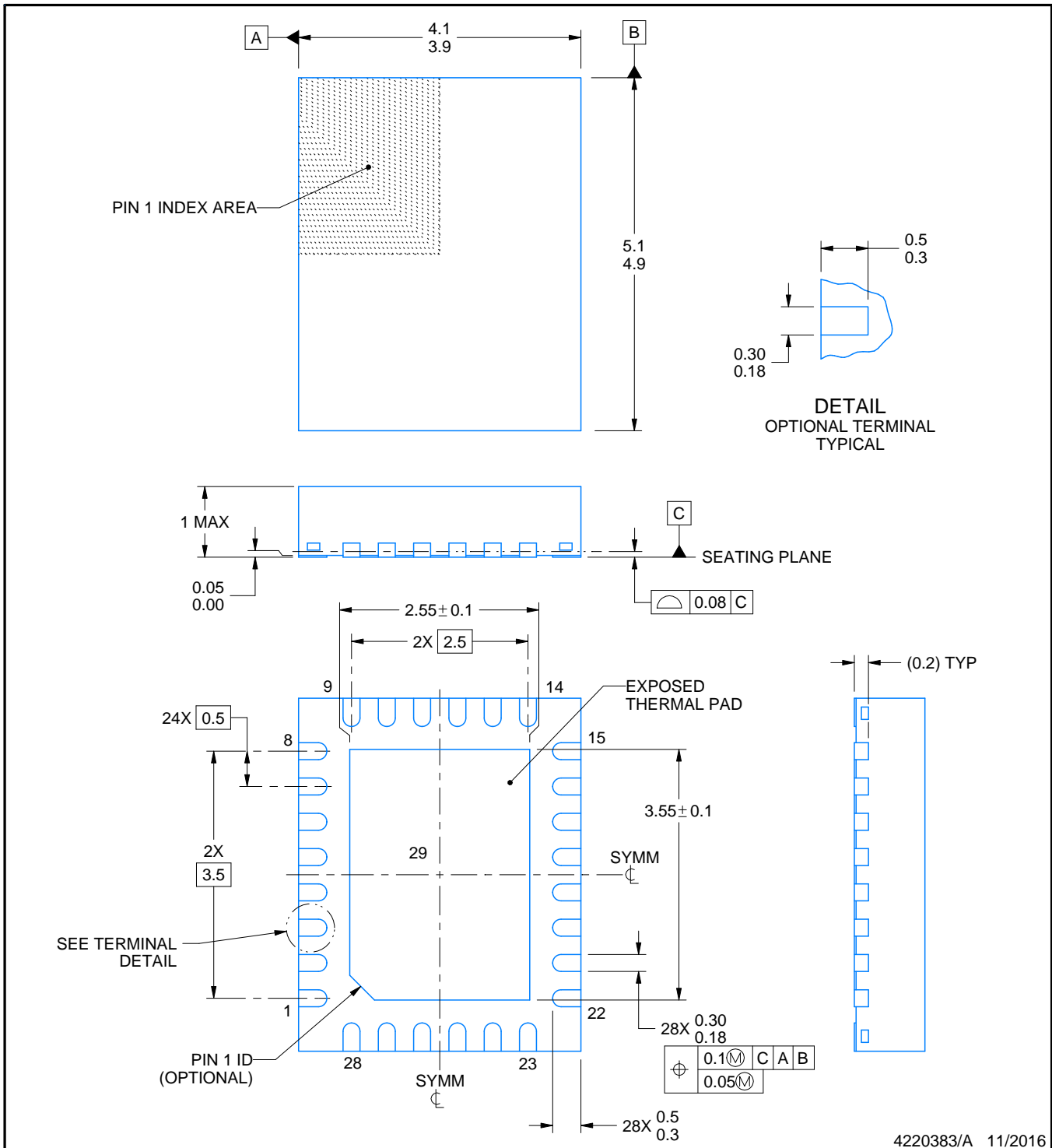
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

RHF0028A

(2.55)

SYMM

28

23

28X (0.6)

1

28X (0.24)

24X (0.5)

29

22

(1.525)

(3.55)

SYMM

(4.8)

(∅ 0.2) TYP
VIA

8

15

(R0.05)
TYP

9

14

(1.025)

(3.8)

LAND PATTERN EXAMPLE
SCALE:18X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220383/A   11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4220383/A   11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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