Interfacing the TLC5510 Analog to Digital Converter to the TMS320C203 DSP

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Interfacing the TLC5510 Analog to Digital Converter to the TMS320C203 DSP

Abstract

This application report presents guidelines for interfacing the Texas Instruments (TI™) TLC5510 8-bit parallel-output analog-to-digital converter (ADC) to the TI TMS320C203 DSP data bus. The 8-bit ADC operates at a rate of 20 MHz. The C callable application program (assembly code) used to initialize the TMS320C203 and execute the code is also discussed.

This report serves as reference information for further development of hardware and software. The contents include hardware schematics and associated program software, block and timing diagrams, and a program flow chart.

Product Support

Related Documentation

The following list specifies product names, part numbers, and literature numbers of reference documents:

- *TMS320C2xx User's Guide*, Literature number SPRU127B
- *TMS3200C1x/C2x/C2xx/C5x Assembly Language Tools, User's Guide*, Literature number SPRU018D
- *TI C2xx Development System User's Manual*, from Wyle Electronics, http://www.wyle.com
- TLC5540/TLC5510 Evaluation Module, Literature number SLAU007
- Texas Instruments, Data Book: *Data Acquisition Circuits, Data Conversion, and DSP Analog Conversion Interface*, Literature number SLAD001
- Texas Instruments, Data Sheet: *TLC5510, TLC5510A 8-Bit High-Speed Analog-to-Digital Converters*, Literature number SLAS095I
- Texas Instruments, Data Sheet: *74AC11004 Hex Converter*, Literature number SCAS033B
- Texas Instruments, Data Sheet: *TMS320C203, TMS320C209, TMS320LC203 Digital Signal Processors*, Literature number SPRS025
- Texas Instruments, Data Sheet: *74AHCT1G04 Single Inverter Gate*, Literature number SCLS319E
- Texas Instruments, Data Sheet: *74AHC1G32 Single 2-Input Positive-OR Gate*, Literature number SCLS317G

World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Introduction

The TLC5510 ADC translates the analog input signal into a binary digital form for data processing. Generally, parallel ADCs are used for high-speed applications, for example, video frequencies (>5 MHz). However, there is often a trade off between the converter maximum sampling frequency and its resolution. High-speed untrimmed ADCs used for video and higher frequencies have resolutions from 6 to 10 bits. The devices are usually designed with modified flash architectures producing the most cost-effective device solution for fabrication.

This application report focuses on the hardware interface and assembly code implementation. First, the TLC5510 Evaluation Module (EVM) is reviewed. A detailed discussion of the TMS320C203 Development Module (DVM) interface to the TLC5510 EVM follows. Finally, an overview of the software is presented.

Figure 1 shows a cost-effective solution consisting of a fixed point TMS320C203 DSP device, a TLC5510 ADC, and control logic circuits to access the data bus.

Figure 1. TLC5510 to TMS320C203 Interface Block Diagram

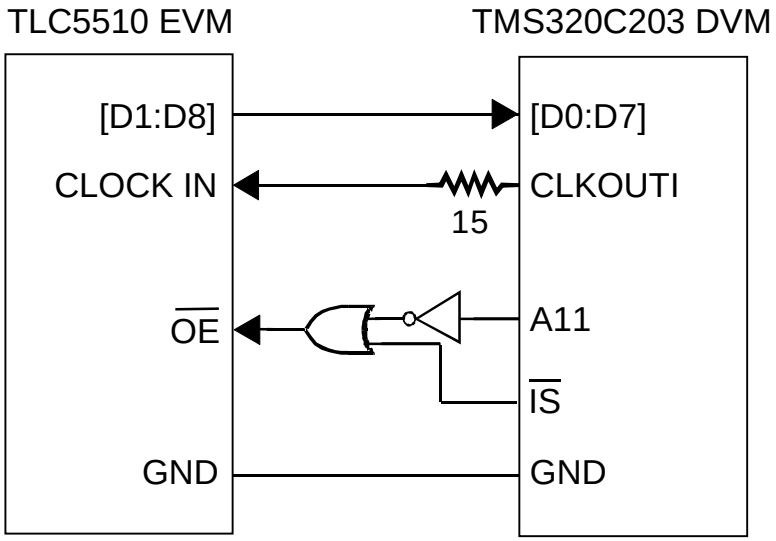
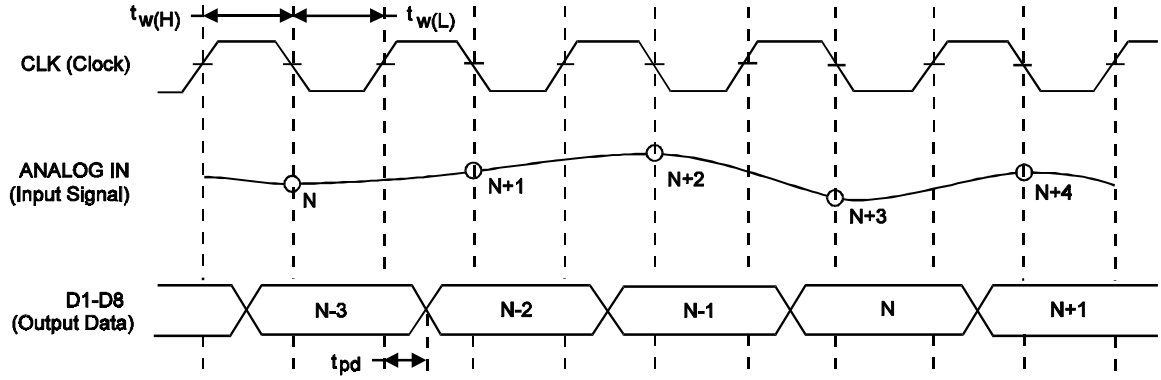


Figure 2 shows the idealized TLC5510 I/O timing waveforms.

Figure 2. TLC5510 I/O Timing Diagram



The digital data is valid after a delay time t_{pd} = 30 ns for the TLC5510. Table 1 summarizes important TLC5510 parameters.

Table 1. TLC5510 Parameters

Parameter			MIN	NOM	MAX	UNIT
Pulse duration, clock high, $t_{W(H)}$			25			ns
Pulse duration, clock low, $t_{W(L)}$			25			ns
Parameter		**Test Conditions**				
f_{conv}	Maximum conversion rate	$V_{I(ANLG)}$ = 0.5 V – 2.5 V	20			MSPS
BW	Analog input bandwidth	At –1 dB		14		MHz
		At –3 dB		23		MHz
t_{dd}	Delay time, digital output	$C_L \leq 10$ pF		18	30	ns

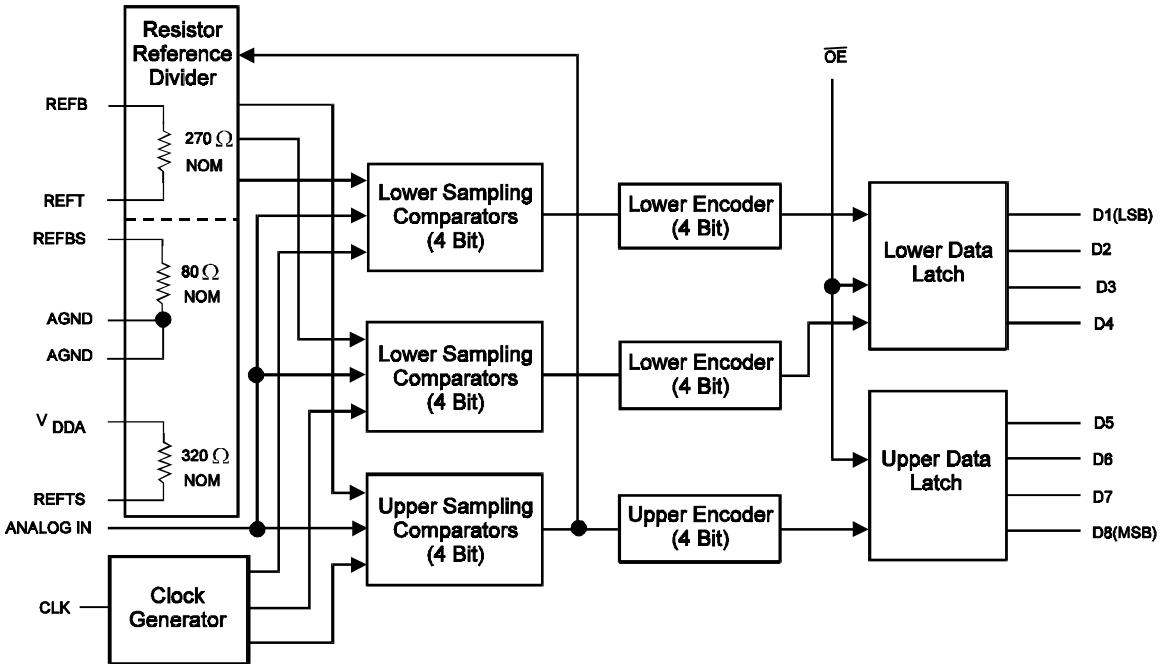
Note: The following conditions apply: V_{DD} = 5 V, V_{RT} = 2.5 V, V_{RB} = 0.5 V, f_s = 20 MSPS, T_A = 25°C

TLC5510 ADC Overview

The TLC5510 is a CMOS, 8-bit, 20 MSPS (mega samples per second) ADC utilizing a semi-flash architecture. The TLC5510 ADC includes internal reference resistors, a sample and hold circuit, and 8-bit parallel outputs with high impedance mode. The ADC typically consumes 128 mW of power and operates with a single 5 V supply.

Figure 3 shows the TLC5510 ADC block diagram and the input and output signals.

Figure 3. TLC5510 Functional Block Diagram

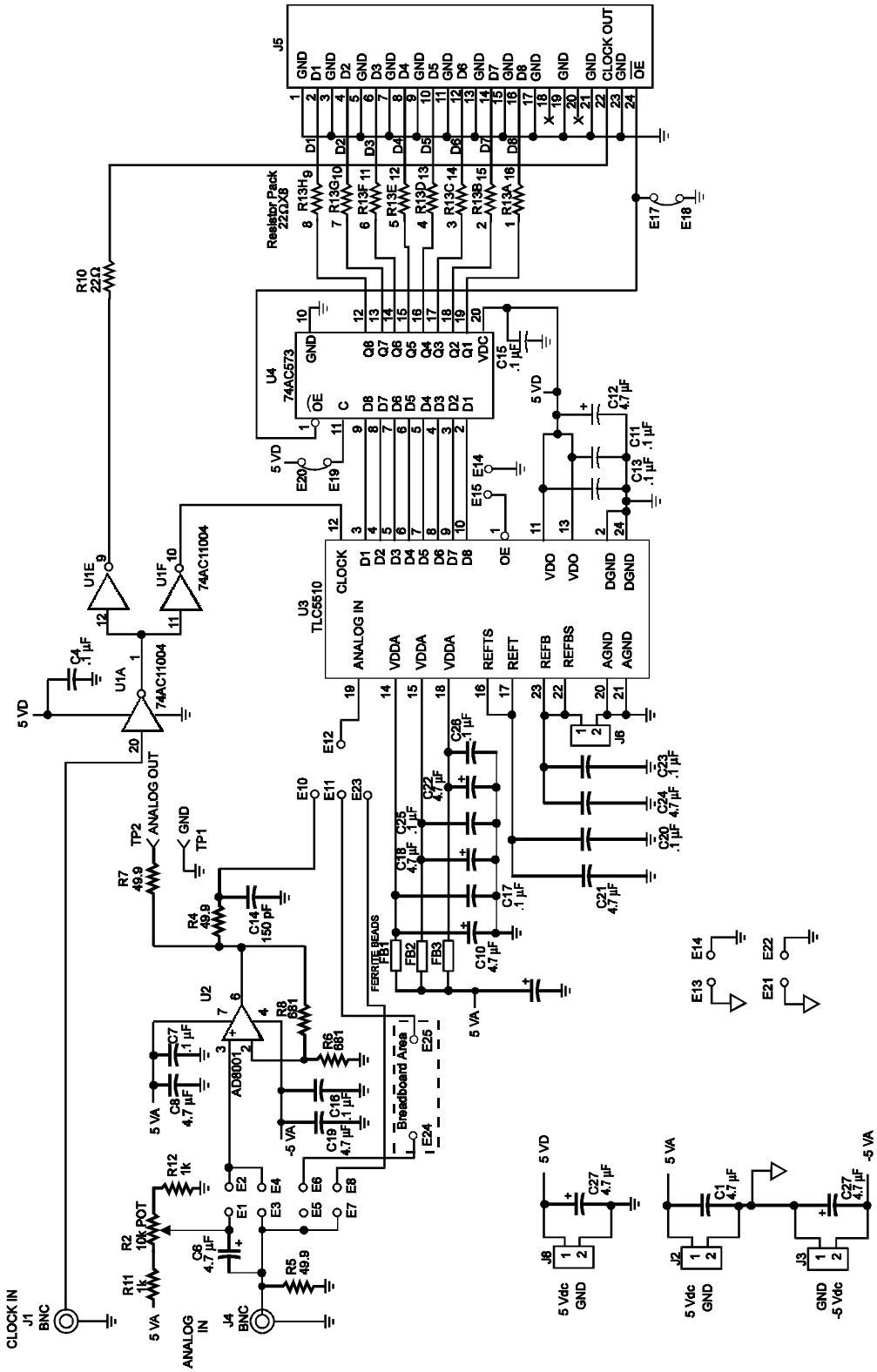


TLC5510 EVM

The Texas Instruments TLC5510 evaluation module (EVM) is designed specifically for the development of hardware utilizing the 8-bit high-speed low cost TLC5510 ADC.

The ADC is capable of 20 MSPS with an error of just ½ LSB and typical analog input bandwidth >14 MHz. Above 1 or 2 MHz sampling rate, the board layout is critical to the performance of the ADC and requires careful consideration of several issues. Therefore, using a breadboard for an ADC evaluation is no longer a suitable method. Figure 4 shows the TLC5510 EVM board schematic.

Figure 4. TLC5510 EVM Circuit Diagram



Supply Voltages

For best performance, the TLC5510 EVM board must be provided with the following three (3) separate voltages:

- Analog +5V
- Analog -5V
- Digital +5V

Table 2 details the jumpers and applications for the supply voltages.

Table 2. TLC5510 Supply Voltages

Voltage	Jumper	Application
+5V	J2	Analog supply voltage and +ve supply of the input op amp
-5V	J3	-ve supply voltage of the input op amp
+5V	J8	Digital logic supply voltage

The TLC5510 EVM board has a common analog ground area (0 V) for the analog +/- 5V supply voltages. The digital ground area for the digital supply voltage is isolated from analog ground to prevent noise spikes from the digital logic from influencing the analog circuits on the board.

The analog and digital grounds can be connected together by making a connection from E21 to E22 or E13 to E14 (see Figure 4). With this arrangement, it is possible to create and evaluate alternative methods of grounding.

Analog Input

Interfacing to the TLC5510 EVM with an analog signal source is simple because the analog input signal is taken via the BNC connector J4. This signal is taken to the input of the TLC5510 via one of four (4) alternative routes:

- Direct
- Via the amplifier input with DC coupling
- Via the amplifier input with AC coupling
- User-defined input

Direct Input

The input signal can be directly fed to the ANALOG IN pin of the TLC5510 device by jumpering E7 to E8 and E23 to E12. In the circuit shown in Figure 4, the reference voltage for the TLC5510 ADC is generated by the device internal resistors. If the jumper J6 is inserted, the reference voltage will be 2.28 V with respect to 0 V; otherwise, it will be 2.6 V with respect to 0.6 V.

DC Coupled Amplifier Input

The TLC5510 EVM board input stage uses an AD8001 operational amplifier. With a gain of +2, the amplifier –3dB bandwidth is 400 MHz. This op amp is suitable for driving the ADC because it has low distortion and fast settling time.

The amplifier gain is set to +2 by resistor R6 and R8. Removing R6 sets the gain to +1 (unity gain). The AD8001 is a current feedback transimpedance amplifier device. The non-inverting input is at high impedance and the inverting input is at low impedance; hence, there is a good possibility that the device will oscillate when R6 is removed from the circuit. To avoid oscillation at unity gain (+1), R8 must be retained in the circuit and its value changed to 953 Ω.

Capacitor C14 and resistor R4 are used for antialiasing low-pass filtering of the op amp output. Frequencies above 10 MHz (fs/2) are filtered out when C14 = 150 pF and R4 = 49.9 Ω.

Having resistor R4 in series with the output of the op amp helps reduce the capacitive loading at the output. Resistor R7 prevents capacitive loading at the test point TP2 by an oscilloscope probe used for making measurements.

The AD8001 output is connected to the ANALOG IN pin of the TLC5510 by a jumper wire connecting E10 to E12. The amplifier input can be DC or AC coupled to the input at J4. Table 3 lists the connections needed for these options.

Table 3. DC and AC Coupling Connections to J4 Input

Input Coupling	Jumper Connection
DC	E3 to E4
AC	E1 to E2

AC Coupled Amplifier Input

For an AC coupled input signal, resistor R2 provides voltage offset. The offset voltage range is 0 V to +5 V (analog). With an amplifier gain of +2, the positive dynamic output range of the op amp is reached with an offset value of 2.5 V.

The cutoff frequency of the input low-pass filter is set by C6 (4.7 uF) and resistance value set by potentiometer R2.

TLC5510 Analog Input Range

The permissible analog-input voltage range of the TLC5510 depends on jumper J6 settings. The way in which the jumper configuration affects the voltage conversion range is illustrated in Table 4. For example, when jumper J6 is inserted, analog inputs $\geq$ 2.28 V produces all 1s at the ADC output, and $\leq$ 0 V analog input produce all 0s at the converter output.

Table 4. Jumper Configuration and Voltage Conversion Range

Jumper J6	Input Voltage Range
Not inserted	0.6V to 2.6V
Inserted	0V to 2.28V

See the Texas Instruments data sheet, *TLC5510, TLC5510A 8-Bit High-Speed Analog-to-Digital Converters*, for information about other voltage settings.

Test Points

The analog output voltage of the AD8001 op amp is measured at test points TP1 and TP2 (see Figure 4). Table 5 lists the signals monitored by each test point.

Table 5. Signals Monitored by Test Points

Test Point	Signal
TP1	Analog ground
TP2	Output of the op amp

Input Defined by the User

If it is necessary to bypass the AD8001 op amp and directly feed the analog input signal into the TLC5510 ADC, jumper E7 to E8 and jumper E23 to E12 need to be inserted.

ADC Digital Data Output

The digital data of the TLC5510 ADC is buffered by an octal D-type latch (SN74AC573). A 22 Ω resistor is placed in series with Q1 through Q8 outputs to minimize ringing. The individual data lines are taken to the connection strip J5. The $\overline{OE}$ pin of the SN74AC573 latch controls the interface access to the TMS320C203 data bus.

The jumper between E17 and E18 must be removed and the outputs of SN74AC573 controlled by means of J5-24 on the connecting strip (see Figure 4). The outputs are then only active when the DSP addresses the ADC during data access.

Clock Buffer Circuit

The maximum conversion rate of the TLC5510 ADC is 20 MHz. The 20 MHz clock signal is fed in via the BNC input J1. It is buffered by two (2) 74AC11004 inverters before it is applied to both the clock pin of the TLC5510 and J5-22.

TLC5510 EVM to TMS320C203 DVM Interfacing Signals

An outline schematic of the TLC5510 EVM interface to the Wyle TI TMS320C203 DVM is shown in Figure 6. The TMS320C203 DVM is a standalone board carrying a TMS320C203PZ DSP, analog interface circuit (AIC), flash memory, SRAM, and serial interface for communication with a PC via the serial COM port.

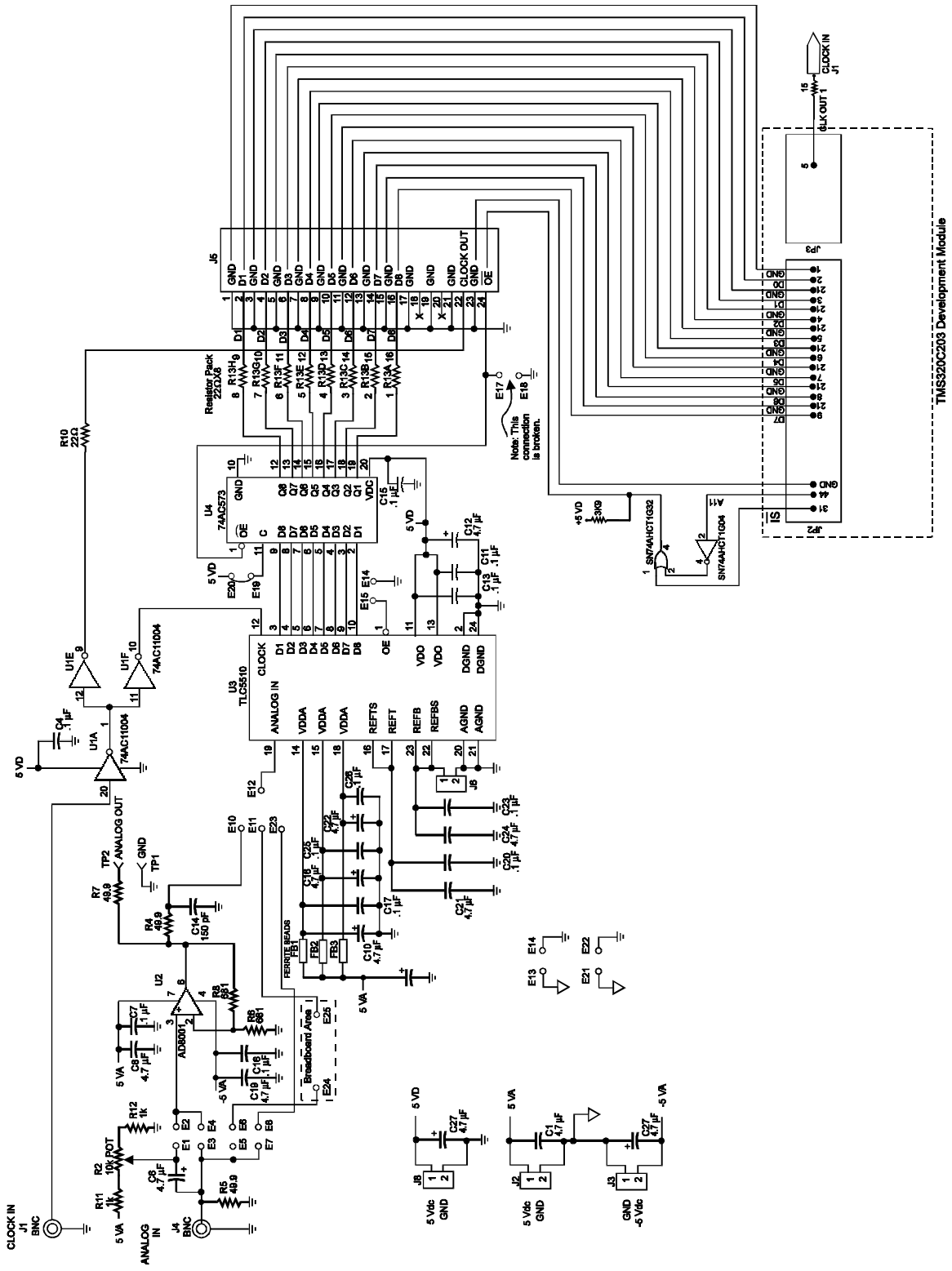
The fixed point TMS320C203PZ has an instruction cycle time of 50 ns and is optimized for the efficient implementation of digital signal processing algorithms. Referring to Figure 6, the data bus, D1 – D8, is connected via the data bus driver SN74AC573 (J5 pins 2,4,6,8,10,12,14, and 16) through a short ribbon cable to the TMS320C203 DSP data bus lines (D0 – D7).

To prevent bus contention, the SN74AC573 device must only be in an active state when data is being read from the ADC.

Each time the DSP wishes to read data from the ADC, address line A11 is set to a logic high level and $\overline{IS}$ is set to logic low. A11 and $\overline{IS}$ form the inputs to the control logic that drives the $\overline{OE}$ pin to logic low and thus switches the data bus driver SN74AC573 from tristate to an active state.

The ADC 20 MHz sampling frequency is generated by the DSP, which outputs the 20 MHz signal at CLKOUT1 pin. The CLKOUT1 signal is connected directly to the BNC input J1 of the TLC5510 EVM. A pair of 74AC11004 inverters buffers the clock before it is taken to both the ADC and the connecting strip J5-22.

Figure 5. TLC5510 EVM toTMS320C203 DVM Interface Schematic



Software Overview

The program editing and assembly are done on the host PC and downloaded to the TMS320C203 DVM for real time processing.

The DSP executes the interface program and acquires and processes *n* input samples from the ADC. Figure 6 shows the program flowchart.

The Crystal is 40 MHz. The internal CPU CLK for the C203 DSP is 20 MHz. CLK IN for the TLC5510 is driven by CLKOUT1, which is 20 MHz.

The program starts with a common initialization procedure for the DSP followed by the initialization of several auxiliary registers (ARs).

The following steps define the program constants:

1) Set the data page pointer to 0h.

2) Set Starting Address.

3) Set number of samples.

4) Set A/D address.

The program executes the following steps:

1) On interrupt, disable global interrupts and save PC, ARs, and Status Registers.

2) Initialize the C203 DSP.

3) Load the appropriate ARs.

4) Send the device address to the TLC5510, loading the A/D output into the memory

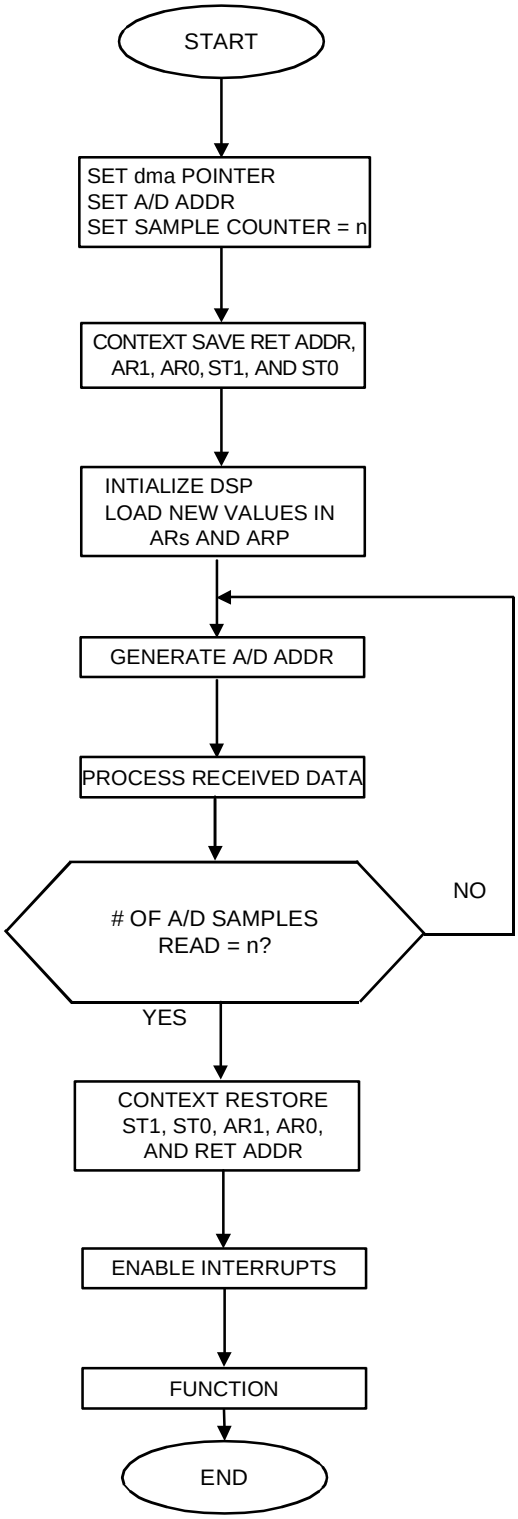
5) After obtaining a predefined number of A/D converter samples, the DSP exits the “loop” subroutine.

6) Restore the PC, Status Registers, and ARs.

7) Enable global interrupts.

The data is now available for use in customer-defined functions (algorithms).

Figure 6. TLC5510 to TMS320C203 Interface Program Flow Chart



Appendix A. Program Listing

```
*************************************************************************
˝
* (C) TEXAS INSTRUMENTS, INC., 1997                                     *
˝
* File: TLC5510.ASM                                                     *
* Interface 'C203 Wyle C2xx DSP Development Board to the TLC5510        *
*************************************************************************
; This routine allows the TMS320C203 DSK+ to interface with the TLC5510
; on the external data bus of the DSP. The TLC5510 is a CMOS, 8-bit,
; 20 MSPS analog-to-digital converter(ADC) that utilizes a semiflash
; architecture and operates with a single 5V supply.

;                .length 55         ; Page length = 55 lines
;                .width  80         ; Page width = 80 characters

                .title "TLC5510EVM Interface"

                .mmregs            ; Include C2xx memory-mapped
registers.
*
* Variables
*
ADC_Addr        .set  0800h        ; Define octal latch SN74AC573 output
                                   ; enable(OEn) control bit. Address bit
                                   ; A11 is gated with IS\ and STRB\ to
                                   ; formed the OE\ input signal. The
                                   ; digital data [D1:D8] from the ADC
                                   ; are buffered by the SN74AC573.
;
Mem_Pointer     .set  0F00h        ; Define starting address in data
                                   ; memory.
Sample_Count    .set  001Eh        ; Define the number of analogue input
                                   ; samples read into data memory.
               .ps  0

             B   _TLC5510          ; Reset vector-jump to label _TLC5510
                                   ; on reset.
            CLRC  INTM             ; 2h INT1, external interrupt.
            RET
            CLRC  INTM             ; 4h INT2/INT3, external interrupt.
            RET
            CLRC  INTM             ; 6h TINT, external interrupt.
            RET
                .def _TLC5510      ; Comment this line out when using
                                   ; Wyle TASM
locals          .set 0             ; Set equal to the number of local
                                   ; variables.
                .ps  1000h
                .entry
*
* Our program begins at address 1000h
*
_TLC5510:
;
;Context save
            POPD *+                ; Save return address
```

```
            SAR AR0, *+             ; Save FP
            SAR AR1, *              ; Save SP
            LAR AR0, *+, AR1        ; Set-up new FP
            ADRK locals             ; Set-up new SP for local variables

            SST  #1, *+             ; Save status registers
            SST  #0, *+             ;
;Save is complete
;
*
*Initialisation
*
;
            LAR  AR2, #ADC_Addr     ; Address for A/D converter, set A11
            LAR  AR3, #Mem_Pointer  ; Pointer to data memory for conv.
                                    ; values
            LAR  AR4, #(Sample_Count-1); Counter for the number of samples
            MAR  *, AR3             ; Select AR3.
*
* Transfer ADC data
*
;
W_LOOP:    IN *+, ADC_Addr, AR4     ; Save each read A/D converter sample
                                    ; in data memory.
            Banz W_LOOP, *-, AR3    ; Loop for n = sample_count-1
*************************************************************************
*         Stack Management on Exit                                      *
*************************************************************************
; Context restore
            MAR *, AR1              ; Set ARP = SP
            MAR *-                  ; Point to saved ST0
            LST #0, *-              ; Restore ST0
            LST #1, *               ; Restore ST1 and ARP
            LAR AR1, *-             ; Pop old SP
            LAR AR0, *-             ; Pop FP
            PSHD *                  ; Put return address on H/W stack
            CLRC INTM               ; Enable interrupts
            RET

      .END                          ; Assembler module end directive
                                    ; -optional.
```