Application Report
SLLA326–April 2012

TLK10002 Latency Measurement in Wireless Base Station System

Junming Li, Maxwell Robertson — *Communications Interface*

ABSTRACT

Latency is one of the primary concerns in wireless base station design. For the systems employing MIMO technology, all transmissions from several base stations in one cell must be strictly synchronized. Therefore, the latencies of different transmitters and other components on the cascaded transmitter signal chain need to be measured precisely for compensation.

With higher and higher data rates needed to support the CPRI link between baseband units (BBUs) and remote radio units (RRUs), it becomes increasingly difficult to accurately measure the latency through the high speed serializer or deserializer (SerDes) used to transmit and receive data. However, the accuracy of the latency measurement is critical to the overall system's performance.

This report briefly introduces the latency measurement function of Texas Instruments' 10 Gbps SerDes transceiver, the TLK10002, as well as the latency contributions of its various internal logic blocks. Two methods of latency measurement and calculation methods are presented along with a discussion of their accuracies.

Contents

List of Figures

1 TLK10002 Latency Measurement Function and Latency Contributions

TLK10002 is a two-channel serializer and de-serializer with support for next generation high bit rate WI serial links up to 10 Gbps. It supports standard CPRI (1x/2x/3x), OBSAI (1x/2x), 1GbE, Fiber Channel (1x/2x), and proprietary data rates, which is ideal for baseband unit to remote radio unit data links.

1.1 Basic Latency Measurement with Stopwatch Circuits

The TLK10002 has built-in measurement function consisting of two groups of stopwatches and the latency counter, which could be employed for some blocks' latency measurement. The first comma found at the assigned counter start location will start up the latency counter, and the first comma detected at the assigned counter stop location will stop the latency counter. Therefore, the duration between the start location and stop location can be measured accordingly, as shown in Figure 1.

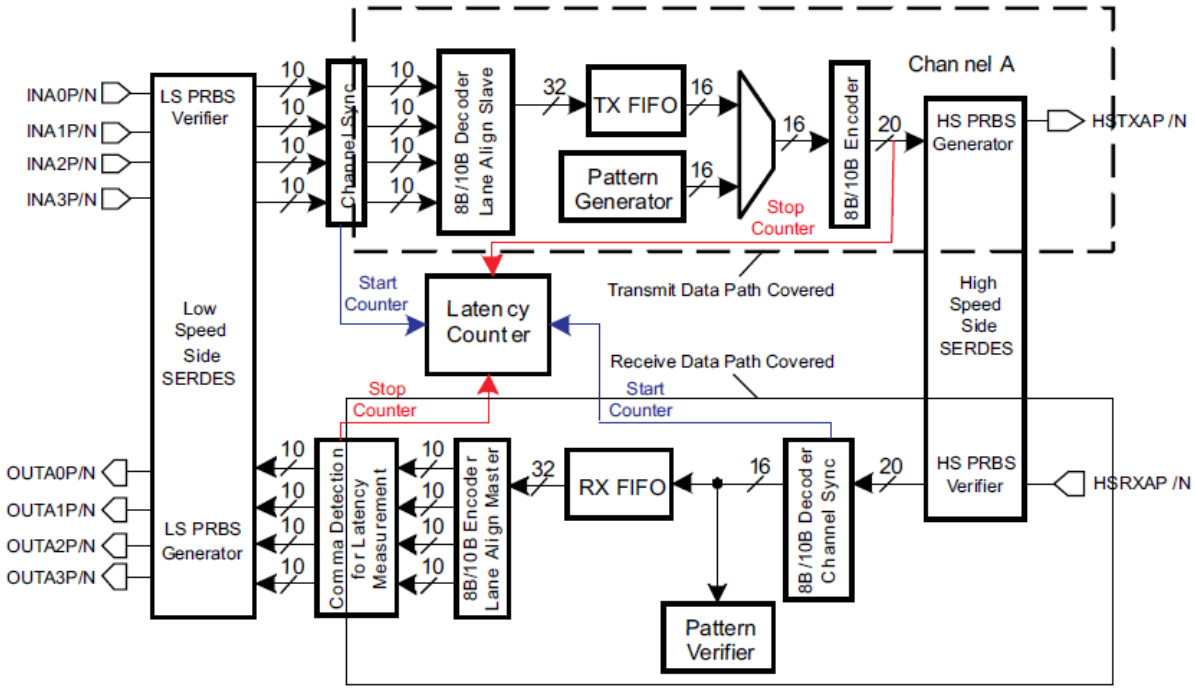

Figure 1. Latency Measurement with Stopwatches

1.2 Latency Contribution and Stopwatch Measurement Restriction

For a given 10 Gbps system in 4:1 mode, the latency contributions of TLK10002 and FPGA are shown in Figure 2. The main block's latency of TX/RX path could be measured through the stopwatch function, however, there are still some blocks which are not contained within the stopwatch circuit and could not be measured directly.

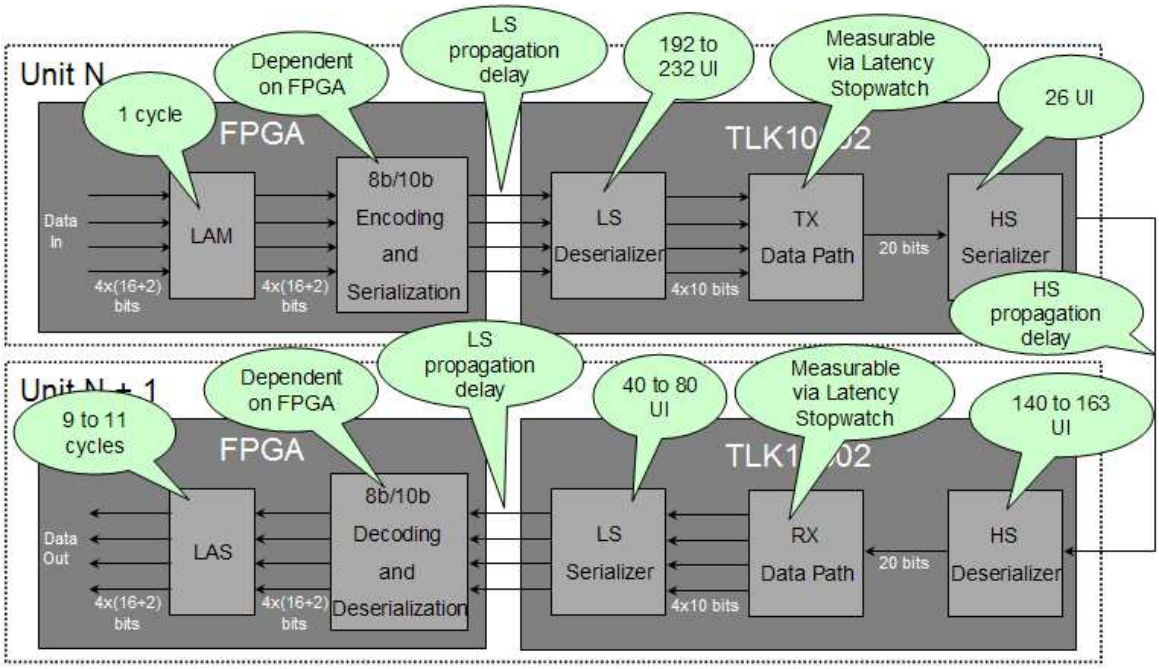

Figure 2. TLK10002 Latency Contribution in 4:1 Mode at 10 Gbps

In the TX direction, the blocks outside of the measurement circuit are:

- LS deserializer
- Part of the channel synchronization block
- HS serializer

In the RX direction, the blocks outside of the measurement circuit are:

- HS deserializer
- Part of the channel synchronization block
- LS serializer

These blocks will have a fixed latency during normal operation, but their latencies can take on a range of possible values each time the serial link is established. If these ranges are not accounted for, the accuracy of the overall latency measurement will be reduced.

1.3 Latency Uncertainty and Variance

In the TX direction, the latency through the device that occurs outside of the stopwatch measurement circuit is between 192 high-speed unit intervals (HSUI) and 232 HSUI before the counter start location and 26 HSUI after the counter stop location in 4:1 mode (full rate). This gives a maximum variance of 40 HSUI. Of this 40 HSUI, 4 HSUI is due to the deserializer's latency variance and 36 HSUI is due to latency variance in the channel synchronization logic. The channel synchronization logic is used to align the deserialized data to 10-bit word boundaries by using comma detection, so its latency will vary depending on the incoming data's word framing. Note that it is possible to eliminate this 36 HSUI range by allowing the LS deserializer to perform comma alignment during link initialization. This brings the overall TX latency uncertainty to just 4 HSUI, or about 0.407 ns at a high speed line rate of 9.8304 Gbps.

In the RX direction, the latency through the device that occurs outside of the stopwatch measurement circuit is between 140 HSUI and 232 HSUI before the counter start location and between 40 HSUI and 80 HSUI after the counter stop location in 4:1 mode (full rate). This gives a total range of variance of 63 HSUI. This amount of possible variance is significantly larger than in the TX direction, so it is especially beneficial to reduce this range through measurement.

The following sections will discuss the latency measurement of the blocks which are outside the stopwatch measurement circuit as well as the latency calculation and measurement of the blocks which have a large amount of latency variance. Measurement approaches using loopback configuration and without loopback configuration will be discussed separately.

2 Latency Measurement with Loopback Mode

2.1 LS Serializer Latency Calculation

The LS serializer's latency can be measured through loopback of the LS side, as shown in Figure 3. The counter stop point can be set before RX data path, and the counter stop point can be set after the TX data path. The loopback latency measurement provides the latency from reception of a comma on the HS RX side to transmission of a comma on the HS TX side. Looping back the data inside the FPGA allows the link to remain established throughout the measurement.

The whole loop consists of the following five parts: the RX data path, FPGA, LS deserializer, LS serializer and TX data path.

Assuming the latency of LS serializer is T_{ls}, we get

$$T_{ls} = T_{total} - T_{rx} - T_{fpga} - T_{lsd} - T_{tx} \quad (1)$$

Where the T_{total} is the total LS loopback latency, T_{rx} is the latency of RX data path, T_{fpga} is the latency in FPGA,T_{lsd} is the latency of LS deserializer and T_{tx} is the latency of TX data path.

In this equation, the total LS loopback latency could be measured through the stopwatch circuits via the LS side loopback. The TX and RX data paths' latencies could also be directly measured through the stopwatch circuits. The LS deserializer's latency is approximately 70 HSUI. The latency inside the FPGA could be measured through a simple stopwatch circuit. It will start its count when a comma is detected at the input and stop its count when a comma is detected at the output.

As T_{total}, T_{rx}, T_{fpga}, T_{tx}, are all measurable or known value, T_{ls} can be calculated accordingly.

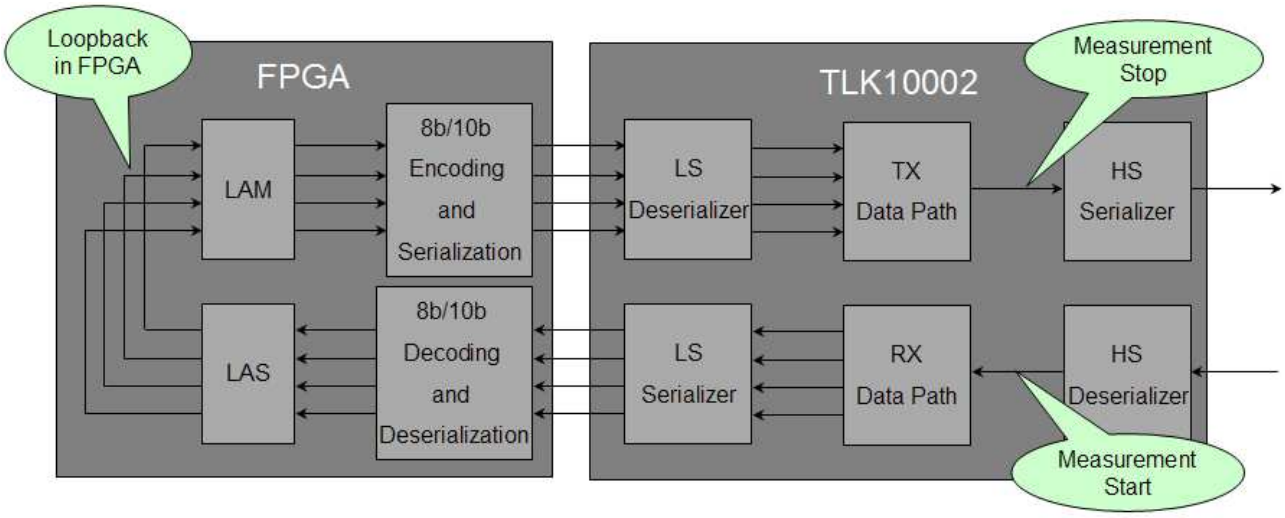

Figure 3. LS Side Loopback

2.2 HS Deserializer and HS Channel Sync Latency Calculation

Besides the LS serializer, there are also some parts which have variable latency before the RX-direction stopwatch start location—the HS deserializer and HS channel synchronization block. The HS deserializer has 3 HSUI of possible variance; the HS channel sychronization block has 20 HSUI of possible variance. These variances can also be reduced by HS side loopback testing.

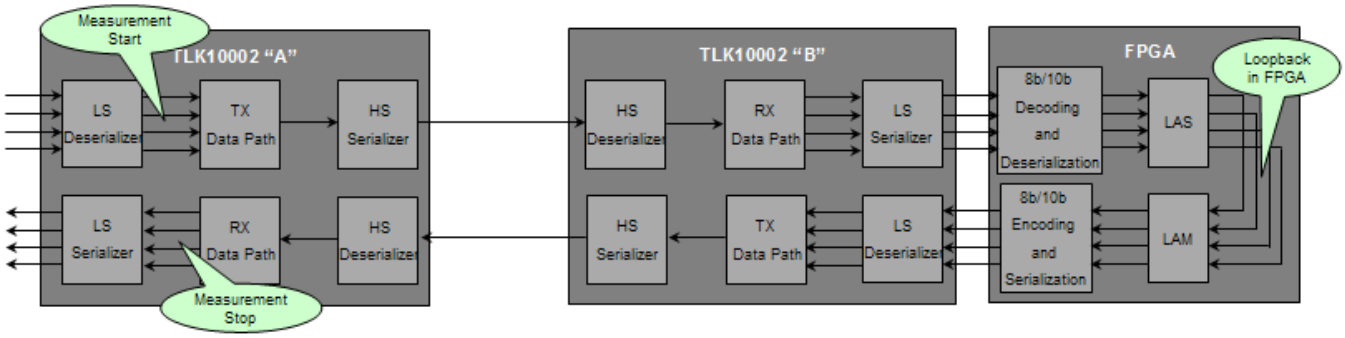

Figure 4. Far-End Loopback

As shown in Figure 4, the data is looped back within the FPGA at the far end of the link. This gives the full round-trip latency including two TX data paths, two RX data paths, two fiber delays, and the loopback delay within the FPGA. The start comma and stop comma positions are the same with that of the LS loopback mode, however, the data passes through the full round-trip in the far-end device.

The full loop consists of the following parts: two TX data paths, two RX data paths, two HS serializers, two HS deserializers, two HS channel synchronization blocks, one LS serializer, one LS deserializer, the FPGA, and the physical interconnect. Assuming the full path latency is T_{total}, we get

$$T_{total} = T_{txa} + T_{hsa} + T_{media} + T_{hdb} + T_{hcsb} + T_{rxb} + T_{ls} + T_{fpga} + T_{ld} + T_{txb} + T_{hsb} + T_{hda} + T_{hcsa} + T_{rxa} \quad (2)$$

Where T_{txa} and T_{txb} are the latency of the two TX data paths, T_{rxa} and T_{rxb} are the latency of two RX data paths, T_{hsa} and T_{hsb} are the latency of two HS serializers, T_{hda} and T_{hdb} are the latency of two HS deserializers, T_{ls} is the latency of the LS serializer, T_{ld} is the latency of the LS deserializer, T_{hcsa} and T_{hcsb} are the latency of two HS channel synchronization blocks, T_{fpga} is the latency of the FPGA and T_{media} is the latency of physical interconnect media.

In the equation, T_{total}, T_{txa}, T_{txb}, T_{rxa}, T_{rxb}, T_{hda}, T_{hdb}, T_{ld}, T_{ls}, T_{fpga} can be measured through the stopwatch circuits or have a known value. Therefore, these known blocks can be subtracted from the loopback measurement, giving a value equal to twice the interconnect delay plus the HS serializer & channel synchronization latencies for the near- and far-end devices. That is,

$$T_{hsa}+T_{hsb}+T_{hcsa}+ T_{hcsb} + T_{media} = T_{total} - T_{txa} - T_{txb} - T_{rxa} - T_{rxb} - T_{hda} - T_{hdb} - T_{ld} - T_{ls} - T_{fpga} \quad (3)$$

This value can be divided by two to estimate the latency for the interconnect plus the HS serializer and channel synchronization in one direction, either uplink or downlink.

3 Latency Measurement without Loopback Mode

Instead of aligning the TX and RX commas, it may be easier to simply measure the time between them using a stopwatch circuit, as shown in Figure 5.

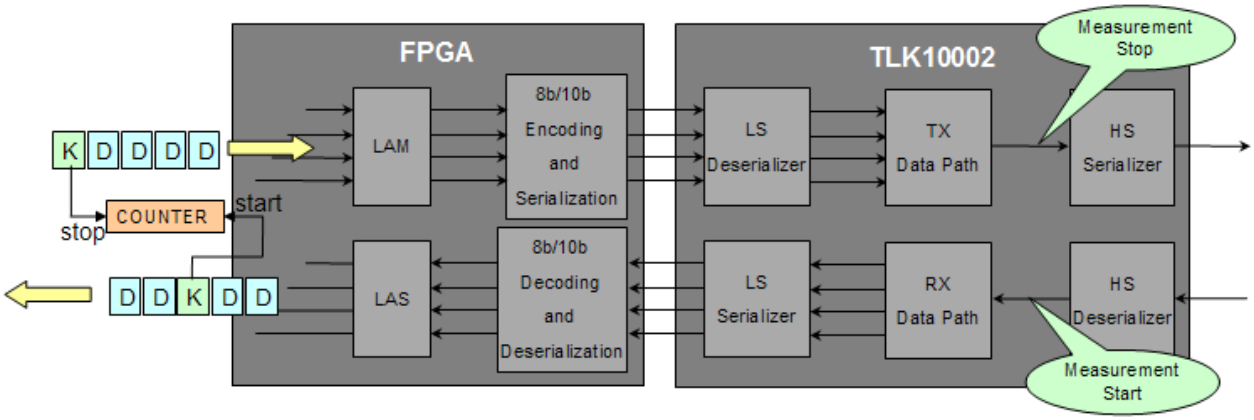

Figure 5. Latency Measurement Without Loopback Mode

This method has several advantages. The latency can now be measured at any time during operation. The link remains up throughout the measurement and normal data transmission is not altered or interrupted. There is no requirement on the relationship between the transmitted and received data; the two data streams can be completely independent

3.1 LS Serializer Latency Calculation

As discussed in the last section, Equation 1 can be used to calculate the LS serializer latency in loopback mode. This same equation can be modified for a non-loopback approach. It will just need to include the time that elapses between received and transmitted commas. The first term in the equation (LS Loopback Latency Measurement) is no longer a real loopback measurement, but now simply the time between comma detection at HS receiver and comma detection at HS transmitter. Hence, the LS serializer latency calculation in non-loopback mode could be expressed as Equation 4

$$T'_{ls} = T'_{total} - T_{rx} - T'_{fpga} - T_{lsd} - T_{tx} \quad (4)$$

Where T'_{total} is the latency between TLK10002 HSRX and HSTX commas, T_{rx} is the latency of RX datapath, T_{tx} is the latency of TX datapath, T_{tx} is the latency of LS deserializer and T'_{fpga} is the time between RX and TX commas in the FPGA.

In this equation, T_{tx}, T_{rx} and T'_{fpga} can be measured through the stopwatch circuits, the LS deserializer latency can be estimated to be 70 HSUI in 4:1 mode at 10 Gbps, and T'_{total} could be measured by the FPGA by detecting the difference of HSRX and HSTX commas. Therefore, T'_{ls} can be calculated through Equation 4.

4 Measurement Error Analysis

For the TX direction, everything is directly measured except for the channel synchronization block and the LS deserializer. As previously discussed, the uncertainty in the channel synchronization block can be eliminated by fixing the alignment of LS deserializer. If the latency of the LS deserializer is estimated to be 70 HSUI, then the maximum error is 2 HSUI (~0.203 ns).

The LS serializer can be calculated, but the calculation includes an estimate of the LS deserializer latency. Therefore, the same maximum error applies (~0.203 ns).

For the HS deserializer and channel synchronization, the previously described method provides an estimate for the latency that is equal to the average value measured for two devices. If these blocks vary the same way in both devices, there will be no error introduced. The maximum error introduced would be when both devices vary at opposite extremes of their range. In this case, the maximum measurement error would be 11.5 HSUI (~1.17 ns).

Overall, the amount of latency measurement uncertainty for data passing through the TLK10002 TX data path is 0.203 ns. The amount of latency measurement uncertainty for data passing through the TLK10002 RX data path is 0.203 ns + 1.17 ns=1.373 ns. These values should be able to meet the stringent requirements of most wireless base station applications.

5 Conclusion

This document introduces the latency variance and latency measurement approaches of TLK10002. In summary, the latency of the main blocks of TLK10002 could be directly measured by the stopwatch circuits. For the parts which are not included in the stopwatch circuits and have large variance, the latency could be precisely calculated using the loopback mode or non-loopback mode presented in this report.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265