Hybrid Battery Charger With Load Control for Telecom Equipment

ABSTRACT

Commercial telecom equipment needs multiple power input systems to ensure continuous network connectivity. The load must be backed up to different sources. This application note describes a synchronous-buck-based reference design using MSP430, CSD87350 power blocks and the UCC27211 half-bridge driver to use multiple OR'ed inputs (solar and AC/DC adaptor) to charge a 12-V SLA battery. Priority charging is used when solar energy is available. Seamless transfer between two sources ensures battery is always charged when inputs are available. It runs MPPT algorithms to charge while on solar input and conventional CC/CV charging when working from an adaptor input. Multiple protection schemes ensure it is a robust design.

Topic **Page**

Trademarks

1 Design Specifications

Table 1. Design Specifications

Parameter	Description	Value
V_{IN} range	Panel	16.5 to 21 V
	Adaptor	15.5 to 16 V
Battery specifications	Capacity	12 V, 100 Ah
Charging specifications	Charging current	7 A
	Voltage during CV mode charging	14.2 V
F_{SW}	Switch frequency	100 kHz
Output specifications	Load current	4 A
	Output voltage	10.2 to 14.2 V
Protection features	• Hot swappable load • Output short circuit • Reverse polarity protection • Two level overcurrent protection • Battery UVLO • Overtemperature protection	

2 Block Diagram

Figure 1 shows the block level implementation of the system.

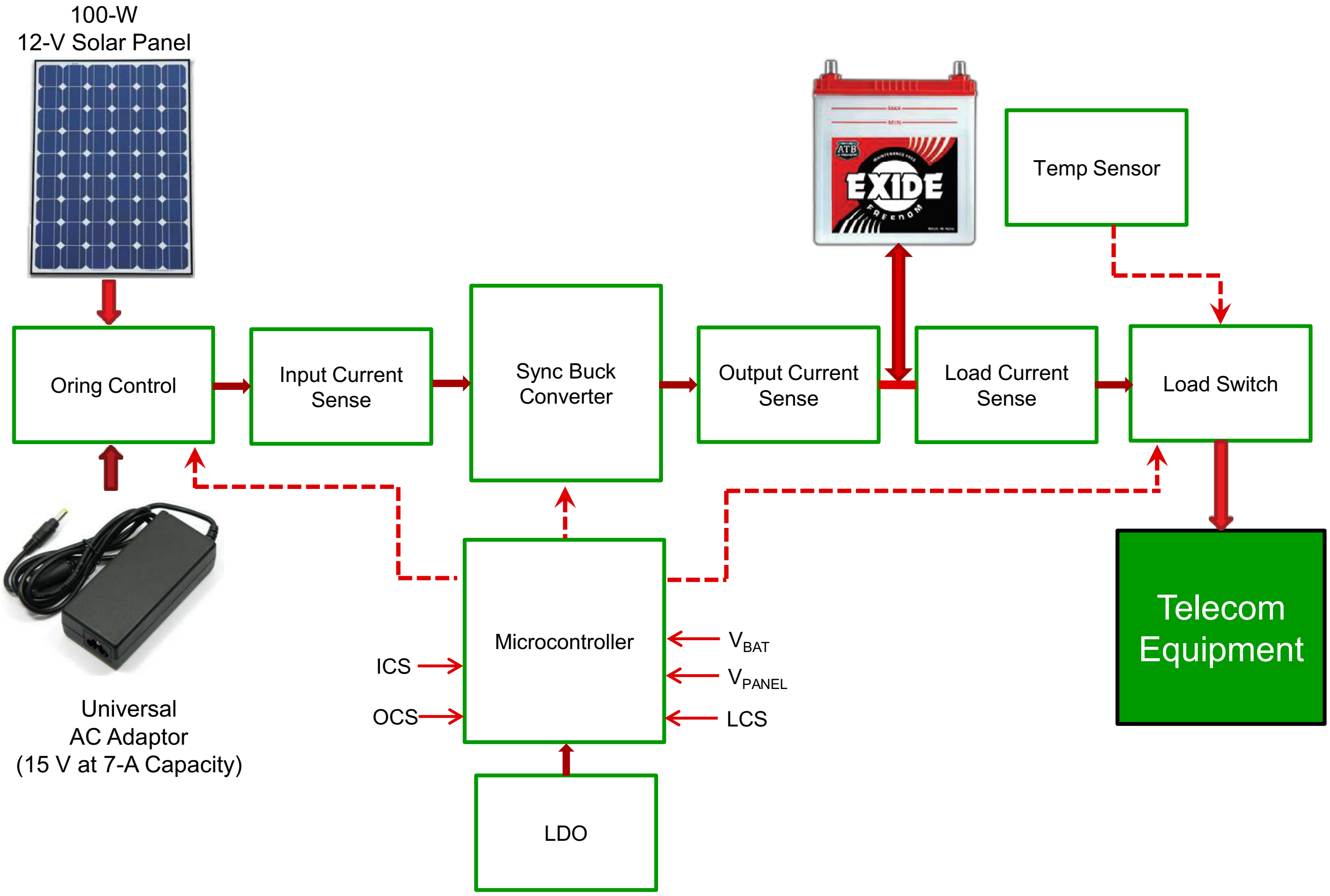


Figure 1.

3 System Explanation and Design

3.1 Power Source Control and Monitoring

The telecom equipment (load) is always powered either from a solar panel, AC/DC adaptor, or the battery. As long as solar energy from the panel is available, priority charging is used to deliver the required power (average 17 V and current sufficient enough to manage load or to charge battery). If panel voltage drops below adapter (15 V), the charge controller microcontroller turns off the panel switch and turns on the AC/DC adapter switch, which also ensures no leakage of the stronger source into the weaker one. Two 30-V, ultra-low $R_{DS(on)}$ FETs from TI (CSD17527Q5A) are selected for this purpose. The simple transistor is used for proving the drive from the microcontroller.

3.2 Synchronous Buck Power Stage

The synchronous buck convertor has better efficiency and lower loss compared to asynchronous topology because a diode on the bottom side is replaced with a low $R_{DS(on)}$ value. A single 30-V, 25-A power block from TI (CSD87350Q5D) is selected for this. The advantage of a power block is the smaller package and ease of layout eliminating parasitics of board layout of high frequency hot nodes. The microcontroller PWM module can generate multiple PWMs on the same timer base. Each output can be configured for different output modes, for example, toggle, reset/on, reset/off, always on, and so forth. With this flexible logic, the user can achieve complimentary logic with required dead band. However, a half-bridge driver with a floating high side drive is required to drive the high side and low side MOSFETs. The UCC27211, *UCC2721x 120-V Boot, 4-A Peak, High-Frequency High-Side and Low-Side Driver*, has high drive strength, low propagation delays, and excellent delay matching to optimize the timing of the buck power stage resulting in minimal switching loss. The other power stage components (inductor and capacitor) calculations are designed using standard equations of the buck converter based on the prior specifications.

- L_{OUT} (cal) = 12.67 µH, selected L_{OUT} = 10 µH, from Wurth Electronics
- Selected C_{OUT} = 47 µF × 1; 22 µF × 2

3.3 Current Sense Inputs

To ensure continuity to ground loop, a high-side sense circuit was used. A zero-drift instrumentation amplifier from TI, INA282, with a 50-V/V gain, wide common-mode input range is selected for this application.

3.4 Load Management

A simple load switch with hotswap control from TI TPS25910 is used for monitoring the load behavior. If there is any short or overload, it immediately trips sending it into a hiccup mode on the load. The fast-trip comparator of the microcontroller also quickly disables the PWM. This is second-level protection for the load. To prevent the load from discharging back into the source, a blocking FET (CSD17313Q2) from TI is used. It is controlled by the load switch.

3.5 Microcontroller

A MSP430F5132 microcontroller is used in this application. See *Section 4* for further details of the software routines.

3.6 LDO and Temperature Sensor

A simple OR’ed supply is used as the input of the LDO to ensure that power to the controller is always available to sense any inappropriate condition. The 3.3 V generated by the LDO (TPS73801) is used to power the MCU, LEDs, instrumentation amplifiers, and a simple thermostat TMP709, which is used for tripping the load in case there is any abnormal increase in the temperature.

3.7 Battery Management

The section explains the battery management software portion in the microcontroller. It checks for the state-of-charge of the battery and applies the charging profile appropriately. This application uses a lead-acid battery. The following list shows the battery properties that are considered while charging.

- Minimum 2.10 V per cell is considered as a good battery
- Cells in a string are not the same strength, some are weak and some are strong.
- Should not be charged above 50°C
- Overcharging increases the risk of hydrogen gassing on the positive plate.
- Undercharging increases sulfation on the negative plate.
- Battery charge profile is in constant current mode until battery attains, for example, 70%, constant voltage mode from 70% to 90% and float charge after that.

3.8 Maximum Power Point Tracking Algorithm

A simple MPPT algorithm known as perturb and observe is used for controlling this system. As explained in the *PWM Resolution* section, every one count of PWM timer yields 0.04% of duty cycle variation, which is “fine” enough to achieve smoother and slower tracking. With this at MPP stage, there will be 0.04% oscillation which may be negligible in a low-power application. If duty cycle variation is increased more than 1 count, tracking is faster and reduces the variation to minimize the MPP stage oscillations. This also resembles incremental conductance method. It monitors battery/load current with respect to ΔV applied to the converter, increasing the ΔV drives to MPP faster and at the MPP stage reduces the ΔV and settles smoothly at MPP.

4 Software Flow

This application uses the MSP430F5132 microcontroller. The following are key features, which enable efficient usage of resources to achieve an efficient solar power convertor.

MSP430F5132 key features supporting efficiency expectation:

- Fully operates from 3.6 to 1.8 V
- Only 180-µA/MHz active current, lowest current at shut down is 0.25 µA
- Fast wake-up, less than 5 µs from stand by
- 200 KSPS, 10-bit ADC, with just 110-µA current consumption with built-in reference
- Hi-resolution timer/PWM = 4-ns minimum pulse duration, 250-µA current consumption

4.1 PWM Resolution

The MSP430F5132 has a special hi-resolution timer, timer-D. This timer can be programmed to generate high switching frequency to accommodate a smaller inductor's size. This timer is clocked from the following sources:

- MCLK/SMCLK – Maximum range is 16 MHz
- ACLK – Maximum 32 kHz
- Special timer-D clock generator of the following values:
  - 64 MHz
  - 128 MHz
  - 200 MHz
  - 256 MHZ

Effective number of bits (ENOB) is an important parameter in achieving smoother control, thereby reducing switching noise and protecting the battery from stress caused by larger voltage variations caused in a low-resolution system.

$$\text{ENOB} = \text{Log2(Module clock / Output frequency)} \quad (1)$$

This application requires 100-kHz switching frequency. Therefore, the following settings provide,

Module clock = 256 MHz

Output frequency = 100 kHz

ENOB = 11.36 bits

$$V_{OUT} = D \times V_{IN}$$

where

- D = Duty cycle or on-time of the switch
- V_{IN} = Input voltage (from battery, solar panel, or ACDC adapter)
- V_{OUT} = Output voltage (2)

Consider the converter to be 100% efficient. Therefore, no loss factor is taken into account in this calculation. For a single bit change in D varies by approximately 4 ns in a 100-kHz period wave, which is 0.038% of V_{IN}; if a V_{IN} of 17, V_{OUT} varies by 0.00646 V.

4.2 ADC Module

This device has 10-bit SAR ADC, speed can be configured for 50ksps for low power or 200ksps for faster processing. This application can go slow, which helps to conserve additional power loss caused by the ADC module itself (refer to the data sheet for power consumption data). This module can be operated independently without sharing the CPU clock. Hence, the CPU can be placed in low-power mode, enabling only the ADC to function.

A special ADC DMA can be configured to scan all channels and interrupt the CPU when data is available at the RAM for further processing. This application requires 6 channels: battery current, panel current, battery voltage, panel voltage, load current, and temperature sensor. Therefore, a 6-channel conversion is required every loop, until then the CPU can be put in IDLE to conserve power.

4.3 ADC Measurement Range

This MCU has a 10-bit SAR ADC, input voltage range is 0 V to AVCC, which can be up to 3.6 V (refer to data sheet for more electrical data). Hence, input signal strength can be from 3.3 mV per count of ADC until 3.3 V (1023 counts) can be sensed. Sense resistors are 5 mΩ. Hence, minimum current sensible from panel/load/battery with a gain of 50 is about 13 mA.

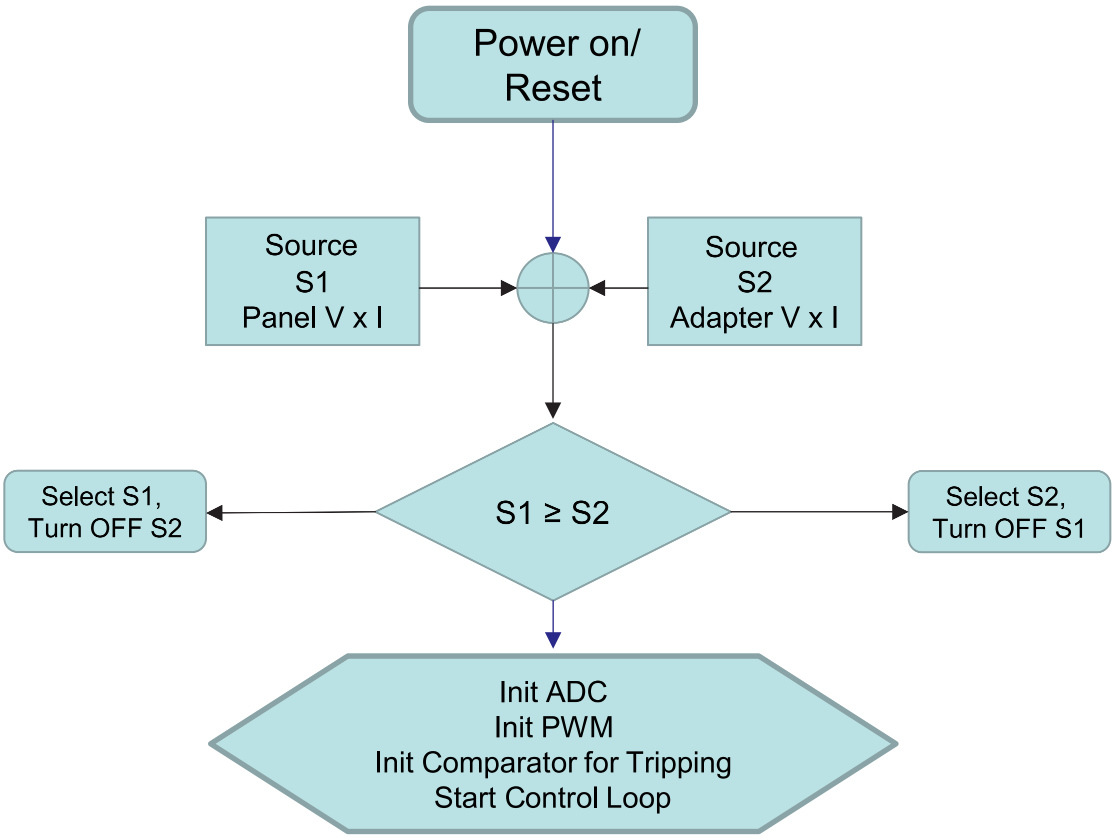


Figure 2. Initialization Flow Chart

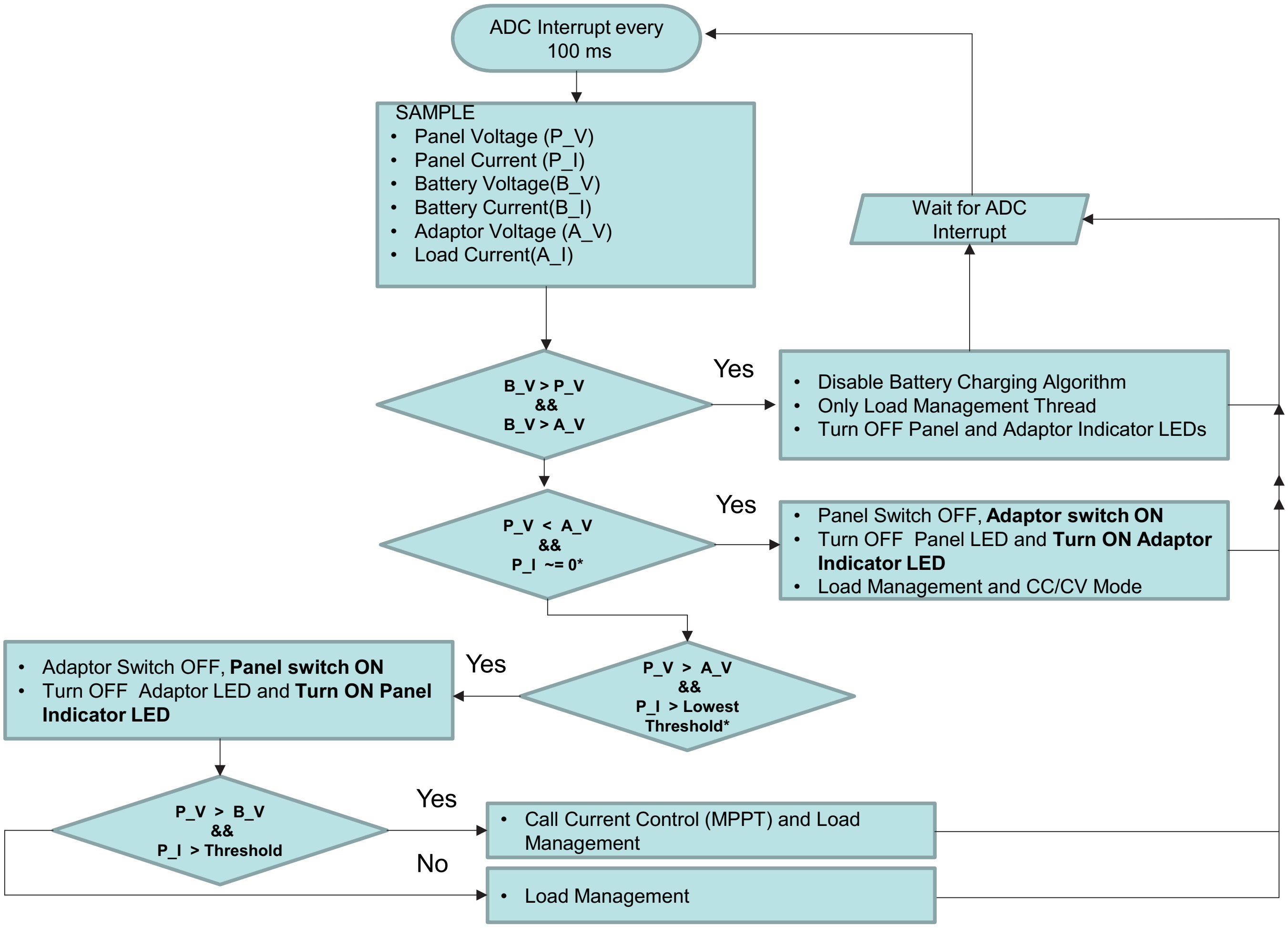


Figure 3. Control Loop Flow Chart

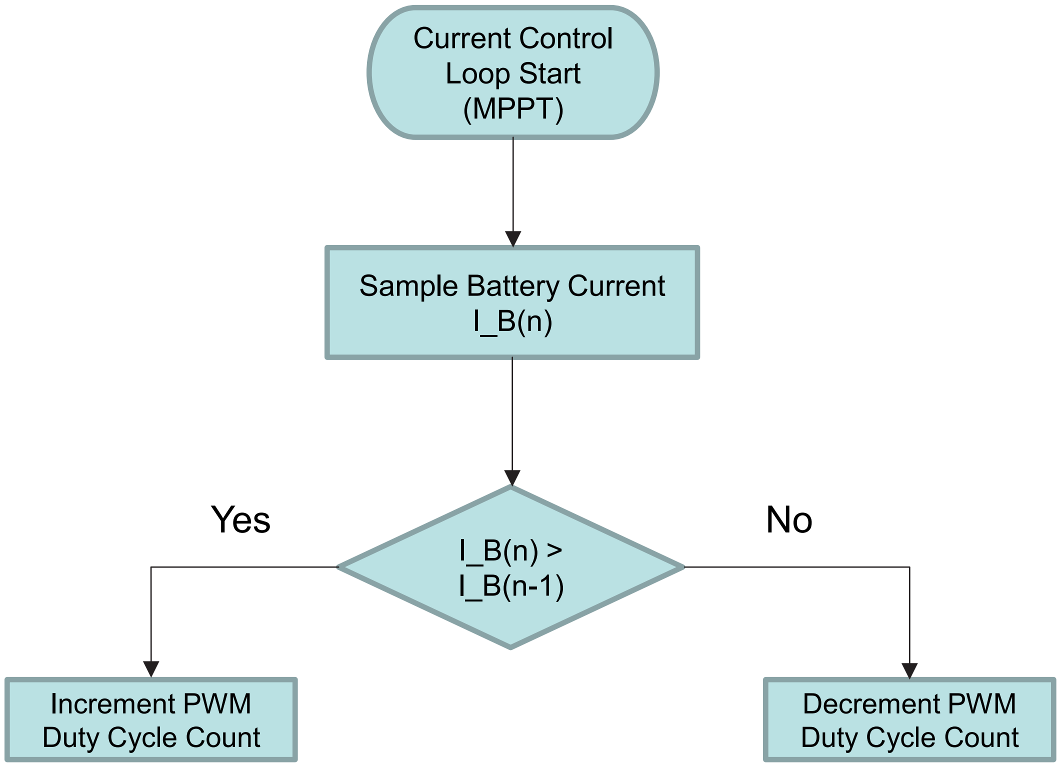


Figure 4. MPPT Algorithm Flow Chart

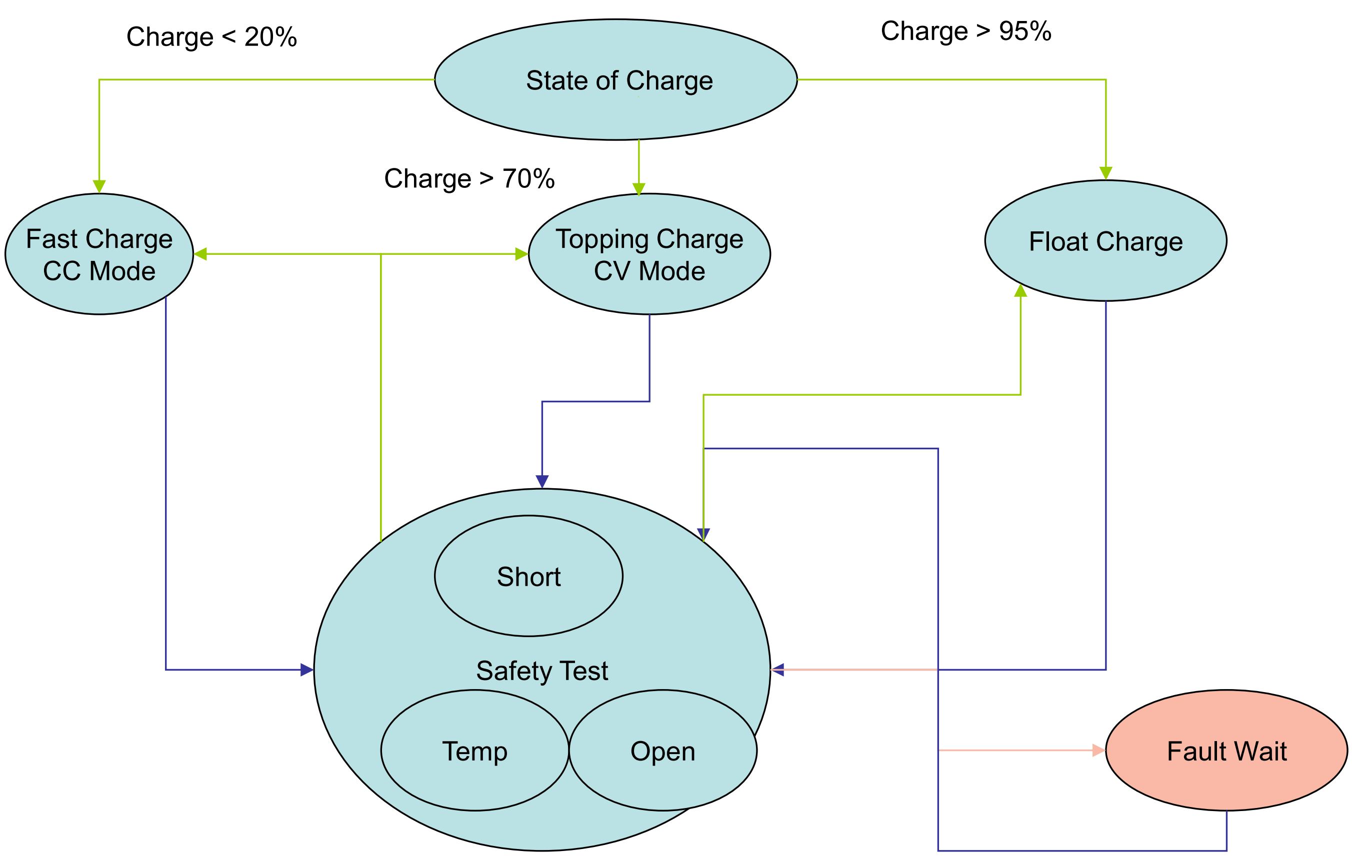


Figure 5. Battery Management Flow Chart

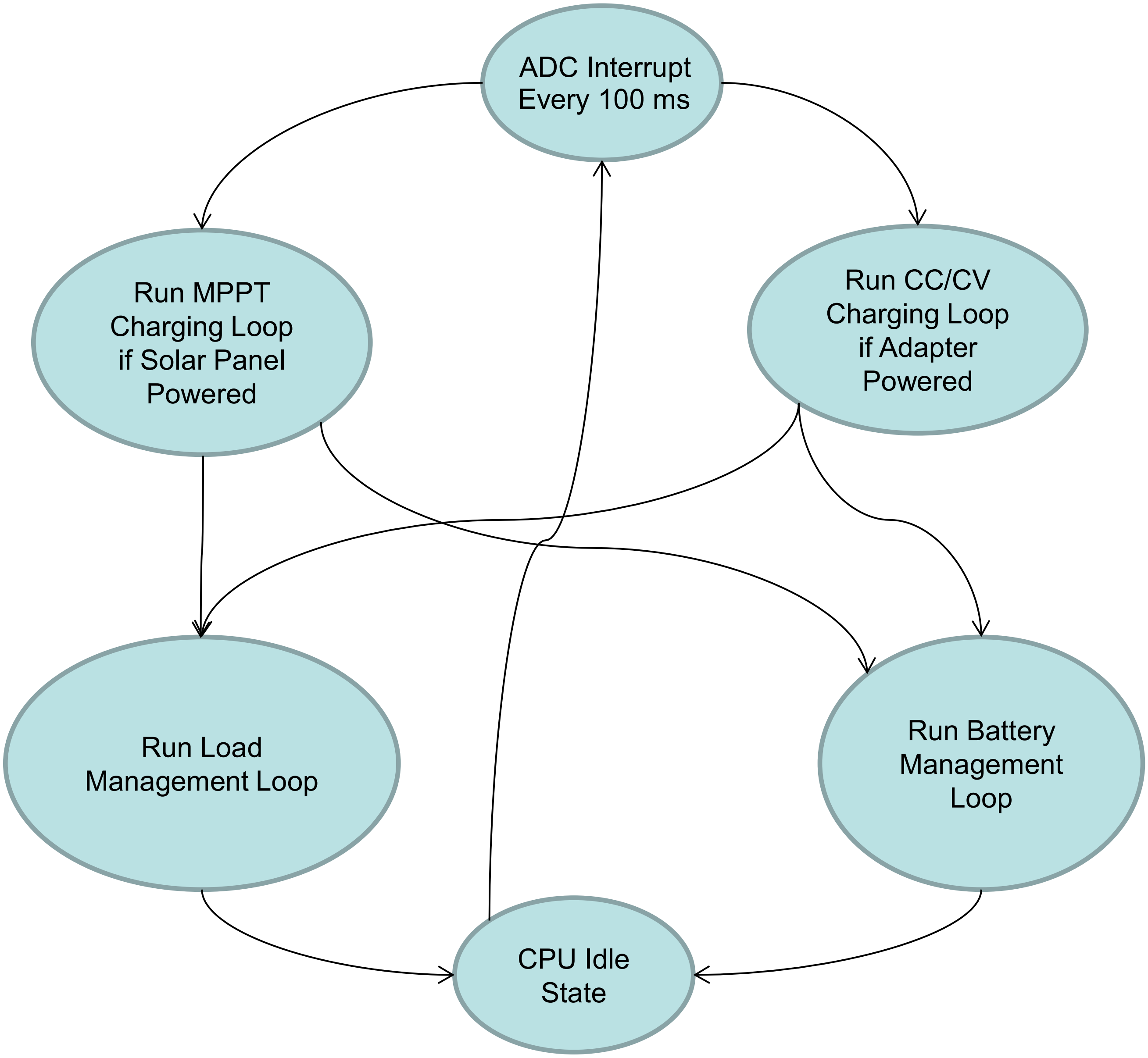
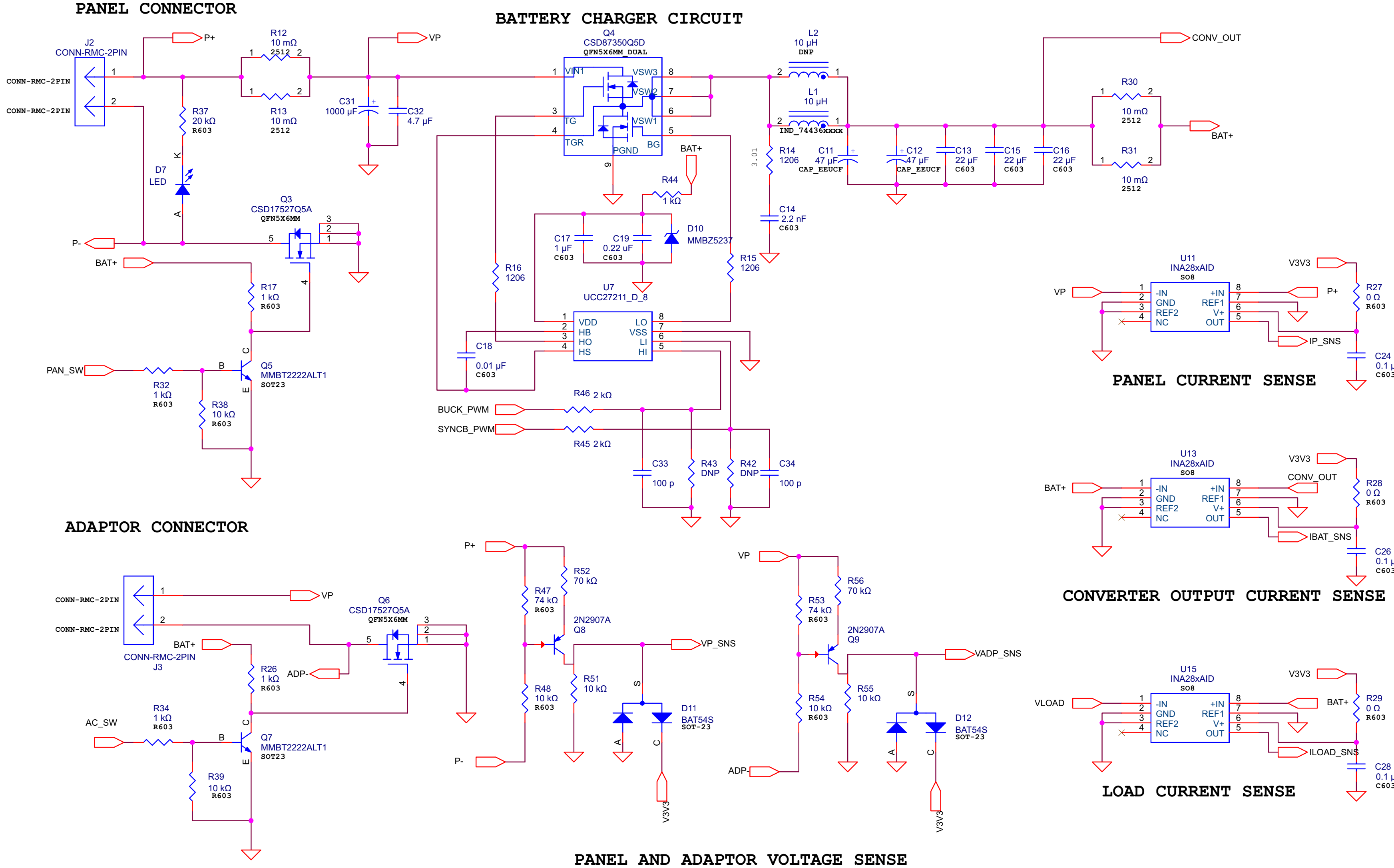
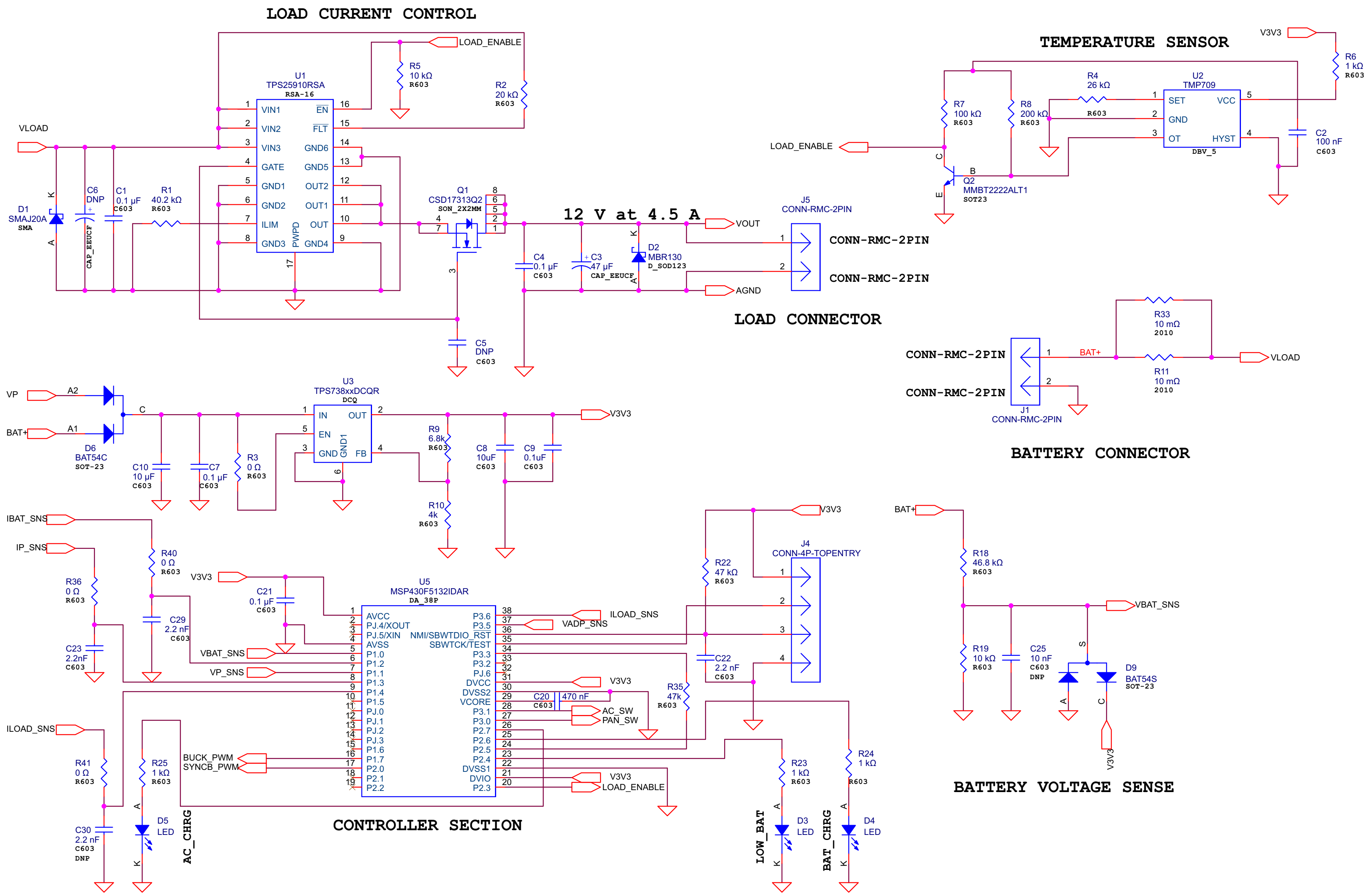


Figure 6. Control Loop Logic

5 Schematics




LOAD CURRENT CONTROL
LOAD_ENABLE
R5
10 kΩ
R603
R2
20 kΩ
R603
U1
TPS25910RSA
RSA-16
VIN1
VIN2
VIN3
GATE
GND1
GND2
ILIM
GND3
EN
FLT
GND6
GND5
OUT2
OUT1
OUT
GND4
PWPD
VLOAD
D1
SMAJ20A
SMA
C6
DNP
CAP_EEUCF
C1
0.1 µF
C603
R1
40.2 kΩ
R603
Q1
CSD17313Q2
SON_2X2MM
12 V at 4.5 A
VOUT
AGND
C4
0.1 µF
C603
C3
47 µF
CAP_EEUCF
D2
MBR130
D_SOD123
J5
CONN-RMC-2PIN
CONN-RMC-2PIN
CONN-RMC-2PIN
LOAD CONNECTOR
C5
DNP
C603
TEMPERATURE SENSOR
V3V3
R6
1 kΩ
R603
R4
26 kΩ
R603
U2
TMP709
SET
GND
OT
VCC
HYST
DBV_5
R7
100 kΩ
R603
R8
200 kΩ
R603
C2
100 nF
C603
LOAD_ENABLE
Q2
MMBT2222ALT1
SOT23
R33
10 mΩ
2010
R11
10 mΩ
2010
BAT+
VLOAD
CONN-RMC-2PIN
CONN-RMC-2PIN
J1
CONN-RMC-2PIN
BATTERY CONNECTOR
VP
BAT+
A2
A1
C
D6
BAT54C
SOT-23
U3
TPS738xxDCQR
DCQ
IN
EN
GND
OUT
FB
GND1
V3V3
C10
10 µF
C603
C7
0.1 µF
C603
R3
0 Ω
R603
R9
6.8k
R603
R10
4k
R603
C8
10uF
C603
C9
0.1uF
C603
IBAT_SNS
IP_SNS
R40
0 Ω
R603
R36
0 Ω
R603
C23
2.2nF
C603
C29
2.2 nF
C603
V3V3
C21
0.1 µF
C603
U5
MSP430F5132IDAR
DA_38P
AVCC
PJ.4/XOUT
PJ.5/XIN
AVSS
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
PJ.0
PJ.1
PJ.2
PJ.3
P1.6
P1.7
P2.0
P2.1
P2.2
P3.6
P3.5
NMI/SBWTDIO_RST
SBWTCK/TEST
P3.3
P3.2
PJ.6
DVCC
DVSS2
VCORE
P3.1
P3.0
P2.7
P2.6
P2.5
P2.4
DVSS1
DVIO
P2.3
ILOAD_SNS
VADP_SNS
VBAT_SNS
VP_SNS
V3V3
C20
470 nF
C603
AC_SW
PAN_SW
BUCK_PWM
SYNCB_PWM
V3V3
LOAD_ENABLE
ILOAD_SNS
R41
0 Ω
R603
C30
2.2 nF
C603
DNP
R25
1 kΩ
R603
D5
LED
AC_CHRG
CONTROLLER SECTION
V3V3
R22
47 kΩ
R603
J4
CONN-4P-TOPENTRY
C22
2.2 nF
C603
R35
47k
R603
R23
1 kΩ
R603
D3
LED
LOW_BAT
R24
1 kΩ
R603
D4
LED
BAT_CHRG
BAT+
R18
46.8 kΩ
R603
VBAT_SNS
R19
10 kΩ
R603
C25
10 nF
C603
DNP
D9
BAT54S
SOT-23
V3V3
BATTERY VOLTAGE SENSE

6 Test Results

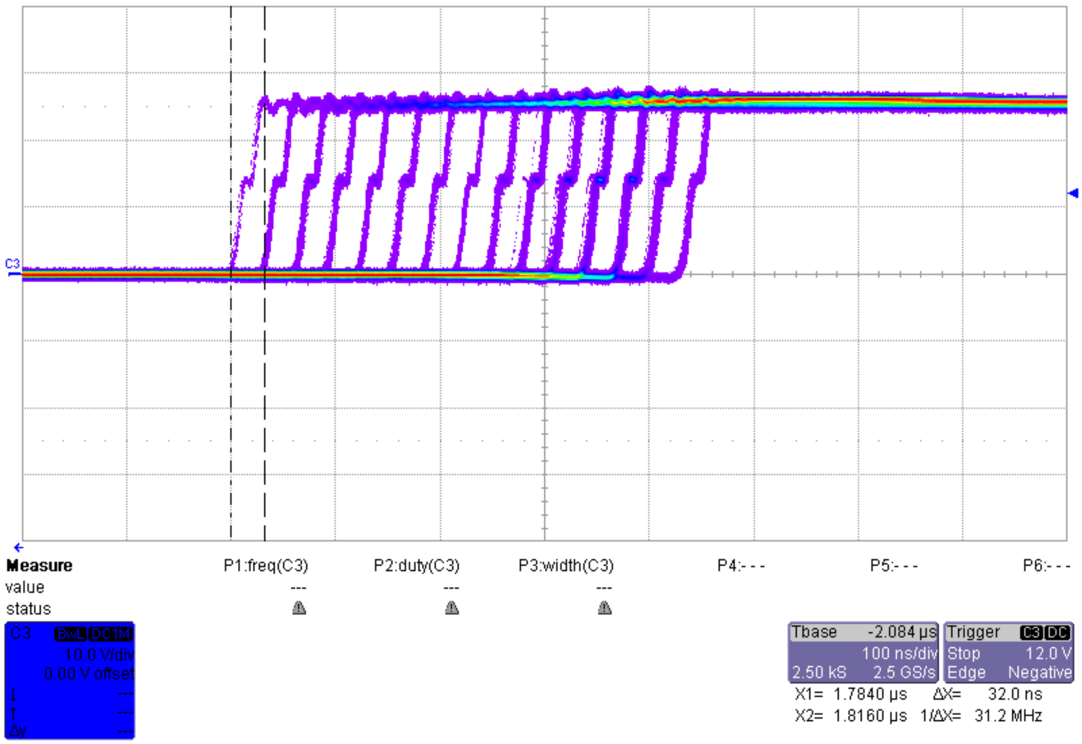


Figure 7. Variation of the Duty Cycle from the Controller

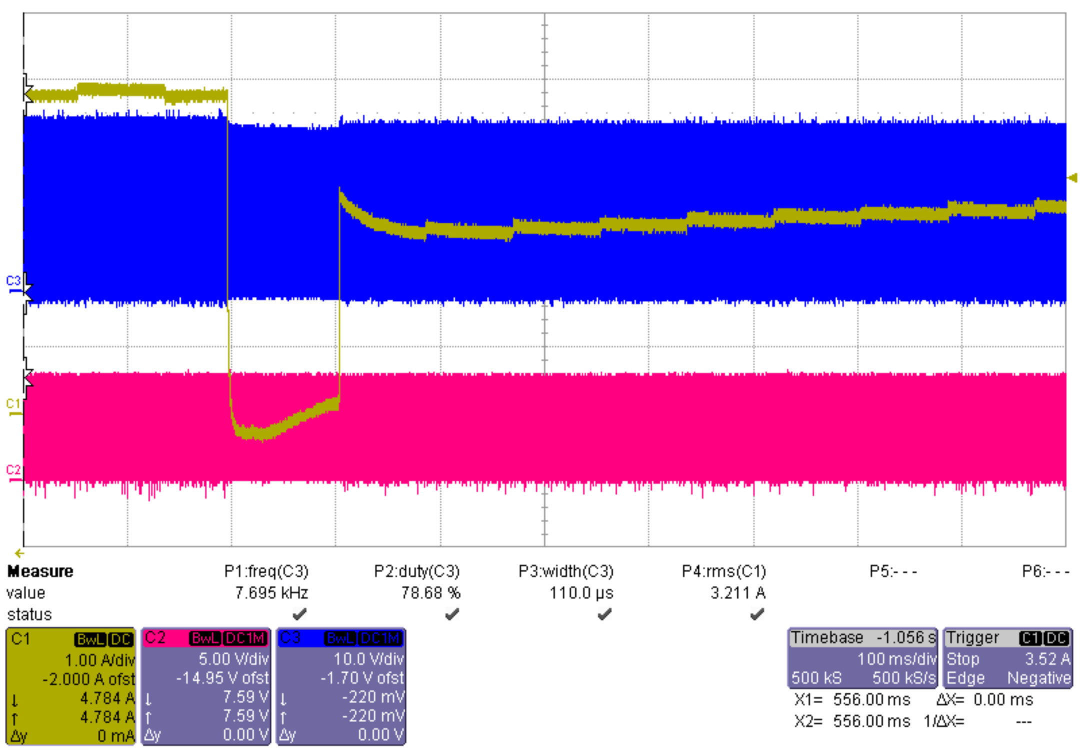


Figure 8. Seamless Transfer from Panel to Adaptor

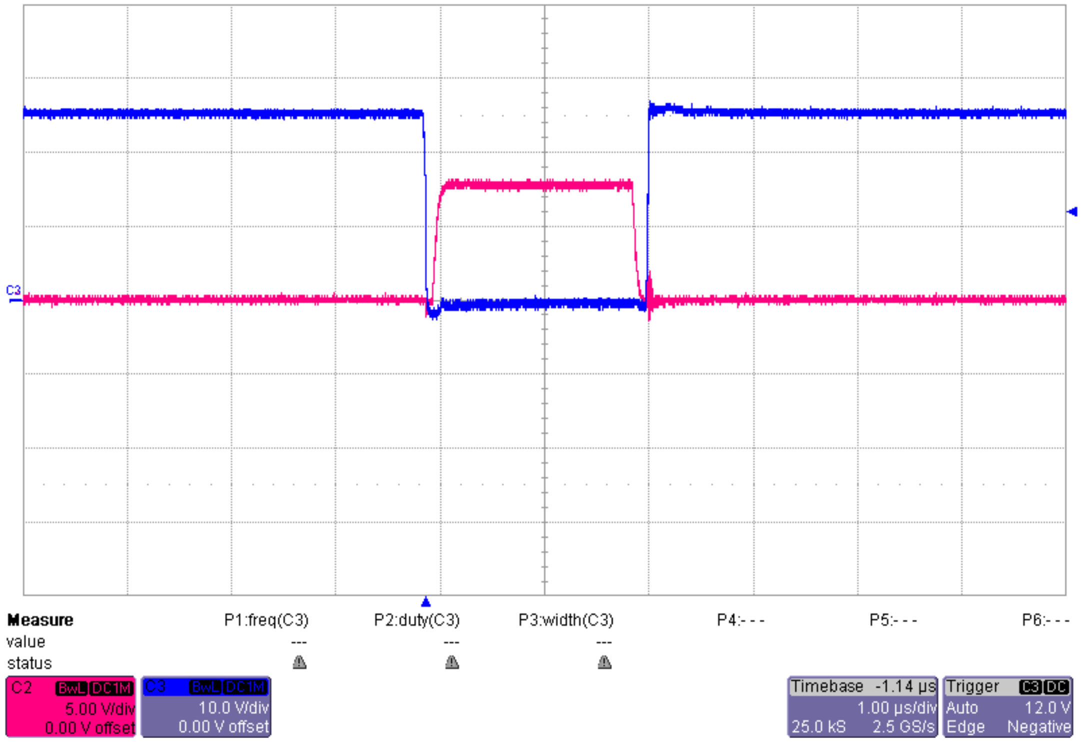


Figure 9. Output PWM Pulses from UCC27211

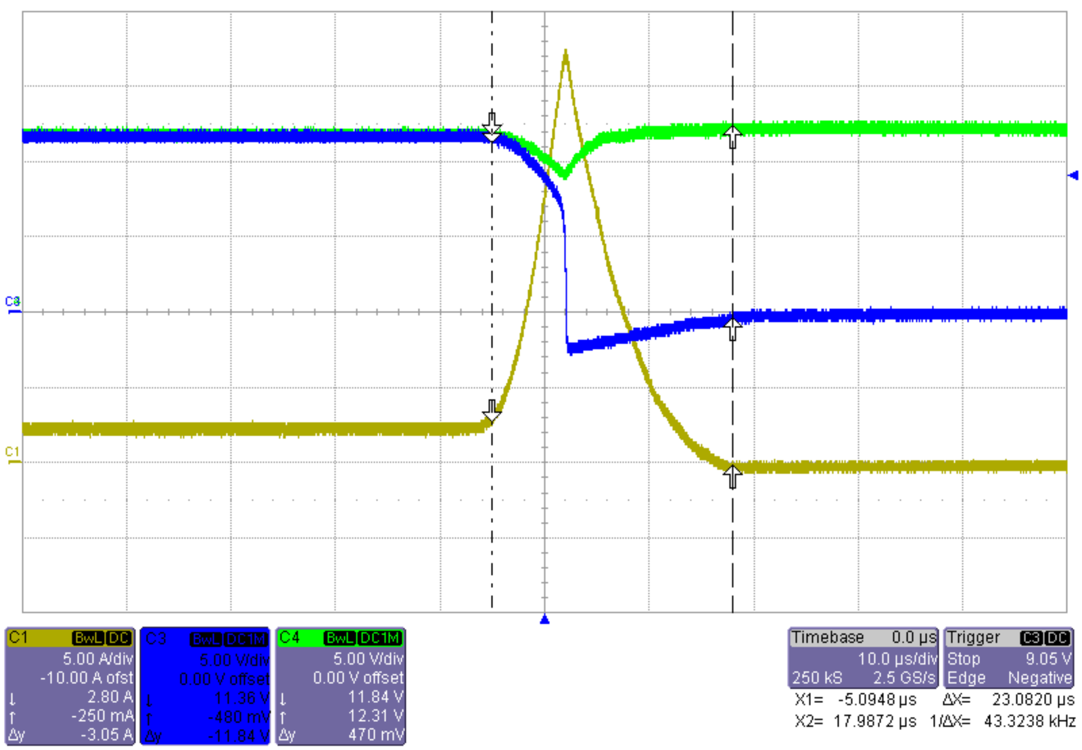


Figure 10. Load Switch Response to Short Circuit

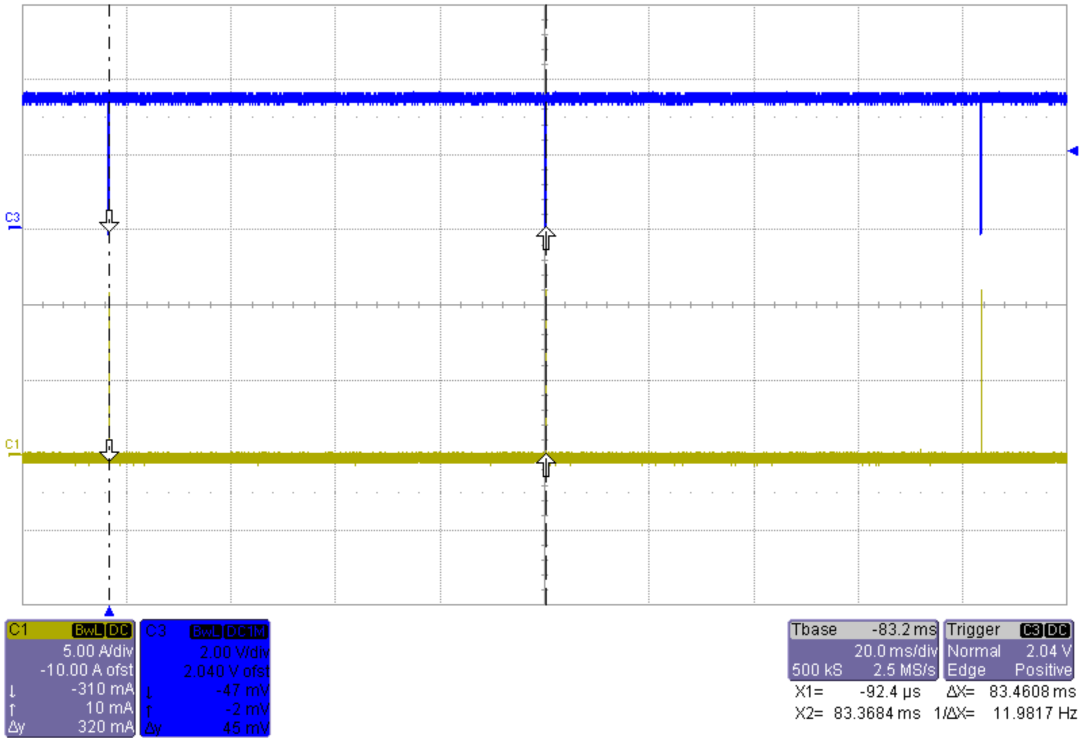


Figure 11. MSP430 Fast Trip Comparator Response to Load Short Circuit ($\overline{EN}$)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2014) to A Revision	Page

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