TEXAS INSTRUMENTS

Characteristics, Operation, and Use of the TLV571/TLV157x EVM

User's Guide

November 2000

AAP Data Conversion

SLAU025A

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the 10-bit TLV1571/1578 analog-to-digital converter (ADC) evaluation module.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—EVM Overview
- Chapter 2—Getting Started
- Chapter 3—User Configurations
- Chapter 4—Control Registers

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Chapter 1

EVM Overview

This chapter gives a general overview of the TLV1578/TLV1571/TLV571 evaluation module (EVM), and provides a general description of the features and functions that should be considered in using this module properly.

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1.1 System Block Diagram

The TLV1578/TLV1571/TLV571 EVM provides a practical platform for evaluating the following devices:

- TLV1578 10-bit, eight-channel data acquisition system
- TLV1571 10-bit, one-channel data acquisition system
- TLV571 8-bit, one-channel data acquisition system

The EVM supports two package styles as shown in Table 1–1.

Table 1–1. Package Styles Available

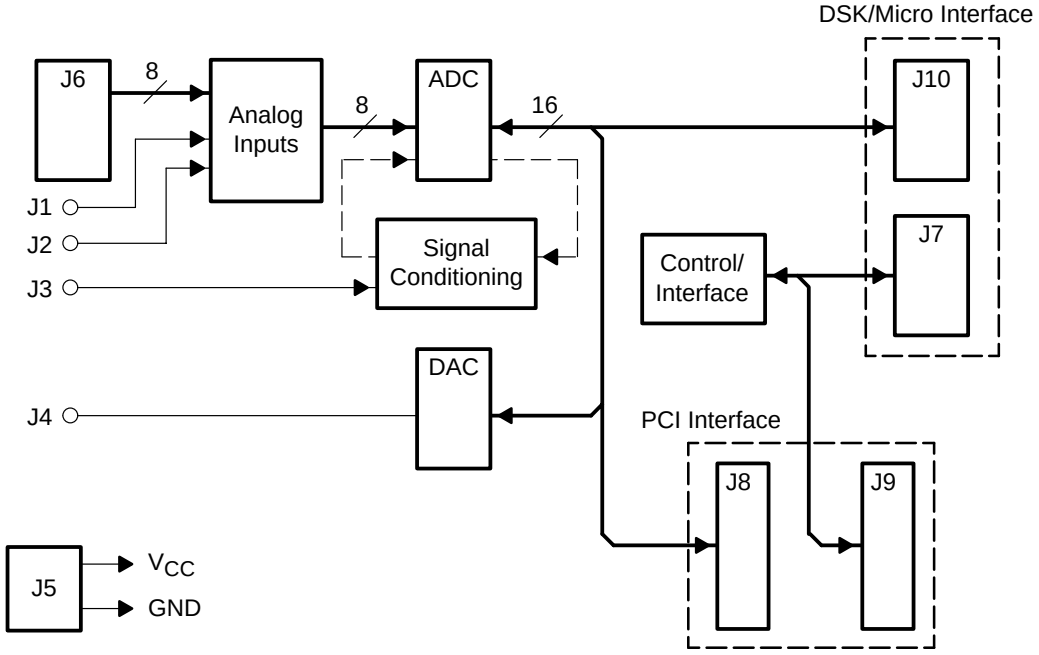
Device	DA Package† Supported?	DW Package‡ Supported?	PW Package§ Supported?
TLV1578	Yes, 32 pins	No	No
TLV1571	No	No	Yes, 24 pins
TLV571	No	No	Yes, 24 pins

† The DA package is a TSSOP device, with pins on a 0.65-mm pitch.
‡ The DW package is a small outline (SO) device, with pins on a 1.27-mm pitch.
§ The PW package is a TSSOP device, with pins on a 0.65-mm pitch.

The system block diagram is shown below. This illustration provides a general overview of the EVM. It is not meant to replace the circuit diagram, but to give a brief indication of the features and functions available. It should be read in combination with the circuit diagram supplied.

The elements of this block diagram are discussed in Figure 1–1.

Figure 1–1. Block Diagram



1.2 ADC System Discussion

This printed wiring board (PWB) EVM supports three analog-to-digital converters (ADCs).

- TLV1578
- TLV1571
- TLV571

From a physical and functional viewpoint, the significant distinction between these parts is that the TLV1578 features an 8–1 multiplexer (MUX). This allows selection of the analog-input channel to be digitized. The TLV1571 and TLV571 do not provide a MUX.

General features of these ADCs are given in Table 1–2.

Table 1–2. General ADC Features

Device	Resolution	Channels	Sweep Mode	Self-Test Output	Throughput at 5 V	Available Package	EVM Order Number
TLV1578	10 bit	8	Yes	Yes	1.25 MSPS	DA	TLV1578
TLV1571	10 bit	1	No	Yes	1.25 MSPS	DW/PW	TLV1571
TLV571	8 bit	1	No	No	1.25 MSPS	DW/PW	TLV571

1.2.1 ADC

This successive approximation scheme relies on charge redistribution to count and weigh each bit from MSB to LSB. Each bit of the ADC has a corresponding capacitor. The procedure involves successively comparing the charge on each capacitor to a reference value. As the process develops, the digital bit corresponding to each capacitor is either set or cleared.

1.2.2 DAC

A 12-bit digital-to-analog converter (DAC) present on the EVM can be used either as an independent device (via either the DSP starter kit (DSK) interface or the peripheral component interconnect (PCI) interface), or can be arranged to operate in synchronization with the ADC.

1.2.3 Signal Conditioning

Signal conditioning is available prior to conversion. The conditioning circuit consists of an operational amplifier in a noninverting configuration. The nominal gain for the circuit is one, but you can change it. The slew rate of the amplifier should be sufficiently high (25 V/μS) to respond to fast-changing signals such as square-wave inputs.

1.2.4 Control/Interface

The control signals can be derived from either a DSK/microprocessor or a dedicated PCI-based DSP. The signals from either source are the same. The decision regarding which host system to use is left to the discretion of the user.

1.3 EVM Operating Modes

There are three modes of operation for the EVM:

- Stand-alone mode
- DSK/Microprocessor mode
- PCI daughtercard

Each of these modes is discussed below.

1.3.1 Stand-Alone Mode

Upon power up, all the bits in both ADC control registers are cleared; this allows the ADC to immediately begin conversion from a known condition. The stand-alone mode is the minimal operating mode for the system. Conversions are automatic and do not require a host.

1.3.2 DSK/Microprocessor Mode

The DSP starter kit (DSK)/microprocessor mode supports parallel transfers via TI's range of DSK modules—'C54xDSKplus, 'C54xDSK, or the 'C203DSK. In general, any microprocessor that can provide basic address, data, and control signals can be interfaced to the EVM.

1.3.3 PCI Daughtercard

The EVM also supports the TMS320C6000 daughtercard specification. This specification introduces a standard physical and electrical interface to 'C6000 and 'C5000 systems integrated on a PCI card. The PCI local bus is a high-performance bus that provides a processor-independent data path between the CPU and high-speed peripherals.

1.4 Power and Cabling Requirements

The EVM dc supply voltage is 3 V to 5 V and should be set to approximately 3.3 V or 5.3 V, respectively. The power and externally applied reference voltage should be supplied to the EVM through shielded twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher-frequency digital circuitry.

1.5 PCA as Part of a System

1.5.1 Stand-Alone Mode

The stand-alone mode allows the ADC and DAC to operate without a host system. The following steps are required to achieve this:

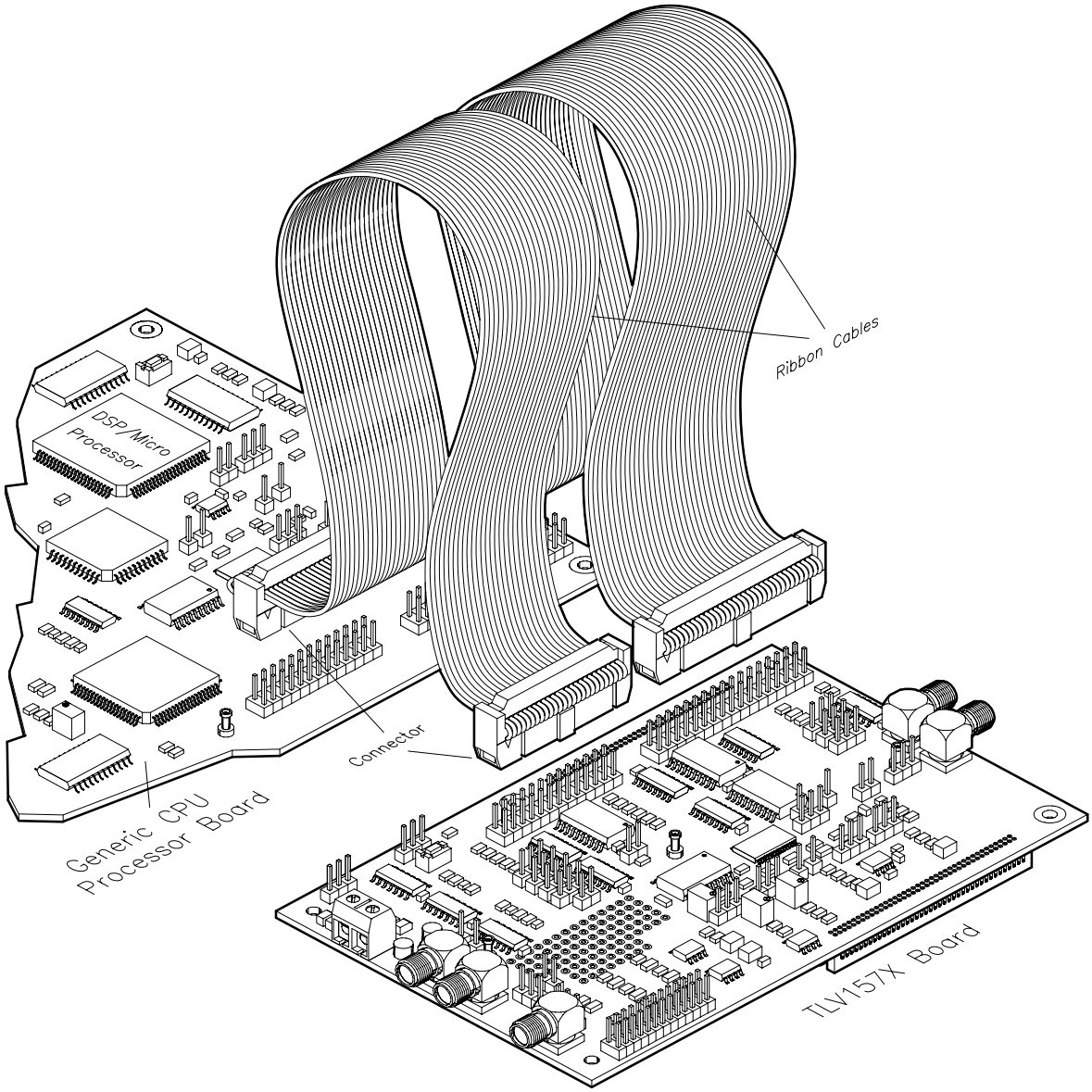
- ❑ Supply +5 V and ground via J5
- ❑ Jumper between pins 15 and 16 of J7
- ❑ Jumper between pins 19 and 20 of J7
- ❑ Jumper between pins 21 and 22 of J7
- ❑ Clip (or wire-wrap) a connection between TP3 and pin 13 of J7
- ❑ Remove W22 (located on the breadboard area)
- ❑ Supply and analog signal for conversion via J6 (ribbon cable) or J1 (BNC)
- ❑ Supply a convert signal via J11
- ❑ Jumper between pins 1 and 2 of W20
- ❑ Jumper between pins 1 and 2 of W6
- ❑ Initiate conversion by momentarily pressing SW1

Subsequent conversions occur automatically. No DSP or microprocessor is required.

1.5.2 DSK/Microprocessor Mode

In this mode the DSP supplies control and address signals via J7, and data via J10.

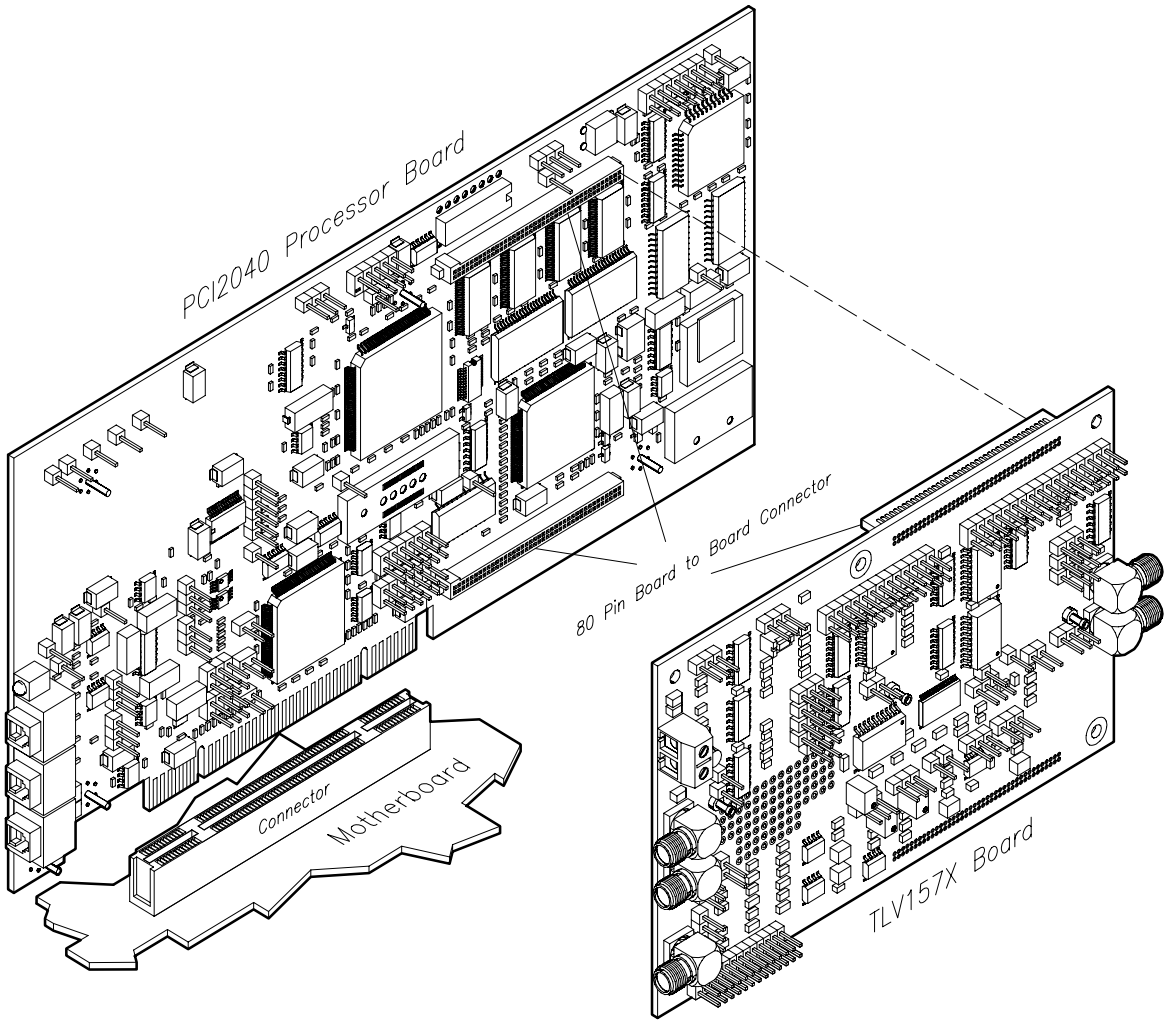
Figure 1–2. Mating of Connectors J7 and J10



1.5.3 PCI2040 ’C54x Mounting

In this mode, J8 and J9 mate directly to corresponding connectors in the motherboard card (see Figure 1–3).

Figure 1–3. Mounting the EVM on the PC12040



1.6 PCA Options Available

To ensure the flexibility of the printed-circuit board (PCB), three possible ADCs featured in this series are described in Table 1–3.

Table 1–3. Possible ADCs

ADC Part No.	No. of Channels	No. of Bits	Speed	EVM Order No.
TLV571	1	10	1.25 MSPS	TLV571
TLV1571	1	10	1.25 MSPS	TLV1571
TLV1578	8	10	1.25 MSPS	TLV1578

Ensure that the printed-circuit assembly (PCA) has the correct check mark on the silkscreen.

Each PCA may have additional hardware to install, if appropriate.

Chapter 2

Getting Started

This chapter describes the physical characteristics and PCB layout of the EVM, and lists the components used on the module.

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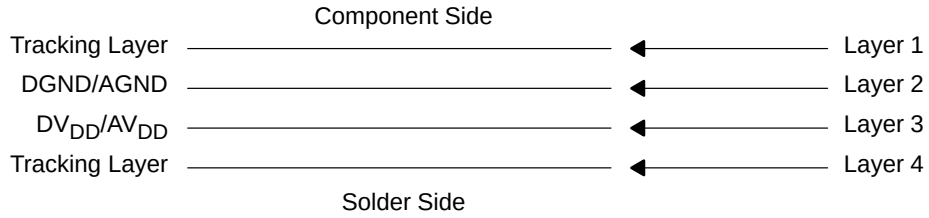
2.1 Physical Description

The PWB is constructed in four layers as shown in the following illustrations. The dimensions of the PWB are 5.25 in × 3.5 in (133.35 mm × 88.9 mm). See Figure 2–1.

Figure 2–1. PWB Layers



Figures 2–2 through 2–5 show the tracking for each layer.

Figure 2–2. Layer 1

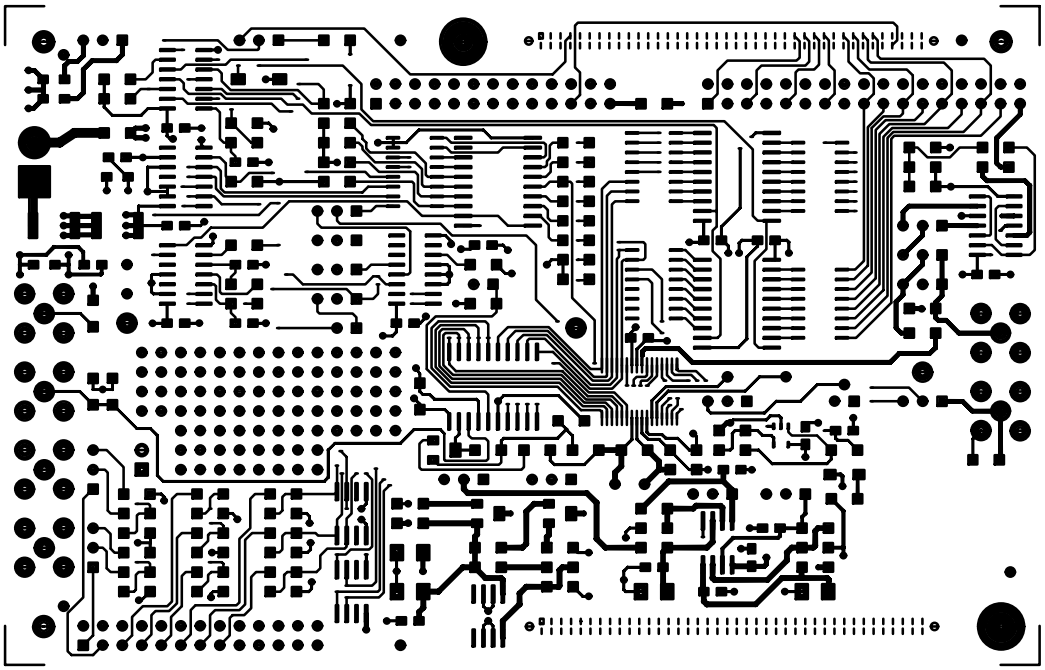


Figure 2–3. Layer 2

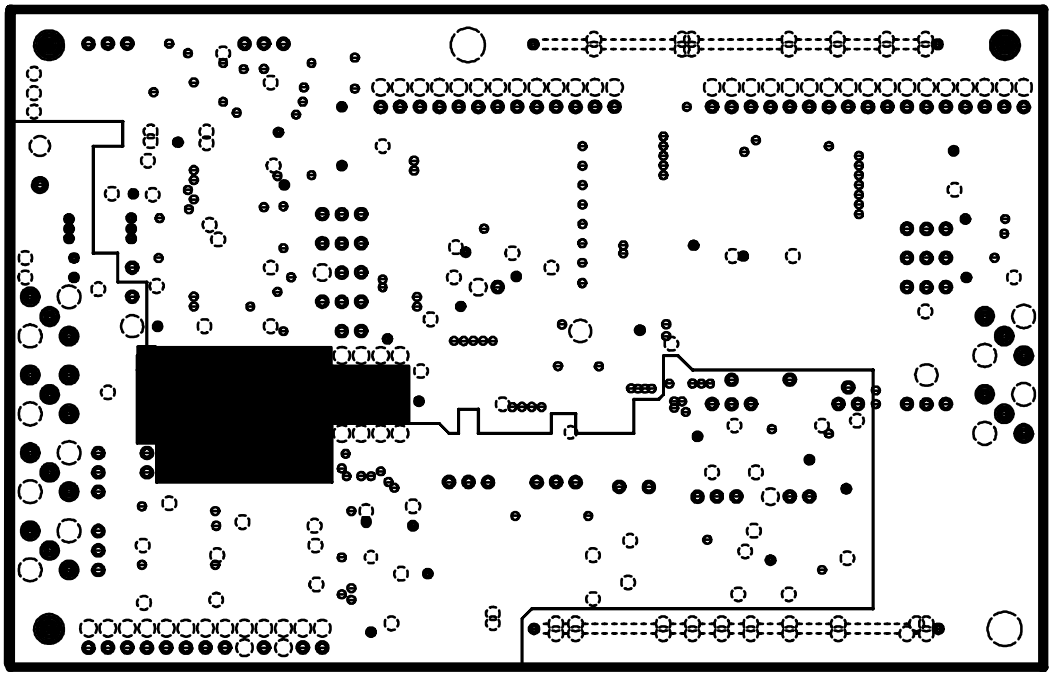


Figure 2–4. Layer 3

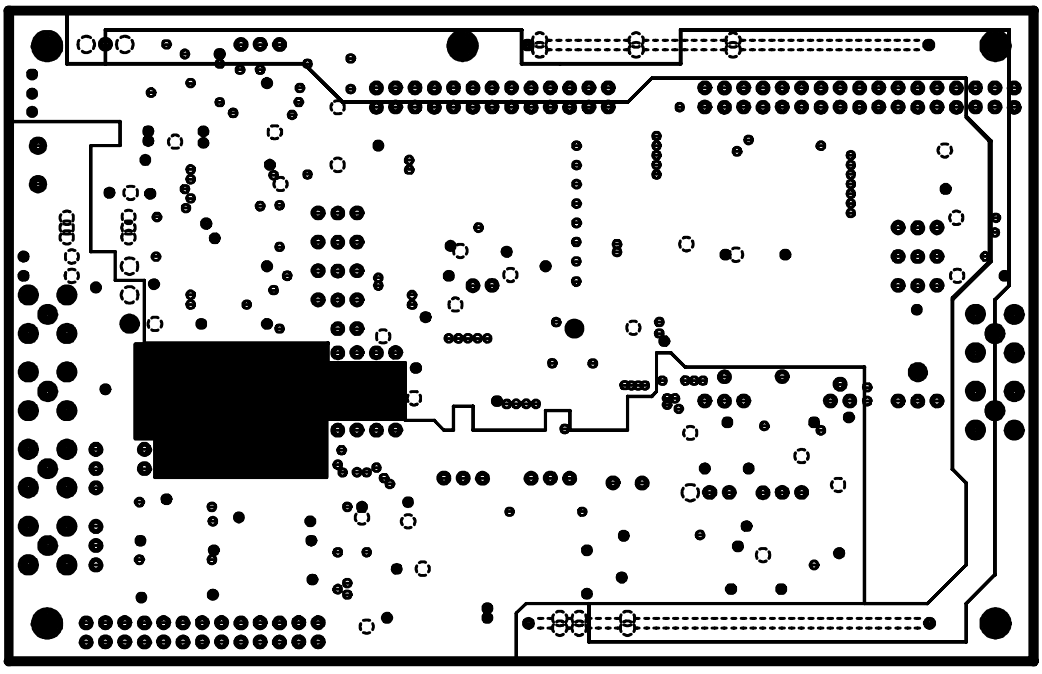
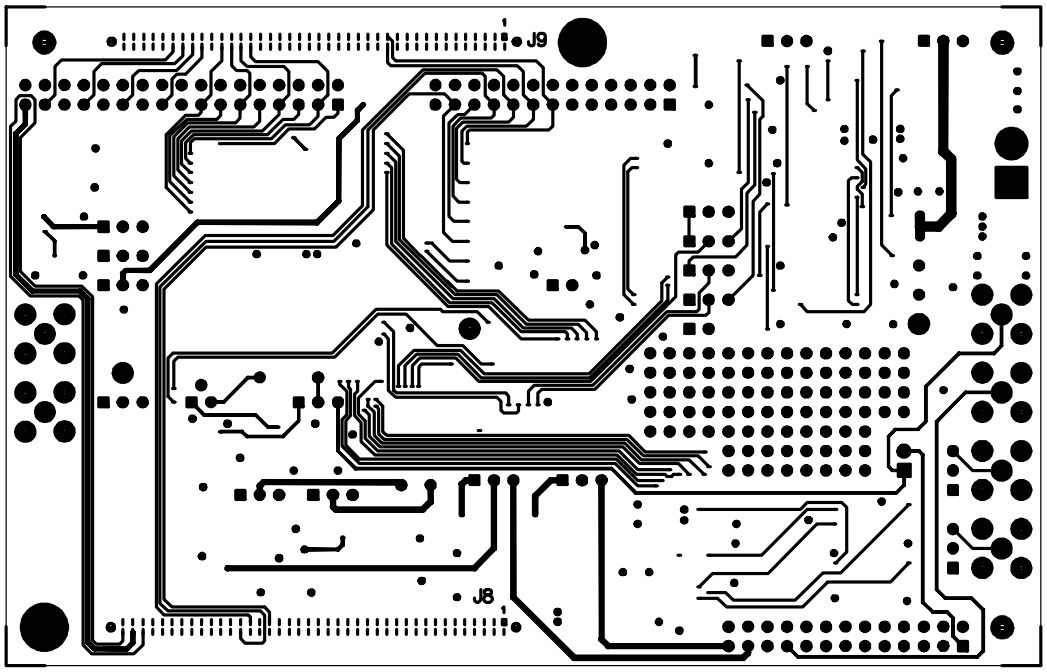
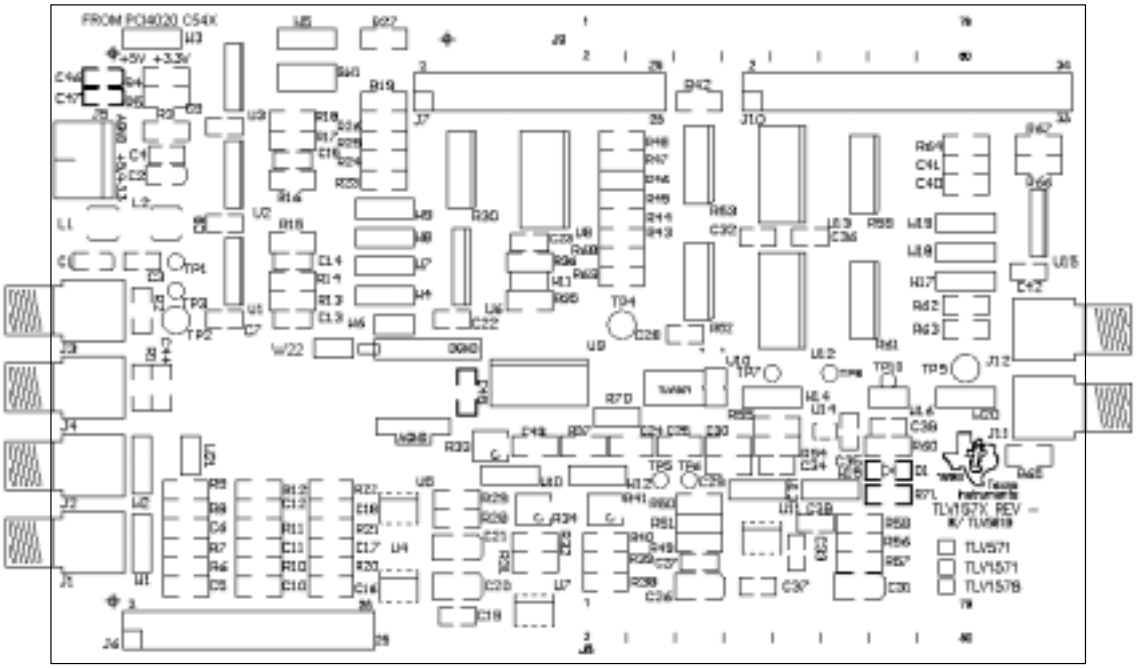


Figure 2–5. Layer 4



Note: This layer is the solder-side of the PCA and is shown reversed for clarity.

Figure 2–6. Silk Screen



2.2 Parts List

This table lists the parts required for the TLV571/TLV157x devices.

Table 2–1. Parts List for the TLV571/TLV157x Devices

Quantity			Value	Ref. Des.	Footprint	Description	Manufacturer	Part Number
571	1571	1578	PCB fabrication	N/A	N/A	TLV157X Rev – PCB fabrication	TBD	TLV157X
8	8	8	0.1 µF	C24 C25 C29 C30 C40 C41 C43 C45	1206	Ceramic, X7R, 50 V, 10%	Kemet	C1206C104K5RAC
16	16	16	0.1 µF	C19 C22 C23 C27 C28 C3 C32 C33 C35 C36 C37C4 C42 C7 C8 C9	805	Ceramic, X7R, 50 V, 10%	Kemet	C0805C104K5RAC
2	2	2	100 pF	C34 C38	805	Ceramic, COG, 50V, 2%	Kemet	C0805C101G5GAC
4	4	4	10 µF	C20 C21 C26 C31	3528	10 µF, 10 V, 10%, tantalum	Kemet	T491B106K010AS
1	1		1500 pF	C44	1206	Ceramic, X7R, 50 V, 10%	Kemet	C1206C152K5RAC
		9	1500 pF	C5 C6 C10 C11 C12 C16 C17 C18 C44	1206	Ceramic, X7R, 50 V, 10%	Kemet	C1206C152K5RAC
3	3	3	270 pF	C13 C14 C39	805	Ceramic, COG, 50 V, 2%	Kemet	C0805C271G5GAC
4	4	4	4.7 µF	C1 C2 C46 C47	3216	4.7 µF, 10 V, 10%, tantalum	Kemet	T491A475K010AS
1	1	1	560 pF	C15	805	Ceramic, COG, 50 V, 2%	Kemet	C0805C561G5GAC
1	1	1	GRN LED	D1	1206	Green, 20 mA, 1206 size	Chicago Miniature	CMD11-21VGC/TR8
2	2	2	26PIN_IDC	J6 J7	13X2X.1	26-pin header	Samtec	TSW-113-07-L-D
1	1	1	34PIN_IDC	J10	17X2X.1	34-pin header for IDC	Samtec	TSW-117-07-L-D
1	1	1	KRMZ2	J5	N/A	2-terminal screw connector	Lumberg	KRMZ2
4	4		RA-SMA_JACK	J3 J4 J11 J12	N/A	Right angle PCB mount SMA jack	Lighthorse Technologies	LTI-SALF54NT
		5	RA-SMA_JACK	J1 J3 J4 J11 J12	N/A	Right angle PCB mount SMA jack	Lighthorse Technologies	LTI-SALF54NT
2	2	2	TFM-140	J8 J9	N/A	80-pin 0.050” centers	Samtec	TFM-140-31-S-D-A
1	1	1	1.0 µH	L2	DO1608C	DO1608C Series–Coil Craft	Coil Craft	DO1608C-102
1	1	1	4.7 µH	L1	DO1608C	DO1608C Series–Coil Craft	Coil Craft	DO1608C-472
5	5	5	33 Ω X 8	R30 R52 R53 R59 R61	2NBS16	8-element – isolated resistor pack	Bourns	2NBS16-TJ1-330

Table 2–1. Parts List for the TLV571/TLV157x Devices(Continued)

Quantity			Value	Ref. Des.	Footprint	Description	Manufacturer	Part Number
4	4	4	0 Ω	R3 R39 R54 R70	1206	1206 chip res., 5%	Bourns	CR1206-FX-000
1	1	1	10	R60	1206	1206 chip res., 1%	Bourns	CR1206-FX-10R0
4	4	4	100	R13 R14 R15 R17	1206	1206 chip res., 1%	Bourns	CR1206-FX-1000
24			10K	R1 R4 R5 R16 R18 R19 R23 R24 R25 R26 R27 R35 R36 R49 R50 R51R56 R57 R58 R64 R68 R69 R72 R73	1206	1206 chip res., 1%	Bourns	CR1206-FX-1002
	22	22	10K	R1 R4 R5 R16 R18 R19 R23 R24 R25 R26 R27 R35 R36 R49 R50 R51R56 R57 R58 R64 R72 R73	1206	1206 chip res., 1%	Bourns	CR1206-FX-1002
1	1	1	1K	R32	1206	1206 chip res., 1%	Bourns	CR1206-FX-1001
3	3	3	2.49K	R29 R37 R38	1206	1206 chip res., 1%	Bourns	CR1206-FX-2491
10	10		33	R28 R42 R43 R44 R45 R46 R47 R48 R63 R66	1206	1206 chip res., 5%	Bourns	CR1206-FX-330
		18	33	R6 R8 R10 R11 R12 R20 R21 R22 R28 R42 R43 R44 R45 R46 R47 R48 R63 R66	1206	1206 chip res., 5%	Bourns	CR1206-FX-330
2	2	2	332	R40 R71	1206	1206 chip res., 1%	Bourns	CR1206-FX-3320
1	1	1	470	R67	1206	1206 chip res., 5%	Bourns	CR1206-FX-470
1	1	1	499	R31	1206	1206 chip res.,1%	Bourns	CR1206-FX-4990
3	3	3	5K POT	R33 R34 R41	32X4W	4 mm, 5T, SM potentiometer	Bourns	3214W-1-502-W
1	1	1	Panasonic EVQ-PJSO4K	SW1	EVQ-PJ	Momentary push button	Panasonic	EVQ-PJ
3	3	3	Test point	TP2 TP4 TP9	N/A	Turret type test point	Cambion	180-7337-02-05
7	7	7	Test point	TP1 TP3 TP5 TP6 TP7 TP8 TP10	N/A	Test point – single 0.025” Pin	Samtec	TSW-101-07-LS
1	1	1	SN74AHC04	U1	14-SOP(D)	Hex inverter	Texas Instruments	SN74AHC04D

Table 2–1. Parts List for the TLV571/TLV157x Devices (Continued)

Quantity			Value	Ref. Des.	Footprint	Description	Manufacturer	Part Number
1	1	1	SN74AHC08	U3	14-SOP(D)	Quad NAND gate	Texas Instruments	SN74AHC08D
1	1	1	SN74AHC138	U6	16-SOP(D)	3–8 LINE DEC/DEMUL	Texas Instruments	SN74AHC138D
2	2	2	SN74AHC245	U12 U13	20-SOP(DW)	Octal bus trans-ceiver, 3-state	Texas Instruments	SN74AHC245DW
1	1	1	SN74AHC32	U2	14-SOP(D)	Quad 2-Input positive OR gate	Texas Instruments	SN74AHC32D
1	1	1	SN74AHC541	U8	20-SOP(DW)	Octal buffer and driver	Texas Instruments	SN74AHC541DW
1	1	1	SN74AHC74	U15	14-SOP(D)	Dual D-type FF	Texas Instruments	SN74AHC74D
1	1	1	TL1431	U7	8-SOP(D)	Precision programmable reference	Texas Instruments	TL1431CD/ TL1431QD
		2	TL7726	U4 U5	8-SOP(D)	Hex clamp circuit	Texas Instruments	TL7726CD/TL7726ID /TL7726QD
1			TLV571	U10	24-PW	8-bit single channel ADC	Texas Instruments	TLV571CPW/ TLV571IPW
	1		TLV1571	U10	24-PW	10-bit single channel ADC	Texas Instruments	TLV1571CPW/ TLV1571IPW
		1	TLV1578	U10	32-DA	10-bit eight channel ADC	Texas Instruments	TLV578CDA/ TLV578IDA
1	1	1	TLV2771	U14	5-SOT(DBV)	Low-power single op amp	Texas Instruments	TLV2771IDBV/ TLV2771CDBV
1	1	1	TLV2772	U11	8-SOP(D)	Dual op amp in 8-pin SOP package	Texas Instruments	TLV2772ID/ TLV2772AID/ TLV2772CD/ TLV2772AMD
1	1	1	TLV5619	U9	20-SOP(DW)	12-bit parallel DAC	Texas Instruments	TLV5619CDW/ TLV5619IDW
4	4		Shunt jumper	W11 W6 W16 W21, W22	2pos_jump	2-position jumper 0.1” spacing	Samtec	TSW-102-07-LS
		3	Shunt jumper	W11 W6 W16	2pos_jump	2-position jumper 0.1” spacing	Samtec	TSW-102-07-LS
17	17	17	2-way shunt jumper	W1 W2 W3 W4 W5 W7 W8 W9 W10 W12 W13 W14 W15 W17 W18 W19 W20	3pos_jump	3-position jumper 0.1” spacing	Samtec	TSW-103-07-LS
Customer-Installed Options								
5	5	5	49.9	R2 R7 R9 R62 R65	1206	1206 chip res., 1%	Bourns	CR1206-FX-49R9
1	1	1	SIT	R55	1206	1/4W 1206 chip resistor	Any	
1	1	1	RA – SMA	J2	RA_SMA_JACK	Right angle PCB mount SMA jack	Amphenol	901-143-3

Note: Manufacturer and part number data is supplied for reference only. Substitutions are permissible on all but TI parts.

Chapter 3

User Configurations

This chapter describes the user-definable options.

Topic **Page**

3.1 Schematic Diagram

Figure 3–1 illustrates the EVM schematic.

Figure 3–1. EVM Schematic Diagram

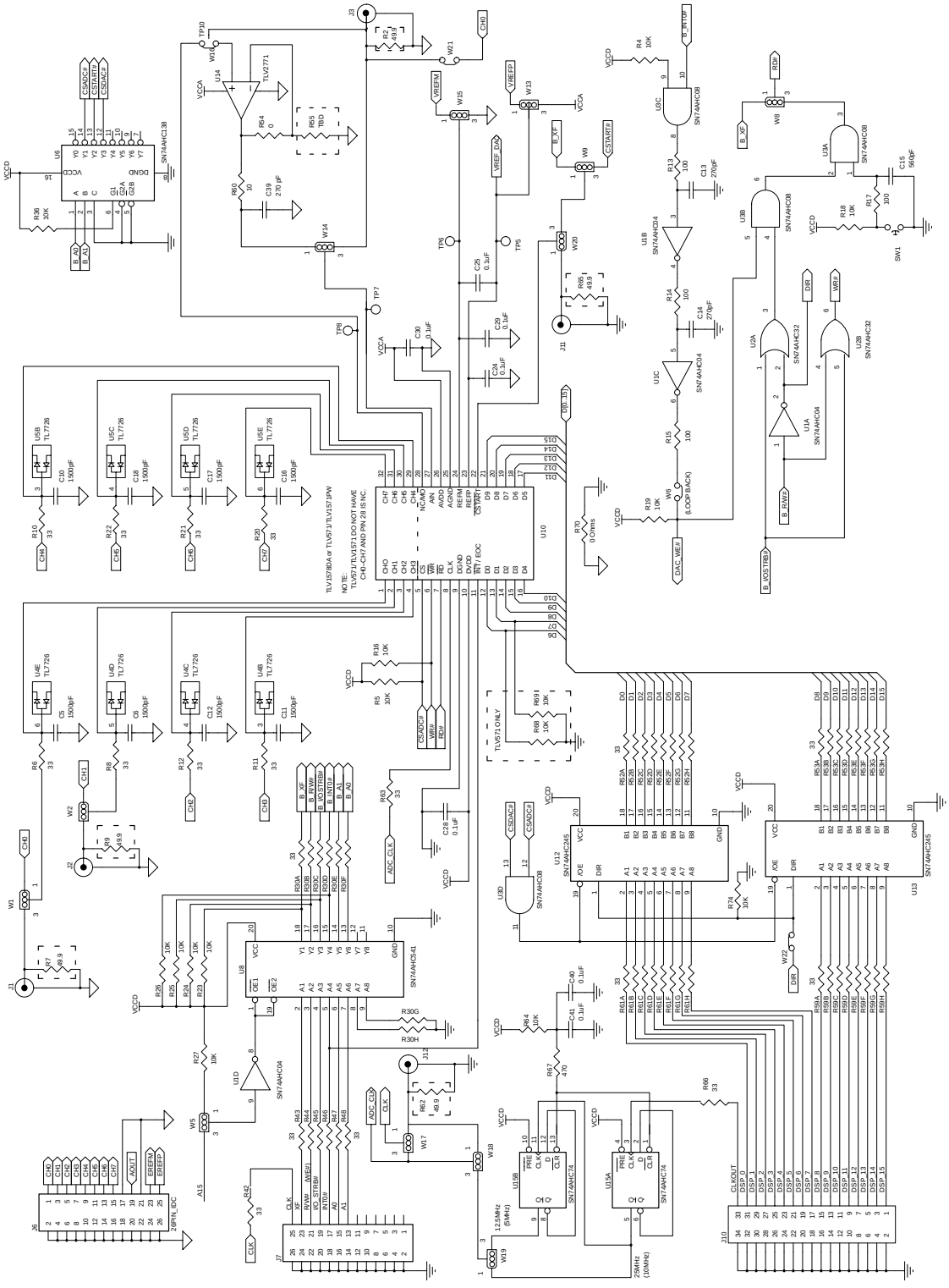
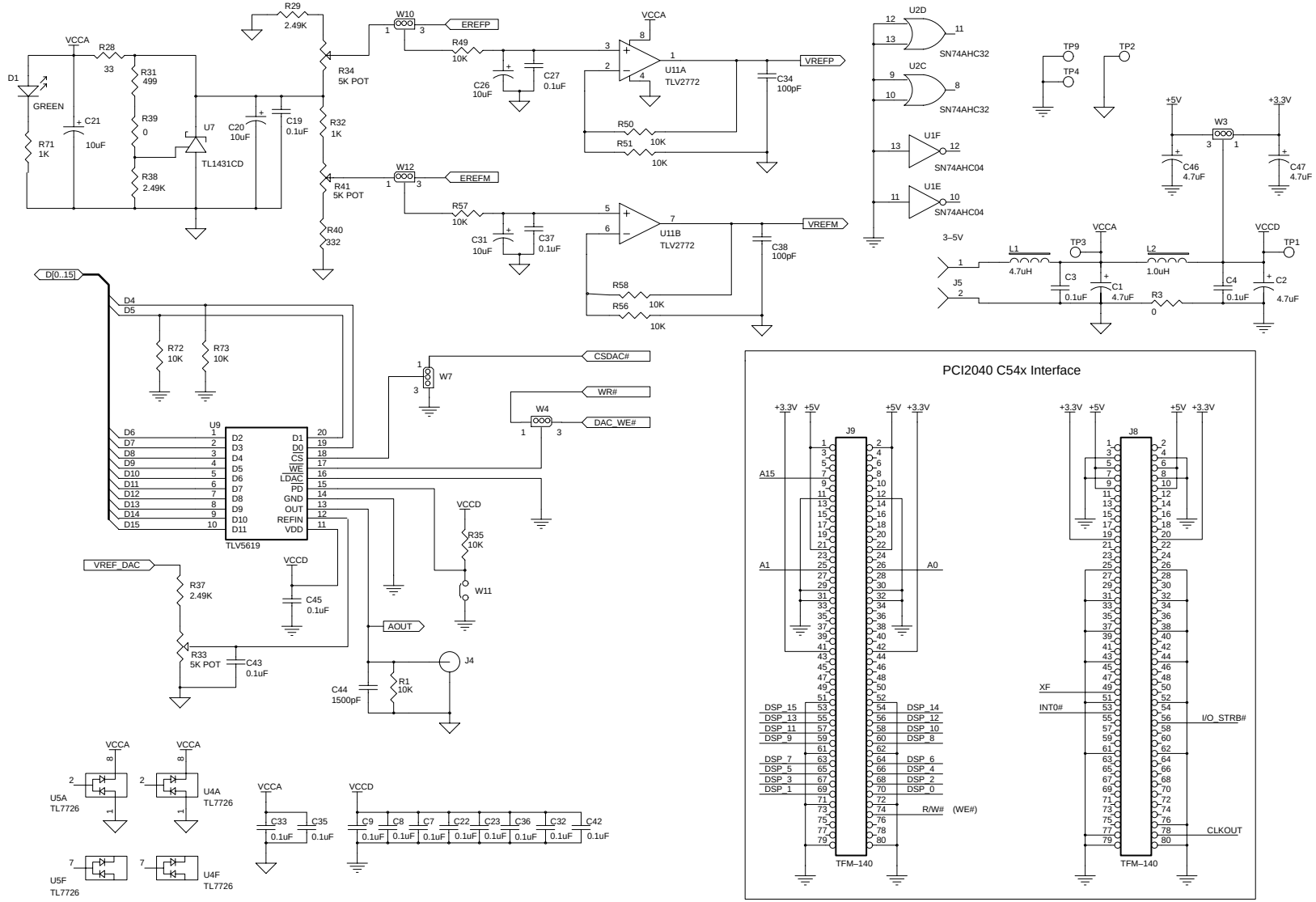


Figure 3–1. EVM Schematic Diagram (Continued)



3.2 User Options

The PCA ships in a state that enables immediate evaluation of the analog-to-digital converter (ADC). However, you can reconfigure various options through hardware. This chapter discusses these options to ensure that any reconfiguration is conducted properly.

The hardware on the PCA falls into various groups:

- 18 jumpers
- 4 wire links
- 2 resistors
- 1 momentary push switch

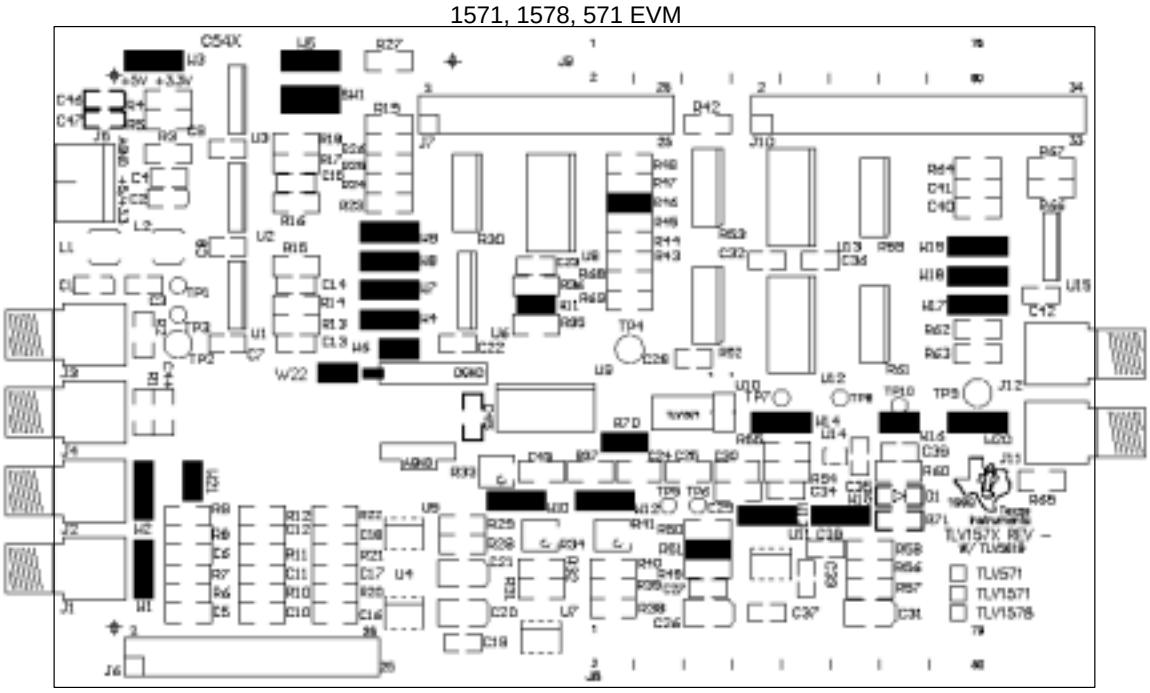
Table 3–1 lists jumper options, a brief description of each function, and information on where the option can be found.

Table 3–1. Jumper Functions

Jumper Reference	Function Description	Section	Comment
W1	Ch 0 input	3.4.2	
W2	Ch 1 input	3.4.2	
W3	Selects 5-V or 3.3-V operation	3.3	
W4	Configure for ADC loopback	3.7.1.2	
W5	Maps PCA address	3.6	
W6	Provides $\overline{WR}$ to DAC in loopback mode	3.7.1.2	Wire link
W7	Loopback mode—provides $\overline{CS}$ to DAC	3.7.1.2	
W8	Stand-alone mode Provides $\overline{RD}$ signal to ADC	3.7.1.1 3.7.1.2	
W9	Selects an internal start conversion signal	3.7.2	
W10	Select internal or external voltage reference	3.5	
W11	Loopback mode—maintains DAC in nonpower-down mode	3.7.1.2	Wire link
W12	Select internal or external voltage reference	3.5	
W13	Provides positive reference voltage to ADC	3.5	
W14	Supplies signal to ADC for conversion	3.4.2	
W15	Provides negative reference voltage to ADC	3.5	
W16	Selects input to gain stage amplifier	3.4.2	Wire link
W17	ADC clock Select external or internal clock	3.8.2 3.8.3	
W18	Select ADC clock	3.8.2 3.8.3	
W19	Select internal clock speed	3.8.2 3.8.3	
W20	Selects internal or external conversion	3.7.2	
W21	Connects CH0 to J3 and W14	3.4.2	Wire link
W22	Supports stand-alone mode	3.4.2	

Figure 3–2 indicates the physical locations of this hardware.

Figure 3–2. Reconfiguration Hardware Location



3.3 Analog Supply Voltage

Two options supply power to the analog section of the EVM:

- 5 V
- 3.3 V

Select either option via jumper W3 in accordance with the following tables.

Table 3–2. Analog Voltage Supply Configuration Options

Jumper W3	Pins 1 and 2	Pins 2 and 3
3.3-V operation	Jumper installed	Jumper not installed
5-V operation	Jumper not installed	Jumper installed

3.4 Analog Input Configurations

A variety of options are available to configure the analog inputs. This section describes these options, along with the jumper settings required.

The two alternatives for the analog inputs are given in the following table.

Table 3–3. Analog Input Options

Analog Input Option	Connector Reference and Type	
	IDC	SMA
Apply signal to ADC multiplexer	J6 – 2 x 13 plug	J1
		J2
Apply signal direct to converter		J3

The user can select various configurations within each of these options. These are discussed below.

3.4.1 Apply to ADC Multiplexer (TLV1578 Only)

Eight possible analog inputs are provided via connector J6. Section 3.9 *Connects Pin and Function Assignments,* gives the pin assignments for J6.

3.4.2 Direct Connect (TLV1578 Only)

Analog inputs can also be taken directly from SMA connectors J1 (for channel 0), and J2 (for channel 1).

In this configuration the user should remove the respective jumper on pins 1 and 2 and replace on pins 2 and 3.

Figure 3–3. Direct Connect Jumper Configuration for TLV1578

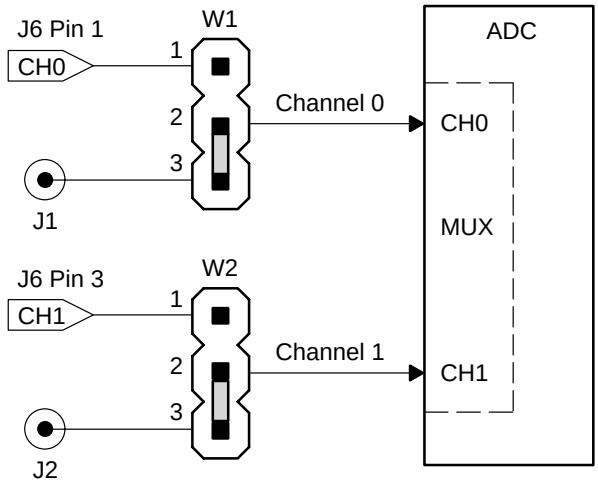


Table 3–4. Shipping Condition of Jumpers W1 and W2

Jumper	Pins 1 and 2	Pins 2 and 3
W1	Jumper not installed	Jumper installed
W2	Jumper installed	Jumper not installed

3.4.3 Apply Direct to Signal Conditioning (TLV1578)

The MUX output of the TLV1578 does not have an internal connection to the ADC. This output is available in case you want to provide some signal conditioning prior to conversion.

There are three options when supplying a direct signal:

- ❑ As the output of the MUX
- ❑ Via IDC J6 pin 1
- ❑ Via J3, the surface-mounted BNC

When applying a signal via J3, clamping of the input voltage will be possible only if W1 is jumpered from 1 to 2 and W21 is intact.

This signal conditioning consists of an op amp configured as a voltage follower with a nominal gain of 1. Alternate values for R54 and R55 affect the gain of this amplifier, as shown by the following expression:

$$G = 1 + \left(\frac{R54}{R55}\right)$$

The configuration for this conditioning circuit is selected via wire links and a jumper, as shown in the following illustration.

Figure 3–4. Gain Circuit Selection

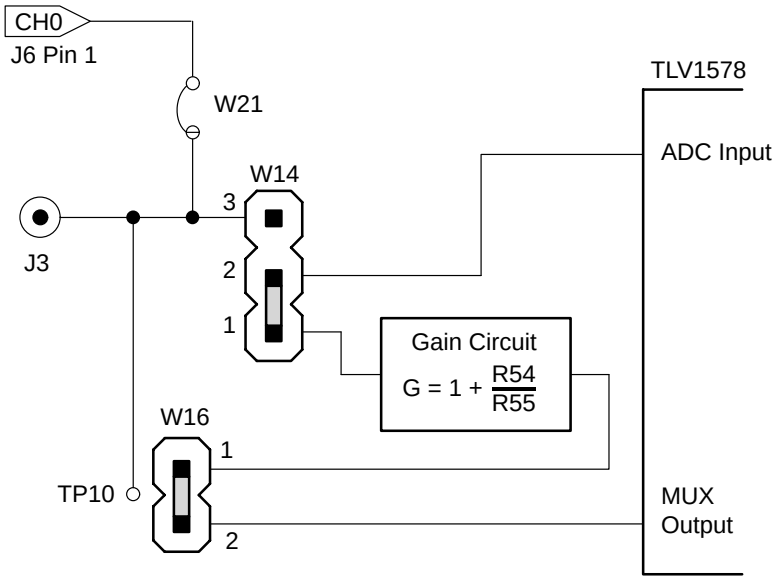


Table 3–5. TLV1578 Shipping Condition

TLV1578 Shipping Condition			
Reference	**Description**	**Position 1 – 2**	**Position 2 – 3**
W14	Selects input signal to ADC Gain circuit output External input via J3 or channel 0 via W21	Installed	Not installed
W16	Link selects input for signal conditioning Multiplexer output External input via J3 or channel 0 via W21	Installed	
W21	Link connects channel 0 to J3 / W14 / W16	Installed	
R54	0 Ω	Installed	
R55	N/A	Not installed	

3.4.4 Apply Direct to Signal Conditioning (TLV1571/TLV571)

Because the TLV1571 and TLV571 do not possess internal multiplexers, the configuration to allow an analog input signal to use the onboard signal conditioning circuit is slightly different, as illustrated in the following figure.

Figure 3–5. Onboard Signal Conditioning Circuit for TLV1571/TLV571

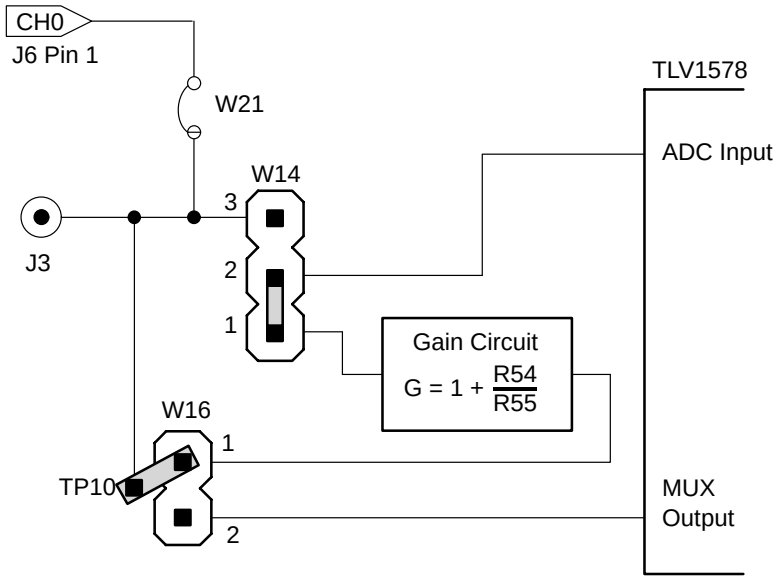


Table 3–6. TLV1571/571 Shipping Condition

Reference	Description	Position 1 – 2	Position 2 – 3
W14	Selects input signal to ADC	Installed	Not installed
W16	Link selects input for signal conditioning Multiplexer output External input via J3 or channel 0 via W21	Install jumper between TP10 and pin 1 of W16	
W21	Link connects channel 0 to J3 / W14 / W16	Installed	
R54	0 Ω	Installed	
R55	N/A	Not installed	

3.5 Generating a Voltage Reference

Two options provide the voltage reference:

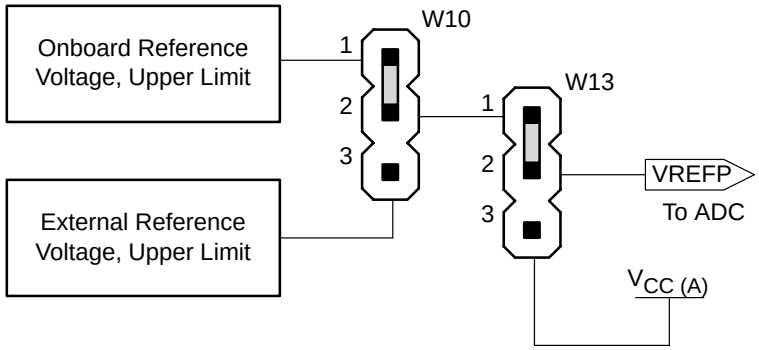
- ❑ Onboard reference (preferable)
- ❑ External reference

3.5.1 Onboard Reference

To set the onboard upper and lower reference voltage, use the jumper configuration shown in Figure 3–6.

Figure 3–6. Onboard Reference Voltage

(a) Upper Limit



To set the onboard lower reference voltage, the user should follow the jumper configuration shown in the following figure.

(b) Lower Limit

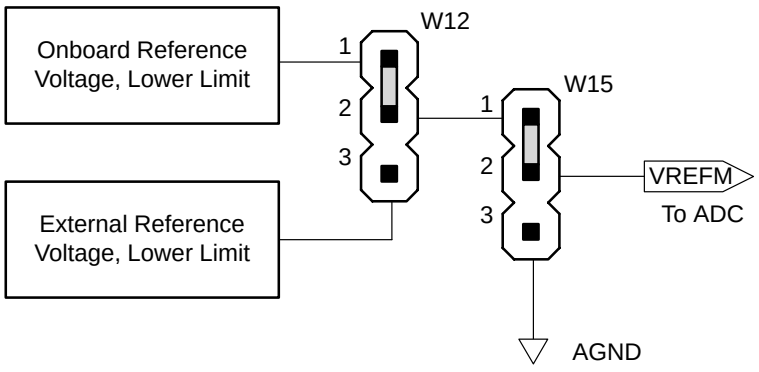


Table 3–7. Shipping Condition for VEREFP and VREFM

Jumper	Pins 1 and 2	Pins 2 and 3
VREFP setting		
W10	Jumper installed	Jumper not installed
W13	Jumper installed	Jumper not installed
VREFM setting		
W12	Jumper installed	Jumper not installed
W15	Jumper installed	Jumper not installed

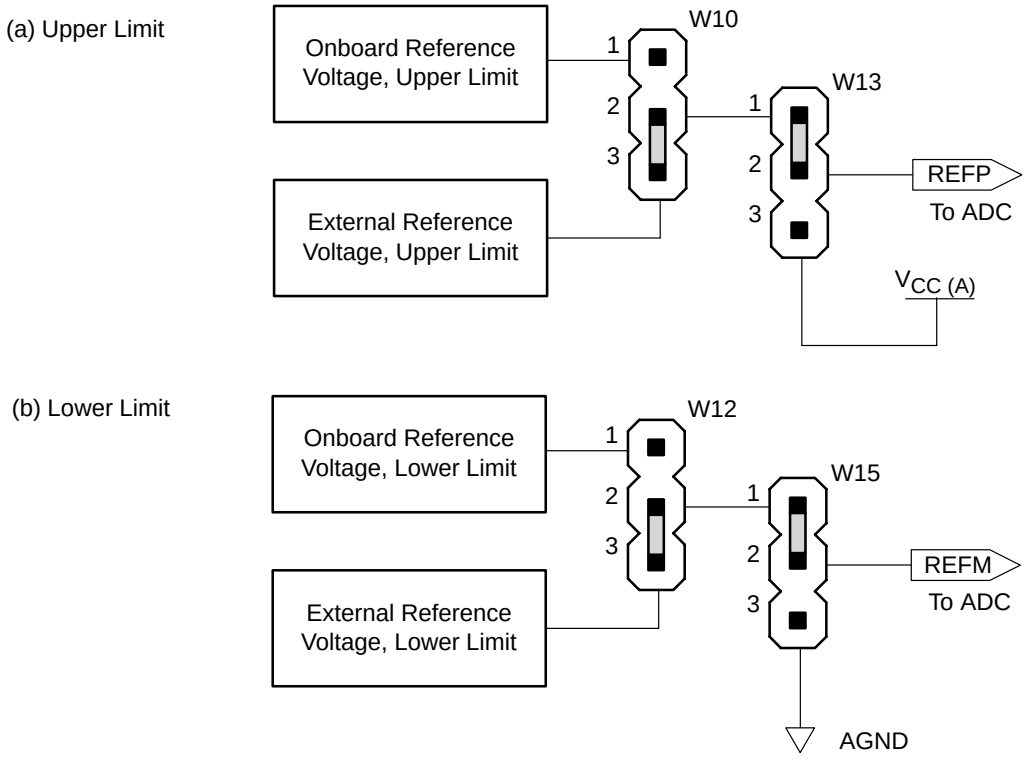
3.5.2 External Reference

It is important to understand that the reference voltage plays a fundamental part in the conversion process. Changes in the value of the reference voltage are reflected in the full-scale range of the device. The variation in voltage for the reference should, ideally, contribute less than 1/2 an LSB of error to the total conversion process.

External reference voltages can be supplied via J6; see Section 3–9 *Connector Pin and Function Assignments* for pinout details. The jumper configuration for this option is given in the following figure.

Under no circumstance should the external voltage exceed the supply voltage by more than 0.3 V.

Figure 3–7. External Reference Voltage



3.6 Host Interface Selection

Two operating modes are available for this EVM, as described in Chapter 2, *Getting Started*. After deciding the operating mode for the EVM, confirm the setting for jumper W5.

If the EVM is mounted on the PCI2040 (C5410) EVM, or on the C5402DSK, the control signals and the internal ADC and DAC registers are accessible by setting a jumper across pins 2 and 3 of W5.

If the EVM is to be used as a stand-alone with an alternate DSP or microprocessor host (for example the ‘C54x DSKplus, ‘C203 DSP EVM, or the ‘C3x DSK), the control signals and ADC and DAC registers are accessed by setting a jumper across pins 1 and 2 of W5.

Table 3–8. Host Interface Jumpers Shipping Condition

Jumper	Pins 1 and 2	Pins 2 and 3
W5	Jumper installed	Jumper not installed

3.7 Conversion Modes

The ADC provides two sampling/conversion methods—software mode and hardware mode. This section presents the user configuration options.

Table 3–9. Device Select/Conversion Start (CSTART) Select

DSP Address Line		Function
A1	A0	
0	0	
0	1	$\overline{\text{CSTART}}$
1	0	$\overline{\text{CSADC}}$
1	1	$\overline{\text{CSDAC}}$

3.7.1 Software Mode

Software mode is selected by setting the CR0 bit 7 of the ADC to 1. Control of conversions is managed by the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals.

In this mode, the system can operate either in stand-alone or in loopback mode. The stand-alone mode is the shipping configuration; this allows you to immediately begin evaluation.

3.7.1.1 Stand-Alone Mode

A pulse initiates stand-alone mode. You supply the pulse by momentarily pressing SW1. The ADC handles subsequent conversions automatically.

Table 3–10. Stand-Alone Mode Configuration

Jumper	Pins 1 and 2	Pins 2 and 3
W8	Jumper not installed	Jumper installed
SW1	Initiate *first* conversion	

3.7.1.2 Loopback Mode

Loopback mode permits the ADC and DAC to operate synchronously. The jumper conditions are shown in the following table.

Table 3–11. Loopback Mode Configuration

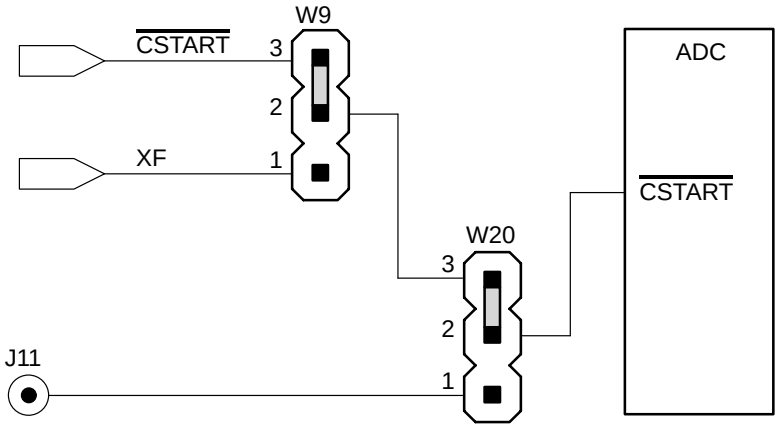
Jumper	Pins 1 and 2	Pins 2 and 3
W4	Jumper not installed	Jumper not installed
W6	Installed	
W7	Jumper not installed	Jumper installed
W8	Jumper not installed	Jumper installed
W11	Not installed	
J4	Analog output	
SW1	Initiate *first* conversion	

3.7.2 Hardware Mode

Hardware mode is selected by setting the CR0 bit 7 of the ADC to 0. In this mode, conversion control is handled by the $\overline{\text{CSTART}}$ signal. This is illustrated in Figure 3–8.

$\overline{\text{CSTART}}$ can be generated from one of three sources and is supplied directly to the ADC.

Figure 3–8. Hardware Mode



3.7.2.1 $\overline{\text{CSTART}}$

$\overline{\text{CSTART}}$ is generated by a dummy access (read or write) to address XX...XX3h.

Jumper	Pins 1 and 2	Pins 2 and 3
W9	Jumper not installed	Jumper installed
W20	Jumper not installed	Jumper installed

3.7.2.2 XF0

$\overline{\text{CSTART}}$ is generated by the DSP signal XF0.

Jumper	Pins 1 and 2	Pins 2 and 3
W9	Jumper installed	Jumper not installed
W20	Jumper not installed	Jumper installed

3.7.2.3 External Trigger

$\overline{\text{CSTART}}$ is generated externally.

Jumper	Pins 1 and 2	Pins 2 and 3
W9	Don’t care	
W20	Jumper installed	Jumper not installed
J11	Feed external signal in via this connector.	

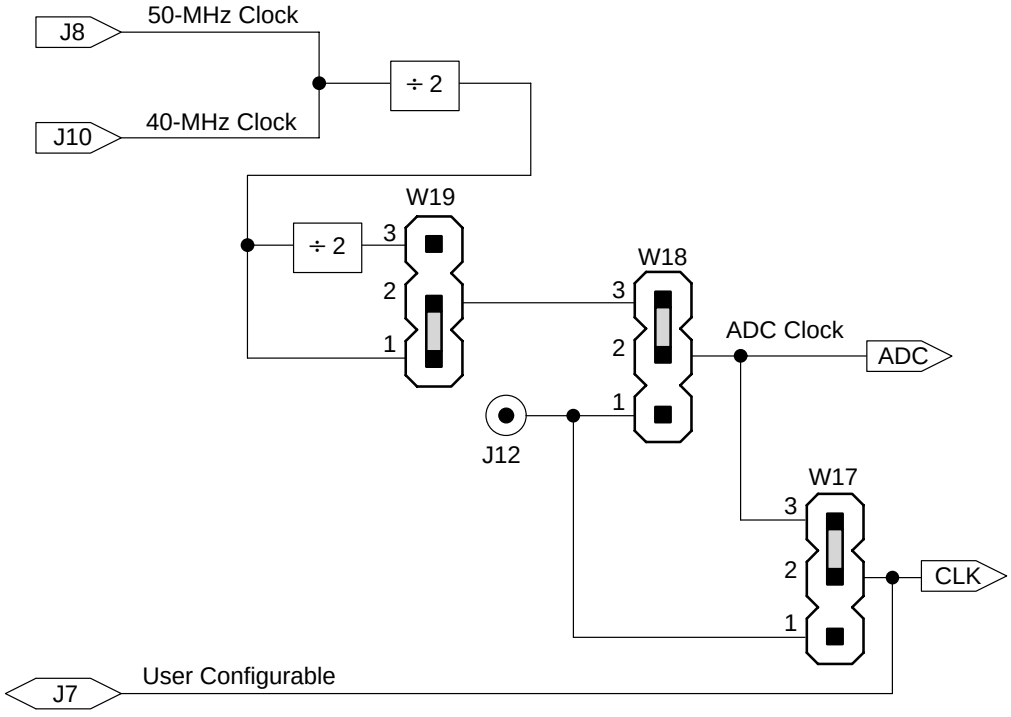
3.8 ADC Clock

The ADC requires an internal or external clock. Various possible external sources for the clock are required by the ADC. The choices are simple and are discussed in the following sections.

3.8.1 External Clock Generation

The maximum operational speed of the ADC is 20 MHz when it operates from a Vcc supply of 5 V, or 10 MHz at 3.3 V. This clock signal derives from three possible sources: in stand-alone configuration from J10 or J7; otherwise, from J8 when mounted on a PCI2040 EVM or ’C5402 DSK.

Figure 3–9. External Clock Signal



3.8.2 DSK/Microprocessor Mode (’C54x DSKplus, ’C203 EVM, ’C3x DSK)

Two configurations are available. On the preferred mode of operation in a stand-alone configuration, the clock signal is present on J10. The clock frequency, via the ’C54x DSK adapter board, is set at 40 MHz. This frequency is too fast for the ADC. To provide an acceptable frequency, the EVM divides the input clock.

You can decide if the clock frequency required is 20 MHz or 10 MHz and set the jumper positions accordingly.

Table 3–12. Stand-Alone Selection, 20 MHz

Jumper	Pins 1 and 2	Pins 2 and 3
W17	Jumper not installed	Jumper installed
W18	Jumper not installed	Jumper installed
W19	Jumper installed	Jumper not installed

Table 3–13. Stand-Alone Selection, 10 MHz

Jumper	Pins 1 and 2	Pins 2 and 3
W17	Jumper not installed	Jumper installed
W18	Jumper not installed	Jumper installed
W19	Jumper not installed	Jumper installed

In stand-alone mode, you may choose to supply the ADC clock externally. In this case, you are responsible for ensuring that the frequency of the clock meets the ADC specifications, and apply the clock signal via J12.

Table 3–14. Stand-Alone Selection External Clock

Jumper	Pins 1 and 2	Pins 2 and 3
W17	Jumper installed	Jumper not installed
W18	Jumper installed	Jumper not installed

3.8.3 PCI2040 and ’C5402 DSK Configuration

When the EVM mates to the PCI2040 card or ‘C5402 DSK, the clock signal is present on J8. The clock frequency, via the PCI2040 card or ‘C5402 DSK, is set at 50 MHz. This frequency is too fast for the ADC. To provide an acceptable frequency, the EVM divides the input clock. You must select both division elements to derive an appropriate ADC frequency.

Table 3–15. PCI2040 EVM ’C5402 DSK Selection, 12.5 MHz

Jumper	Pins 1 and 2	Pins 2 and 3
W17	Jumper not installed	Jumper installed
W18	Jumper not installed	Jumper installed
W19	Jumper not installed	Jumper installed

3.8.4 Synchronizing the EVM

Regardless of whether the EVM mates onto a PCI 2040, the ‘C5402 DSK, or is stand-alone, the clock can be synchronized with other equipment via J12 and/or J7 by choosing the appropriate jumper positions.

3.9 Connector Pin and Function Assignments

This section details the pinouts and functions for all user connectors.

Table 3–16. Connector Pin and Function Assignments

Reference Designator	Function
J1	Input signal applied to MUX Channel 0
J2	Input signal applied to MUX Channel 1
J3	Input signal applied directly to ADC
J4	Output signal from DAC

Table 3–17. J5 Power Connector

Pin Number	Function
1	Power 3 V – 5 V
2	AGND

Table 3–18. J6 Analog Signal Connector

Pin Number	Function	Pin Number	Function
1	Channel 0	2	AGND
3	Channel 1	4	AGND
5	Channel 2	6	AGND
7	Channel 3	8	AGND
9	Channel 4	10	AGND
11	Channel 5	12	AGND
13	Channel 6	14	AGND
15	Channel 7	16	AGND
17	Ground (signal)	18	AGND
19	Analog Output	20	AGND
21	Ground (signal)	22	AGND
23	External ref. lower	24	AGND
25	External ref. upper	26	AGND

Table 3–19. J7 DSK/Microprocessor Control Connector

Pin Number	Function	Pin Number	Function
1	Not connected	2	Ground (digital)
3	Not connected	4	Ground (digital)
5	Not connected	6	Ground (digital)
7	Not connected	8	Ground (digital)
9	Not connected	10	Ground (digital)
11	Not connected	12	Ground (digital)
13	A1	14	Ground (digital)
15	A0	16	Ground (digital)
17	$\overline{\text{INT0}}$	18	Ground (digital)
19	I/O_$\overline{\text{STRB}}$	20	Ground (digital)
21	R/$\overline{\text{W}}$	22	Ground (digital)
23	XF	24	Ground (digital)
25	CLK	26	Ground (digital)

J8 and J9 are 80-pin headers that mate directly to the PCI mothercard as described in Chapter 1, *EVM Overview*. Consequently, you cannot change the functions associated with these headers, so they are not described in this section.

Table 3–20. J10 Parallel Data Connector

Pin Number	Function	Pin Number	Function
1	DSP_15 (MSB)	2	Ground (digital)
3	DSP_14	4	Ground (digital)
5	DSP_13	6	Ground (digital)
7	DSP_12	8	Ground (digital)
9	DSP_11	10	Ground (digital)
11	DSP_10	12	Ground (digital)
13	DSP_09	14	Ground (digital)
15	DSP_08	16	Ground (digital)
17	DSP_07	18	Ground (digital)
19	DSP_06	20	Ground (digital)
21	DSP_05	22	Ground (digital)
23	DSP_04	24	Ground (digital)
25	DSP_03	26	Ground (digital)
27	DSP_02	28	Ground (digital)
29	DSP_01	30	Ground (digital)
31	DSP_00 (LSB)	32	Ground (digital)
33	CLKOUT	34	Ground (digital)

Table 3–21. Function of Connectors J11 and J12

Reference Designator	Function
J11	ADC $\overline{\text{CSTART}}$ signal (optional)
J12	ADC Clock signal (optional)

Chapter 4

Control Registers

Registers 0 and 1 inside the TLV1578 / TLV1571 / TLV571 control various ADC features and functions. This section describes the function of these registers.

Topic **Page**

4.1 Programming Model

The EVM uses an MSB model. The illustration below indicates how bits from a host system are mapped to the corresponding bits on the EVM.

To maintain software compatibility between each device in the family, it is important to note that bits D0 and D1 of the TLV571 EVM are grounded, and cannot be used. Since these bits control the MUX channel selected and some self-test results, the effect of their loss from the TLV571's functionality is small.

Table 4–1. Data Bus Bit

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLV1578	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00						
TLV1571	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00						
TLV571	D07	D06	D05	D04	D03	D02	D01	D00								

4.2 Control Register 0 – CR0

Table 4–2. Control Register 0 (Read/Write)

7	6	5	4	3	2	1	0
STARTSEL	PROG EOC	CLKSEL	SWPWDN	MODESEL	CHSEL (2-0)		

Bit 7 STARTSEL

STARTSEL determines hardware- or software-start for data conversion.

STARTSEL	0	Hardware conversion mode selected
	1	Software conversion mode selected

Bit 6 PROGEOC

PROGEOC determines how the ADC signals the host that a conversion has taken place.

PROGEOC	0	An interrupt signal, $\overline{\text{INT}}$, is generated after each conversion.
	1	An EOC signal is deasserted at the beginning of the conversion, and asserted at the end of the conversion.

The $\overline{\text{INT}}$/EOC signal is available through pin 17 of connector J7.

Bit 5 CLKSEL

CLKSEL establishes which clock signal is used by the ADC.

CLKSEL	0	Internal clock selected The TLV1578 has an integrated oscillator. Its value can be set to 10 ±1 MHz or 20 ±2 MHz by CR1.6.
	1	External clock selected The external clock input is available via J10 pin33.

Bit 4 SWPDWN

SWPDWN controls the power-down mode.

SWPWDN	0	Standard operation (auto-powerdown)
	1	Power-down mode selected In this mode the comparators, clock buffers, and internal reference power down, and the current drawn from the device does not exceed 10 μA.

Notice that the ADC automatically proceeds to a power-down mode if valid data is available, and it has not been read by the system after one clock cycle. In this mode, referred to as *auto-powerdown*, the comparators and clock buffers power down; however, the reference voltage does not power down. Consequently, the current drawn from the device is higher but does not exceed 1 mA.

Bit 3 MODESEL

MODESEL selects between single channel or sweep channel modes.

MODESEL	0	Single channel selected
	1	Each channel is accessed sequentially (swept)

Bit 2 – 0 CHSEL

CHSEL controls channel selection. The value written to this register depends upon the mode the user has selected (via MODESEL).

MODESEL=0: A single channel is selected.

	D2	D1	D0	Channel Selected
CHSEL	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

MODESEL=1: Sweep mode is selected.

	D2	D1	D0	Channels Sequenced
CHSEL	0	0	0	0 – 1
	0	0	1	0 – 1 – 2 – 3
	0	1	0	0 – 1 – 2 – 3 – 4 – 5
	0	1	1	0 – 1 – 2 – 3 – 4 – 5 – 6 –7
	1	0	0	N/A
	1	0	1	N/A
	1	1	0	N/A
	1	1	1	N/A

4.3 Control Register 1 – CR1

Table 4–3. Control Register 1 (Read/Write)

7	6	5	4	3	2	1	0
RESERVED	OSCSPD	RESESRVED		OUTCODE	READREG	STEST1	STEST0

Bit 7 is reserved.

Bit 6 OSCSPD

OSCSPD selects the speed of the integrated oscillator.

STARTSEL	0	Internal oscillator is set slow – 10-MHz clock
	1	Internal oscillator is set fast – 20-MHz clock

Bits 4 and 5 are reserved.

The ADC reserves two bits for internal use. You should always write 0 into these two bits.

Note:

In register readback mode, CR1.5 contains the opposite of what was written in; this should not be a concern.

Bit 3 OUTCODE

OUTCODE determines which output coding scheme is used by the ADC.

OUTCODE	0	Unipolar straight binary code selected
	1	Binary 2s-complement code selected

Bit 2, 1, and 0 READREG STEST1 and STEST0 (TLV1578/TLV1571 Only)

READREG determines if the ADC performs a self-test (3 self-test modes are available), or if the ADC control registers should be set to read-back mode.

READREG	0	Enable self-test
	1	Enable register readback

Three self-test modes are available. When READREG=1, the output is determined by the value of STEST1 and STEST0.

READREG	STEST1	STEST0	Outcome
1	0	0	Output = contents of CR0
1	0	1	Output = contents of CR1
1	1	0	Reserved
1	1	1	

This bit works in conjunction with STEST0 and STEST1.

READREG	STEST1	STEST0	Outcome
0	0	0	Output = conversion result
0	0	1	Output = self-test 1 result, 0000h
0	1	0	Output = self-test 2 result, 1/2 full scale
0	1	1	Output = self-test 3 result, full scale