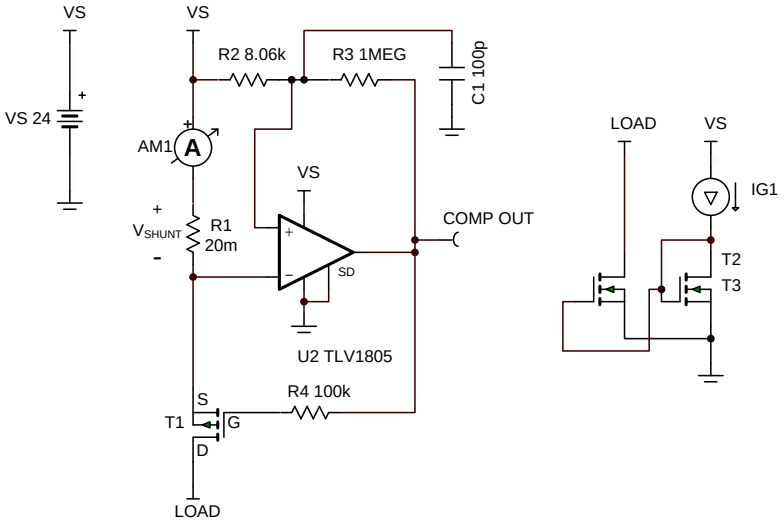
Over-Current Latch with Comparator Circuit

Design Goals

LOAD CURRENT (I_L)		SYSTEM SUPPLY (V_S)	COMPARATOR OUTPUT STATUS	
Over Current (I_{OC})	Recovery	Typical	Over Current	Normal Operation
10 A	power cycle	24 V	> V_S – 0.4 V	< 0.4 V

Design Description

This high-side, current sensing solution uses a high-voltage, rail-to-rail input comparator and a p-channel MOSFET to create an over-current (OC) latch circuit. The OC output signal from the comparator is a logic-high level when the load current exceeds 10A. The logic-high output level turns the MOSFET switch off and disconnects the load from the system supply (V_S). The comparator output also drives the bottom of the R2/R3 resistor divider which controls the OC threshold level. Under normal operating current levels, the bottom of the resistor divider is held low at ground potential. However, when the OC level is exceeded, the comparator output goes high and elevates the non-inverting input of the comparator to a level equal to V_S. Due to the integrated hysteresis of the comparator, the comparator output will remain high and thus a latched output condition is achieved. Only power-cycling V_S will remove the latched output condition. The shutdown pin could also be utilized to clear the latch if a pull-down resistor is added at the output of the comparator.



Design Notes

1. Select a comparator with rail-to-rail input common mode range to enable high-side current sensing.
2. Select a comparator with a push-pull output stage to efficiently drive the p-channel MOSFET.
3. Select a comparator with low input offset voltage to optimize accuracy.
4. Select a comparator with integrated hysteresis to create a latched-output condition.

Design Steps

1. Select the value of shunt resistor (R1) so the shunt voltage (V_{SHUNT}) is at least 10x greater than the comparator input offset voltage (V_{IO}). Note that making R1 very large will improve OC detection accuracy but will reduce supply headroom.

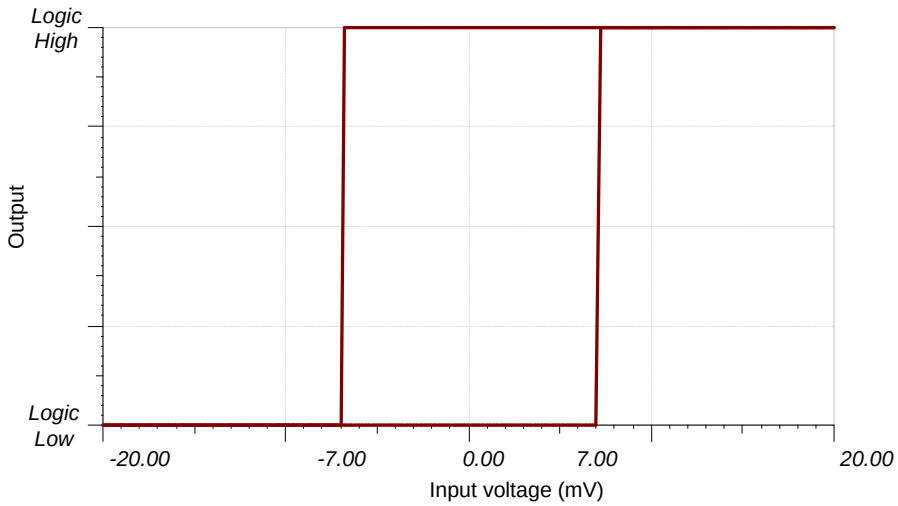
$V_{SHUNT} = (I_{OC} \times R_1) \geq 10 \times V_{IO}$

for $I_{OC} = 10A$ & $V_{IO} = 6.5mV$ (max value for TLV1805), $VSHUNT \geq 65mV$

set $R_1 = 20m\Omega$ so that $V_{SHUNT} = 200mV$ for $I_{OC} = 10A$

2. Since a comparator with integrated hysteresis is being utilized, the hysteresis needs to be accommodated for in the design. Note how a comparator with integrated hysteresis does not transition from high-to-low and from low-to-high at the same input voltage level. In the case of the TLV1805, the hysteresis is 14mV and thus the transition thresholds are at +/-7mV respectively.

Figure 1. TLV1805 Transition Thresholds



3. A good way to model a comparator's internal hysteresis is shown below. One can think of hysteresis as offset that is intentionally added to the design. When the output of the comparator is low, a voltage source equivalent to $V_{HYS}/2$ is added in series with the inverting input pin. However, when the comparator output is high, the hysteresis is modeled as a voltage source of the same value added in series with the non-inverting input.

Figure 2. Comparator Output Low

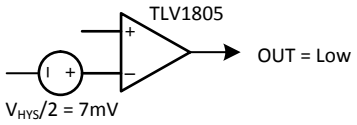
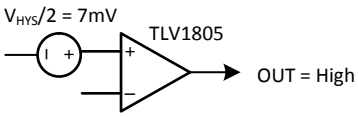


Figure 3. Comparator Output High



4. Select the values of resistor divider R2 and R3 so the comparator output will transition from low-to-high when V_{SHUNT} exceeds 200mV. Since the output of the comparator will be "low" prior to an OC condition occuring, use the Comparator Output Low model. The integrated hysteresis effectively shifts the switching threshold from V_S - 200mV to V_S - 193mV in the case of the TLV1805 which has an integrated hysteresis value of 14mV. Recall that 1/2 of the hysteresis is applied since hysteresis is defined as the difference between the two switching thresholds of a comparator.

5. The following equation is used to solve for R2 and R3.

$$R_2 = \frac{(V_{SHUNT} - V_{HYS}/2) \times R3}{V_S - (V_{SHUNT} - V_{HYS}/2)}$$

for $V_S = 24V$, $V_{SHUNT} = 200mV$, $V_{HYS} = 14mV$ and $R3 = 1M\Omega$

$$R2 = \frac{(200m - 14m/2) \times 1M}{24 - (200m - 14m/2)}$$

$R2 = 8.107k\Omega$ (closest 1% value is $8.06k\Omega$)

6. Since the goal of this design is to create a circuit that will disconnect the load from the system supply when an OC condition occurs, the output of the comparator is connected to the gate of a p-channel MOSFET switch. Recall that a p-ch MOSFET will look like a closed switch when the source to gate voltage is greater than the voltage threshold ($V_{SG} > V_{TH}$). Likewise, the MOSFET will look like an open-circuit when $V_{SG} < V_{TH}$ (see figures below).

Figure 4. Normal Operation = Output LOW and CLOSED Switch

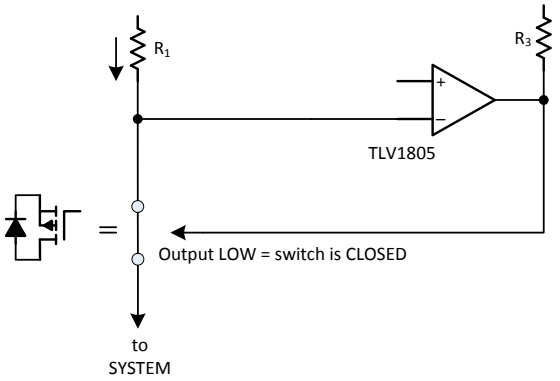
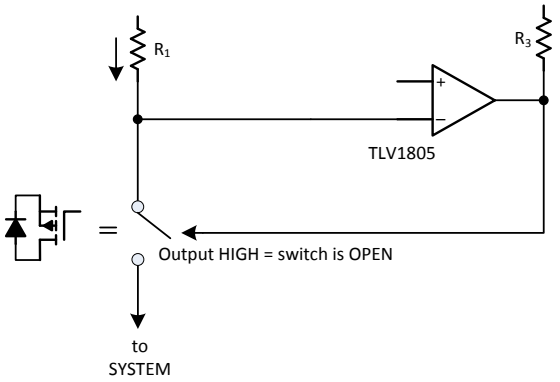


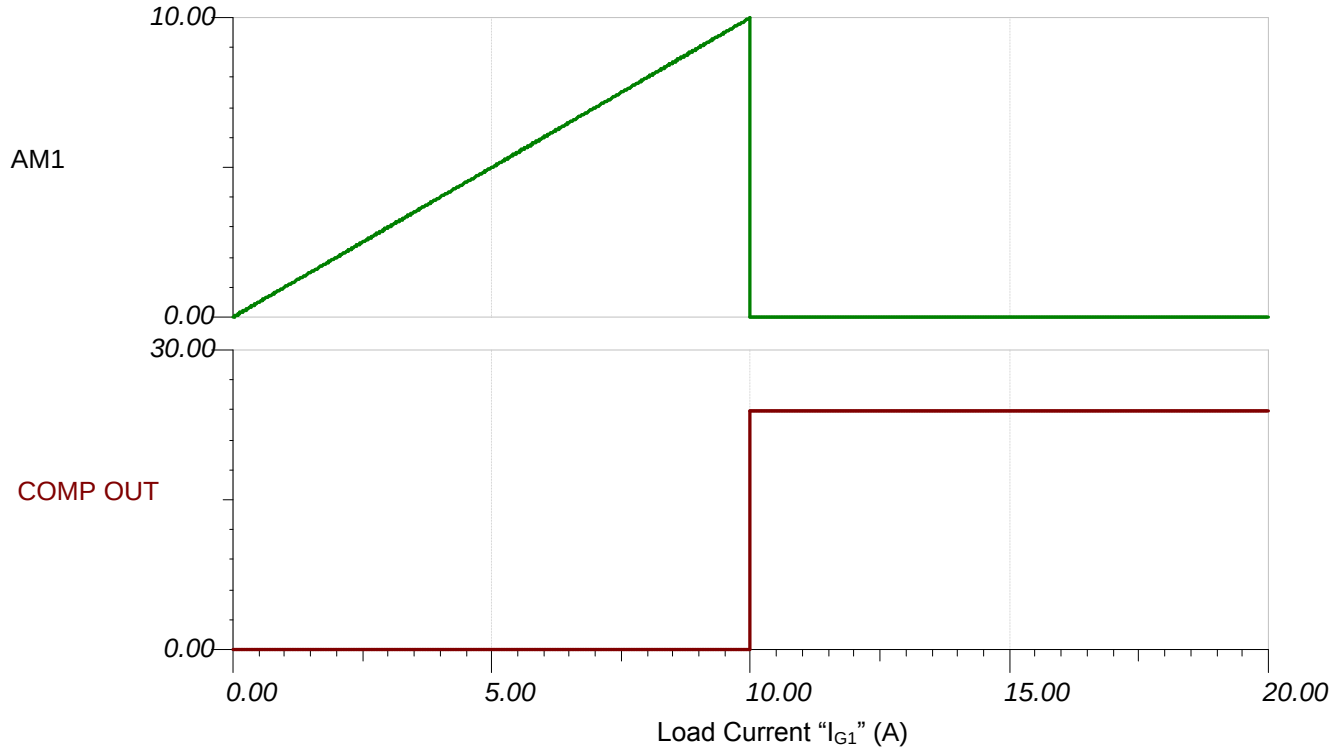
Figure 5. OC Condition = Output HIGH and OPEN Switch



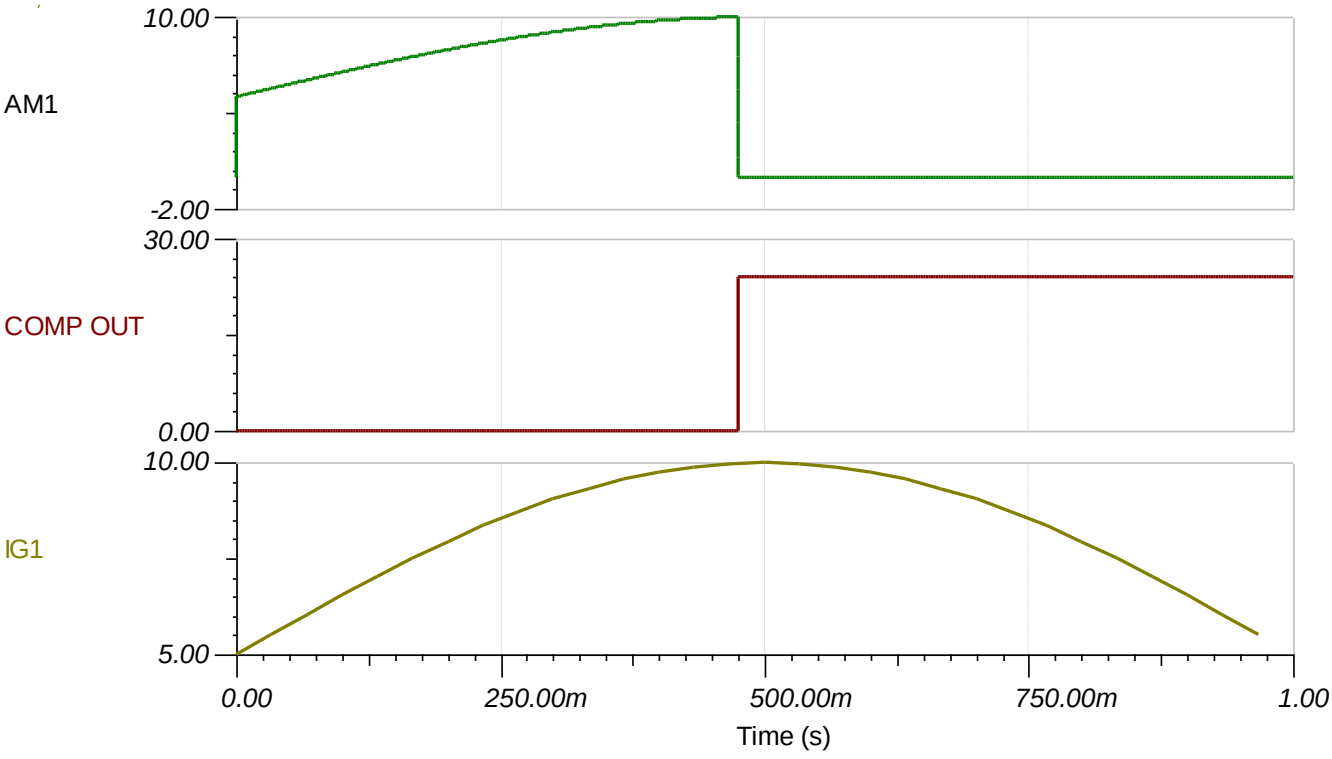
7. Add a series resistor (R4) between the comparator output and the gate of the MOSFET to limit the output current during the transition from low to high. Keeping the current in the mA range is sufficient. Selecting a value of 10kΩ for R1, the current is limited to 2.4mA (24V/10kΩ).
8. The other goal of this design is to latch the circuit when an OC condition occurs. This is accomplished by providing feedback to the resistor divider network of R2/R3. When the output of the comparator goes high, it turns off the MOSFET and raises the non-inverting node of the comparator to a voltage level of V_S.
9. Note that V_{SHUNT} also reduces to 0V since the load current is now 0A. The hysteresis of the comparator that was previously mentioned in Design Step 2 will keep the non-inverting input 7mV higher than the inverting input. This is what latches the comparator output in a logic high state.
10. Lastly, capacitor C1 is connected from the non-inverting input to ground to make sure that the comparator starts in the logic low output state as V_S rises upon initial power-up.

Design Simulations

DC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SLOM456, http://www.ti.com/lit/zip/snom675.

Design Featured Comparator

TLV1805-Q1, TLV1805	
V_S	3.3 V to 40 V
V_{inCM}	Rail-to-rail
V_{OUT}	Push-Pull
V_{OS}	500µV
I_Q	135 µA
$t_{PD(HL)}$	250 ns
#Channels	1
www.ti.com/product/tlv1805	

Design Alternate Comparator

	LMC6762	TLV370x-Q1, TLV370x
V_S	2.7 V to 15 V	2.7 V to 16 V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{OUT}	Push-Pull	Push-Pull
V_{OS}	3 mV	250 µV
I_Q	20 µA	560 nA/Ch
$t_{PD(HL)}$	4 µs	36 µs
#Channels	1	1, 2, 4
	www.ti.com/product/lmc6762	www.ti.com/product/tlv3701

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