Common Sample Rate Selection for TLV320AIC12 /13 /14 /15 /20 /21 /24 /25 Codecs

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ABSTRACT

This application report intends to help TI voice-band codec users to quickly and properly select the commonly used master clock frequency (MCLK) and the corresponding frequency dividers, M, N, and P, which is the first step for utilizing TI's TLV320AIC12 /13 /14 /15 /20 /21 /24 /25 voice-band codecs.

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1 Introduction

When applying TI's voice-band codec, such as TLV320AIC12, TLV320AIC13, TLV320AIC14, TLV320AIC15, TLV320AIC20, TLV320AIC21, TLV320AIC24, or TLV320AIC25, users are required to select the proper master clock, denoted by MCLK. The three corresponding frequency dividers, named M, N, and P, are selected to set the codec(s) to the desired ADC and DAC sample rate(s), up to 26 kHz, for their applications.

The relationship among the sample rate (f_{FS}), the MCLK frequency (f_{MCLK}), and the dividers are expressed by the equation:

$$f_{FS} = \frac{f_{MCLK}}{(16 \times M \times N \times P)} \quad (1)$$

where f_{FS} is equal to or slower than 26 kHz; f_{MCLK} is equal or slower than 100 MHz; and M, N, and P are integers and M = 1, 2, … 128, N = 1, 2, … 16, and P = 1, 2, … 8. There are a couple of restrictions and requirements for the M, N, and P selections, depending on the codec's modes and operation conditions, summarized as the followings:

1. If the codec is running at the *fine* sampling mode, i.e.: P is not equal to 8, then the following equation also must be satisfied:

$$10\ \text{MHz} \le \frac{f_{MCLK}}{P} \le 25\ \text{MHz} \quad (2)$$

2. Under the turbo mode of the codec, P should not be equal to 1.
3. If the codec's internal FIR/IIR is bypassed, M is a multiple of 4, or M divides by 4.

Refer to the corresponding data sheet for details.

Providing several fast reference tables, this application report selected the MCLK frequency and the M, N, P values for the most commonly used voice–band sample frequencies, listed in Table 1. For convenience, these sample rates are grouped.

Table 1. Considered Sample Frequencies

GROUP	SAMPLE FREQUENCY
Group 1	4000 Hz
	8000 Hz
	16000 Hz
Group 2	12000 Hz
	24000 Hz
Group 3	11025 Hz
	22050 Hz

2 Select Codec's Master Clock Rate: f_{MCLK}

To select the codec's master clock f_{MCLK}, use equation 1 under the given or desired sample rate:

$$f_{MCLK} = f_{FS} \times 16 \times M \times N \times P \quad (3)$$

Where the f_{FS} denotes the given sample rate, and the integers M, N, and P are the frequency dividers. Since there are so many choices of the MCLK frequency and the dividers for a given f_{FS}, this report presents some examples for the user's convenience.

2.1 Select f_{MCLK} for Single Sample Rate

If the codec is expected to operate at one fixed sample frequency, we can obtain the accurate sample rate by selecting the prospected MCLK frequency f_{MCLK} from equation 3, for the desired sample rate f_{FS}. Depending on the choice on M, N, P, which is discussed later, the f_{MCLK} can be found. However using the proper f_{MCLK} makes the M, N, P selection much simpler and more accurate.

It is not necessary but safer to select f_{MCLK} at the range of10 MHz to 100 MHz, and being integer–dividable by (16 x 8 x 4), so that the codec(s) can operate at all possible codec operation modes and working conditions whenever needed. Where, the integer 16 is used to composite the 16 in equation 1; the 8 is needed for selecting the *coarse* (vs the *fine*) sample frequency; and the 4 is needed when the FIR or IIR is bypassed.

Table 2 presents the equations that can be used to select the proper MCLK frequency f_{MCLK}, for these common used voice-band sample rates listed in Table 1.

Table 2. f_{MCLK} for Single Sample Frequency

SAMPLE FREQUENCY	MCLK FREQUENCY – f_{MCLK} – EXPRESSION	MCLK FREQUENCY – f_{MCLK}
4000 Hz	$f_{MCLK} = 4000 \times (16 \times 8 \times 4) \times K = 2.048\ MHz \times K$, for K = 5, 6, 7, 8, … , 47, 48	10.24 MHz or 12.288 MHz or 14.336 MHz or 16.384 MHz or … 96.256 MHz or 98.304 MHz
8000 Hz	$f_{MCLK} = 8000 \times (16 \times 8 \times 4) \times K = 4.096\ MHz \times K$, for K = 3, 4, 5, … , 23, 24	12.288 MHz or 16.384 MHz or 20.48 MHz or … 94.208 MHz or 98.304 MHz
16000 Hz	$f_{MCLK} = 16000 \times (16 \times 8 \times 4) \times K = 8.192\ MHz \times K$, for K = 2, 3, 4, … , 11, 12	16.384 MHz or 24.576 MHz or 32.768 MHz or … 90.112 MHz or 98.304 MHz
12000 Hz	$f_{MCLK} = 12000 \times (16 \times 8 \times 4) \times K = 6.144\ MHz \times K$, for K = 2, 3, 4, … , 15, 16	12.288 MHz or 18.432 MHz or 24.576 MHz or … 92.16 MHz or 98.304 MHz
24000 Hz	$f_{MCLK} = 24000 \times (16 \times 8 \times 4) \times K = 12.288\ MHz \times K$, for K = 1, 2, 3, … , 7, 8	12.288 MHz or 24.576 MHz or 36.864 MHz or … 86.016 MHz or 98.304 MHz

Table 2. f_{MCLK} for Single Sample Frequency (Continued)

SAMPLE FREQUENCY	MCLK FREQUENCY – f_{MCLK} – EXPRESSION	MCLK FREQUENCY – f_{MCLK}
11025 Hz	$f_{MCLK} = 11025 \times (16 \times 8 \times 4) \times K = 5.6448\ MHz \times K$, for K = 2, 3, 4, … , 16, 17	11.2896 MHz or 16.9344 MHz or 22.5792 MHz or … 90.3168 MHz or 95.9616 MHz
22050 Hz	$f_{MCLK} = 22050 \times (16 \times 8 \times 4) \times K = 11.2896\ MHz \times K$, for K = 1, 2, 3, … , 7, 8	11.2896 MHz or 22.5792 MHz or 33.8688 MHz or … 79.0272 MHz or 90.3168 MHz

2.2 Select f_{MCLK} for Multiple Sample Rates Within a Group

Using the Table 2, the MCLK frequency for a given sample rate is obtained. There are many possible choices. If more than one sample rate is required for the codec(s) to operate, many of the frequencies for the MCLK may no longer be good. However, if the several desired sample rates are in the same group, the MCLK selection can be very simple. Table 3 lists the MCLK frequencies for multiple sample rates within a group.

Table 3. f_{MCLK} for Multiple Sample Rates Within A Group

SAMPLE FREQUENCY	MCLK FREQUENCY EXPRESSION	MCLK FREQUENCY – f_{MCLK}
4000 Hz 8000 Hz and 16000 Hz	$f_{MCLK} = 16000 \times (16 \times 8 \times 4) \times K = 8.192\ MHz \times K$, for K = 2, 3, 4, 5, 6, … , 11, 12	16.384 MHz or 24.576 MHz or 32.768 MHz or 40.96 MHz or 49.152 MHz or … 90.112 MHz or 98.304 MHz
12000 Hz 24000 Hz	$f_{MCLK} = 24000 \times (16 \times 8 \times 4) \times K = 12.288\ MHz \times K$, for K = 1, 2, 3, 4, … , 7, 8	12.288 MHz or 24.576 MHz or 36.864 MHz or 49.152 MHz or … 86.016 MHz or 98.304 MHz
11025 Hz 22050 Hz	$f_{MCLK} = 22050 \times (16 \times 8 \times 4) \times K = 11.2896\ MHz \times K$, for K = 1, 2, 3, 4, … , 7, 8	11.2896 MHz or 22.5792 MHz or 33.8688 MHz or 45.1584 MHz or … 79.0272 MHz or 90.3168 MHz

2.3 Select f_{MCLK} for General Multiple Sample Rates

When the desired sample rate f_{FS} needs to be changed in different groups, the possible choices for the f_{MCLK} may be restricted for getting an f_{MCLK} that is integer-dividable for all of the $f_{FS} \times 16 \times 8 \times 4$.

Tables 4 to 5 give some of the MCLK frequencies that are used for the f_{MCLK} selection under the multiple common sample rates conditions. Note that in Table 4, there is not a single f_{MCLK} that is integer-dividable for all of the $f_{FS} \times 16 \times 8 \times 4$.

Table 4. f_{MCLK} for 4000/8000/24000/11025/22050 Hz Sample Rates

SAMPLE FREQUENCY f_{FS}	CORRESPONDING MCLK FREQUENCY (see Note 1) f_{MCLK}
4000 Hz	f_{MCLK} = 3,528,000 × (16) (see Note 1) = 56.448 MHz (see Note 2)
8000 Hz	
12000 Hz	
24000 Hz	
11025 Hz	
22050 Hz	

NOTES: 1. There is only one MCLK frequency, i.e.: 56.448 MHz, that is used for all 6 of the sample rates in Table 4 with proper integers M, N, and P, which are discussed in the next section.
2. MCLK at 56.448 MHz for the Codec(s) may be not suitable for some of the modes. For example: at f_{FS} = 8 kHz, set M = 21, N = 7 and P = 3 when f_{MCLK} = 56.448 MHz (since 56.448 M/(16 × 21 × 7 × 3) = 8K). Where P = 3 and the codec(s) is not at the coarse mode.

Table 5. f_{MCLK} for Groups 1 and 2 Sample Rates

SAMPLE FREQUENCY	MCLK FREQUENCY EXPRESSION	SELECTED f_{MCLK}
4000 Hz	f_{MCLK} = 1000 × 4 × 3 × 2 × 2 × (16 × 8 × 4) × K = 48000 × (16 × 8 × 4) × K = 24.576 MHz × K for K = 1, 2, 3, 4	24.576 MHz or 49.152 MHz or 73.728 MHz or 98.304 MHz
8000 Hz		
16000 Hz		
12000 Hz		
24000 Hz		

3 Select Sample Rate Dividers: M, N, and P

After the MCLK frequency is selected or given, the next step is to select the three frequency dividers, or the M, N, and P as the data sheet named, so as to get the desired codec ADC/DAC sample rate. By default, these dividers were preset at: M=16, N=6, and P=8 (coarse sampling) in the TLV320AIC12/13/14/15/20/21/24/25 codecs at the power up. Therefore, the codec's power–up default sample rate is always known, given the MCLK frequency f_{MCLK}.

The sample rates can be changed by software based on the application requirement after the power up or *on-the-fly*, through configuring or reconfiguring the dividers: M, N, and/or P, which are in the codec's control register 4. Refer to the corresponding data sheet for details.

The parameter P, P = 1, 2, 3, …, 8, is related to the codec device's internal digital phase-lock loop (DPLL). When P=8 the DPLL is disabled and the device is working at the *coarse sampling* mode. Otherwise, for P=1 to 7, the DPLL is enabled and the codec is working in the *fine sampling* mode. For the current reversion of TLV320AIC12 /13 /14 /15 /20 /21 /24 /25 codecs, the DPLL may not work properly if P=1 under the turbo mode. To be safe, use the *coarse sample* mode and avoid using P=1 if the codec(s) are in the turbo mode.

With the known f_{MCLK} and f_{FS}, the product of M × N × P can be obtained, by equation 1 or:

$$M \times N \times P = f_{MCLK}/f_{FS}/16 \quad (4)$$

Selecting the M, N, and P individually can be whatever you prefer, as long as:

1. Each of them is an integer at its range (M=1 to 128, N=1 to 16, and P = 1 to 8).
2. If at the fine sampling mode, P should satisfy equation 2.

3. Do not use P=1 at the turbo mode.
4. If the FIR/IIR is bypassed, M is a multiple of 4 or M divides by 4.

3.1 Select Dividers Under Selectable f_{MCLK}

The following Tables 6, 7, 8, and 9 list the M, N, and P for the Table 1 common sample frequencies, where the f_{MCLK} has been selected or selectable so that the theoretically exact sample rate f_{FS} can be obtained. There are many other MCLK frequencies and M, N, and P values that may work, these tables show only some examples.

Table 6. Frequency Dividers (M, N, and P) Selection for Group 1 Sample Rates

MASTER CLOCK FREQUENCY f_{MCLK}	SAMPLE FREQUENCY, f_{FS}								
	4 kHz			8 kHz			16 kHz		
	M	N	P	M	N	P	M	N	P
16.384 MHz	16	2	8	16	1	8	4	2	8
24.576 MHz	16	3	8	8	3	8	4	3	8
32.768 MHz	16	4	8	16	2	8	16	1	8
40.960 MHz	16	5	8	8	5	8	4	5	8
49.152 MHz	16	6	8	16	3	8	4	6	8
56.448 MHz	42	7	3	21	7	3			
57.344 MHz	16	7	8	8	7	8	4	7	8
65.536 MHz	16	8	8	16	4	8	16	2	8
73.728 MHz	16	9	8	8	9	8	4	9	8
81.920 MHz	16	10	8	16	5	8	4	10	8
90.112 MHz	16	11	8	8	11	8	4	11	8
98.304 MHz	16	12	8	16	6	8	16	3	8

Table 7. Frequency Dividers (M, N, and P) Selection for Group 2 Sample Rates

MASTER CLOCK FREQUENCY f_{MCLK}	SAMPLE FREQUENCY f_{FS}					
	12 kHz			24 kHz		
	M	N	P	M	N	P
12.288 MHz	8	1	8	4	1	8
24.576 MHz	16	1	8	4	2	8
36.864 MHz	8	3	8	4	3	8
49.152 MHz	16	2	8	4	4	8
56.448 MHz	14	7	3	7	7	3
61.440 MHz	8	5	8	4	5	8
73.728 MHz	16	3	8	4	6	8
86.016 MHz	8	7	8	4	7	8
98.304 MHz	16	4	8	16	2	8

Table 8. Frequency Dividers (M, N, and P) Selection for Group 3 Sample Rates

MASTER CLOCK FREQUENCY f_{MCLK}	SAMPLE FREQUENCY f_{FS}					
	11.025 kHz			22.050 kHz		
	M	N	P	M	N	P
11.2896 MHz	8	1	8	4	1	8
22.5792 MHz	16	1	8	4	2	8
33.8688 MHz	8	3	8	4	3	8
45.1584 MHz	16	2	8	16	1	8
56.4880 MHz	8	5	8	4	5	8
67.7376 MHz	16	3	8	4	6	8
79.0272 MHz	8	7	8	4	7	8
90.3168 MHz	16	4	8	16	2	8

Table 9. Frequency Dividers (M, N, and P) Selection for Multi-Group Sample Rates

SAMPLE FREQUENCY F_{FS}	MCLK FREQUENCY f_{MCLK} = 56.448 MHz		
	M	N	P
4000 Hz	42	7	3
8000 Hz	21	7	3
12000 Hz	14	7	3
24000 Hz	7	7	3
11025 Hz	8	5	8
22050 Hz	4	5	8

3.2 Select Dividers Under Nonselectable f_{MCLK}

In *real-world* applications the MCLK frequency f_{MCLK} is not always selectable. Or for multiple sample rates systems, one fixed f_{MCLK} can not divide ($16 \times f_{FS}$) for all of the multiple sample rates. As a result, the $f_{MCLK} / f_{FS}/16 = M \times N \times P$, in equation 4, is often not an integer.

Example: Noninteger Product of M, N, and P. In Table 6, the integers M, N, and P do not exist for f_{FS} = 16 kHz if the MCLK frequency f_{MCLK} is selected as 56.448 MHz, since $M \times N \times P = f_{MCLK} / f_{FS} / 16 = 56448000 / 16000 / 16 = 220.5$ is not an integer.

Certainly, the noninteger product can always be rounded to its nearest integer(s). In the above example, we can approximate $M \times N \times P$ to 220. However, the actual sample rate is not 16 kHz but 16.036 kHz, which is about 0.23% off the desired. Note that, in the above example, we should not use M x N x P = 221. Only integers 1, 13, and 17 can divide 221, but 13 and 17 are outside the range of P (P = 1, 2, …, 8), which leaves one choice: P = 1. If P = 1, since f_{MCLK} = 56.488 MHz, the requirement for *fine sample* mode or equation 2 is not satisfied.

Table 10 selected some common M, N, P dividers, under the fixed MCLK frequencies 50, 80, or 100 MHz, which are the common clock frequencies when using the clock from TI's TMS320C5402™ or C5416™ DSPs or their DSKs.

Table 10. Select M, N, and P With Given 50/80/100 MHz MCLK Frequency

SAMPLE FREQUENCY f_{MCLK}	f_{MCLK} = 50 MHz				f_{MCLK} = 80 MHz				f_{MCLK} = 100 MHz			
	M	N	P	Actual f_{FS}	M	N	P	Actual f_{FS}	M	N	P	Actual f_{FS}
4000 Hz	16	6	8	4069 Hz	52	3	8	4006 Hz	32	6	8	4096 Hz
	14	7	8	3986 Hz	12	13	8	4006 Hz	28	7	8	3986 Hz
	52	5	3	4006 Hz	50	5	5	4000 Hz	52	5	6	4006 Hz
8000 Hz	16	3	8	8138 Hz	13	6	8	8013 Hz	16	6	8	8138 Hz
	7	7	8	7972 Hz	79	1	8	7912 Hz	14	7	8	7972 Hz
	26	5	3	8013 Hz	25	5	5	8000 Hz	26	5	6	8013 Hz
16000 Hz	4	6	8	16276 Hz	13	3	8	16026 Hz	8	6	8	16276 Hz
	5	5	8	15625 Hz	20	2	8	15625 Hz	10	5	8	15625 Hz
	13	5	3	16026 Hz	13	6	4	16026 Hz	13	5	6	16026 Hz
12000 Hz	16	2	8	12207 Hz	4	13	8	12019 Hz	16	4	8	12207 Hz
	11	3	8	11837 Hz	12	7	5	11904 Hz	11	6	8	11837 Hz
	13	5	4	12019 Hz	13	4	8	12019 Hz	52	2	5	12019 Hz
24000 Hz	16	1	8	24414 Hz	13	2	8	24038 Hz	16	2	8	24414 Hz
	17	1	8	22978 Hz	6	7	5	23810 Hz	33	1	8	23674 Hz
	13	2	5	24038 Hz	4	13	4	24038 Hz	13	4	5	24038 Hz
11025 Hz	7	5	8	11161 Hz	8	7	8	11161 Hz	14	5	8	11161 Hz
	4	9	8	10851 Hz	19	3	8	10965 Hz	71	1	8	11004 Hz
	47	2	3	11082 Hz	91	1	5	10989 Hz	9	9	7	11023 Hz
22050 Hz	17	1	8	22978 Hz	4	7	8	22321 Hz	7	5	8	22321 Hz
	3	6	8	21701 Hz	29	1	8	21552 Hz	4	9	8	21701 Hz
	71	1	2	22007 Hz	57	1	4	21930 Hz	71	1	4	22007 Hz

4 References

1. *TLV320AIC12, Low Power CMOS, 16-Bit, 26-KSPS CODEC With Smart Time Division Multiplexed (SMARTDM™) Serial Port,* data manual (SLWS115)
2. *TLV320AIC13, SMARTDM™ Low Power, Low Voltage, 1.1 V to 3,6 V I/O, 16-Bit, 26-KSPS CODEC,* data manual (SLWS139)
3. *TLV320AIC14, Low Power CMOS, 16-Bit, 26-KSPS CODEC With Smart Time Division Multiplexed (SMARTDM™) Serial Port,* data manual (SLWS140)
4. *TLV320AIC15, SMARTDM™ Low Power, Low Voltage, 1.1 V to 3,6 V I/O, 16-Bit, 26-KSPS CODEC*, data manual (SLWS141)
5. *TLV320AIC20, Low Power, High-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec*, data manual (SLWS363A)
6. *TLV320AIC21, Low Power, Low Voltage, 1.1 V to 3,6 V I/O, High-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec*, data manual (SLWS365A)
7. *TLV320AIC24, Low Power, High-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec*, data manual (SLWS366A)
8. *TLV320AIC25, Low Power, Low Voltage, 1.1 V to 3,6 V I/O, High-Integrated Programmable 16-Bit 26-KSPS Dual Channel Codec*, data manual (SLWS367A)

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