Application Report
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TLV320AIC32x6 Sleep and Standby Modes

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ABSTRACT

The TLV320AIC3206 and TLV320AIC3256 (or *AIC32x6*) audio converter devices can be configured for low power operation during Standby and Sleep modes. This report provides an overview of how to enable the AIC32x6 for this type of operating mode as well as several sample scripts.

Contents

1 Sleep and Standby Modes

There are a relatively limited number of blocks that must be configured to set the device into (or wake the device from) both Sleep and Standby modes.

Table 1 shows the steps required to set the device into these two operating modes. Registers associated with Sleep mode are marked in blue. It is presumed that both the analog-to digital converter (ADC) and digital-to-analog converter (DAC) channels are used; otherwise, the corresponding steps can be skipped. Note that the ADC and DAC power bits are also associated with **miniDSP_A** and **miniDSP_D** power-up; if the miniDSP_A is used to complement miniDSP_D processing in the AIC3256, or vice-versa, then both the ADC and DAC channels must be powered.

When going into either Sleep or Standby mode, it is recommended to keep the master clock running until all steps are complete. Specific requirements are noted in Table 1.

Table 1. Sleep and Standby Modes Configuration

Step	Description / Associated Register(s)
1. Power down internal amplifiers	The headphone (HP), line (LO), and mixer (MA) amplifiers should be powered off at this point. This state will reduce power consumption and prevent pops/clicks when configuring subsequent blocks. The MicPGA input amplifier can also be configured to ensure that the programmed gain flags (p1_r62_b1-0) are reset when the ADCs are powered down. Register(s): • p1_r9_b5-0 = 000000b (power down HP/LO/MA) • p1_r59_b7 = 0b (enable MicPGA_L gain control) • p1_r60_b7 = 0b (enable MicPGA_R gain control)
2a. Set reference to automatic mode (SLEEP MODE ONLY)	In sleep mode, the internal reference circuit (by default) should be configured to automatically power down when all analog blocks are powered down. Register(s): • p1_r123_b2 = 0b (automatic REF power-up)

Table 1. Sleep and Standby Modes Configuration (continued)

Step	Description / Associated Register(s)
2b. Set reference to forced mode (STANDBY MODE ONLY)	In standby mode, the internal reference circuit should be forced on to allow for quick playback requests. Register(s): • p1_r123_b2 = 1b (forced REF power-up)
3. Disable AGCs	Before powering down the ADCs, ensure that the AGCs are disabled. This condition should be accomplished by writing these registers in the order shown below. Register(s): • p0_r87_b5-1 = 00000b (disable LAGC noise threshold) • p0_r95_b5-1 = 00000b (disable RAGC noise threshold) • p0_r86_b7 = 0b (disable LAGC) • p0_r94_b7 = 0b (disable RAGC)
4. Power down ADCs	Powering down both ADCs will shut down the internal modulators as well as the associated processing blocks, the miniDSP_A (AIC3256 only, if applicable), and the MicPGAs (if MA is powered down). To ensure that both ADCs are powered down, the respective associated flags can be read. The internal ADC_CLK must be active before powering down the ADCs. Therefore, the master clock source must not removed until these flags are cleared. Register(s): • p0_r81_b7-6 = 00b (power down both ADCs) Flags(s): • p0_r36_b6 (LADC power status) • p0_r36_b2 (RADC power status) **After powering down both ADCs, the MCU should wait for p0_r36 = X0XXX0XXb, where *'X'* denotes *don't care*.**
5. Power down DACs	Powering down both DACs will shut down the internal modulators as well as the associated processing blocks and the miniDSP_D (AIC3256 only, if applicable). To ensure that both DACs are powered down, their associated flags can be read. The internal DAC_CLK must be active before powering down the DACs. Therefore, the master clock source must not removed until these flags are cleared. In the same register (p0_r37), the HP and LO power flags can also be verified. This is to ensure that HP and LO amplifiers were completely shut down after step #1. Register(s): • p0_r63_b7-6 = 00b (power down both DACs) Flags(s): • p0_r37_b7 (LDAC power status) • p0_r37_b3 (RDAC power status) • p0_r37_b5 (HPL power status) • p0_r37_b1 (HPR power status) • p0_r37_b6 (LOL power status) • p0_r37_b2 (LOL power status) **After powering down both DACs, the MCU should wait for p0_r37 = 000X000Xb, where *'X'* denotes *don't care*.**

Table 1. Sleep and Standby Modes Configuration (continued)

Step	Description / Associated Register(s)
6. Disconnect output amplifier routing	After powering down the DACs, the internal connections to the HP and LO amplifiers should be disabled. Register(s): • p1_r12_b3-0 = 0000b (HPL inputs disconnected) • p1_r13_b4-0 = 00000b (HPR inputs disconnected) • p1_r14_b4-0 = 00000b (LOL inputs disconnected) • p1_r15_b3,1 = 0b (LOR inputs disconnected)
7. Power off additional blocks	Additional blocks should be powered down to save power. Headset detection must be disabled when going into sleep mode. Register(s): • p1_r51_b6 = 0b (power down MICBIAS) • p1_r58_b7-2 = 000000b (disable weak bias for all inputs) • p0_r29_b2 = 0b (disable forced audio serial interface output) • p0_r30_b7 = 0b (power off BCLK N divider) • p0_r26_b7 = 0b (power off CLKOUT M divider) • p0_r67_b7 = 0b (disable headset detection for sleep mode)
8. Power down clock generation tree	The PLL and its dividers are automatically powered down when there is no block that uses the clock tree (for example, ADCs, DACs, audio serial interface, and CLKOUT). However, it is recommended to power down these blocks manually. Register(s): • p0_r19_b7 = 0b (power down MADC divider) • p0_r12_b7 = 0b (power down MDAC divider) • p0_r18_b7 = 0b (power down NADC divider) • p0_r11_b7 = 0b (power down NDAC divider) • p0_r5_b7 = 0b (power down PLL)
9a. Configure AVDD and Charge pump (SLEEP MODE ONLY)	To go into sleep, AVDD and DVDD should be weakly connected and the analog block configuration bit set to ‘1’ (OFF). The AVDD supply could be removed, if desired. DVDD should be present to preserve internal memory contents. The charge pump must be powered down in order to save power. Register(s): • p1_r1_b1-0 = 00b (power down charge pump) • p1_r2_b3 = 1b (disable analog blocks) • p1_r1_b3 = 0b (enable weak AVDD to DVDD connection)

Table 2 lists the steps to wake the device from both Sleep and Standby modes. Registers associated with Sleep mode are marked in blue.

When waking the device from either Sleep or Standby mode, it is recommended to provide a master clock and the Audio Serial Interface (ASI) bus before beginning the wake procedure. Specific requirements are noted in Table 2.

Table 2. Wake Up from Sleep and Standby Modes Configuration

Step	Description / Associated Register(s)
1a. Configure AVDD Supply and charge pump (SLEEP MODE ONLY)	To wake up from sleep mode, the first step is to configure the AVDD supply. Ensure that the AVDD supply is connected before disabling the weak AVDD to DVDD connection. The charge pump can also be powered if using the ground centered headphone mode. Register(s): • p1_r1_b3 = 1b (disable weak AVDD to DVDD connection) • p1_r2_b3 = 0b (enable analog blocks) • p1_r1_b1-0 = 10b (power up charge pump)
2. Power up clock generation tree	The clock generation tree may be used for several functional blocks of the AIC32x6. Register(s): • p0_r5_b7 = 1b (power up PLL) • p0_r18_b7 = 1b (power up NADC divider; see (1)) • p0_r11_b7 = 1b (power up NDAC divider; see (1)) • p0_r19_b7 = 1b (power up MADC divider) • p0_r12_b7 = 1b (power up MDAC divider)
3. Power up functional blocks (optional)	If desired, special functions blocks can be powered in this step. When operating the audio serial interface (ASI) bus in master mode (that is, BCLK and WCLK are outputs), the associated pins are in high impedance state until an ADC or DAC is powered up unless overridden in p0_r29_b2. MCLK should be provided at this moment if any block depends on its clock (such as ASI or CLKOUT). Register(s): • p1_r51_b6 = 1b (power up MICBIAS, if desired) • p1_r58_b7-2 = xxxxxxb (enable weak bias for analog inputs, if desired) • p0_r29_b2 = 1b (enable forced ASI output, if desired) • p0_r30_b7 = 1b (power up BCLK N divider, for ASI master mode) • p0_r26_b7 = 1b (power up CLKOUT M divider, if desired) • p0_r67_b7 = 1b (enable headset detection, if desired) • p0_r86_b7 = 1b (enable LAGC, if desired) • p0_r94_b7 = 1b (enable RAGC, if desired)
4. Configure ADC channel routing (unless previously configured)	In this step, the ADC channel input source can be selected. If using the analog inputs, the MicPGA input connections should be configured. The digital microphone pin configuration can also be configured, otherwise. Register(s): • p1_r52_b7-0 = xxxxxxxxb (MicPGA_LP routing) • p1_r54_b7-0 = xxxxxxxxb (MicPGA_LM routing) • p1_r55_b7-0 = xxxxxxxxb (MicPGA_RP routing) • p1_r57_b7-0 = xxxxxxxxb (MicPGA_RM routing)
5. Configure output amplifier routing	The output amplifiers should be configured in this step. Register(s): • p1_r12_b3-0 = xxxxb (configure HPL inputs) • p1_r13_b4-0 = xxxxxb (configure HPR inputs) • p1_r14_b4-0 = xxxxxb (configure LOL inputs) • p1_r15_b3,1 = xb (configure LOR inputs)

(1) In cases where miniDSP synchronization (p0_r60_b7 = 1 in AIC3256) is required, NDAC must be powered at Step #8 and NADC can remain off.

Table 2. Wake Up from Sleep and Standby Modes Configuration (continued)

Step	Description / Associated Register(s)
6. Power up ADCs	Once an ADC channel is powered, the clock generation tree will be activated unless another block that depends on the clock generation tree is already powered. Powering up an ADC will power the internal modulator as well as the associated processing blocks, the miniDSP_A (AIC3256 only, if applicable) and the MicPGAs (if MA is powered up or analog inputs are routed). The master clock and audio serial interface (ASI) bus should be active at this point. Register(s): • p0_r81_b7-6 = 11b (power up both ADCs)
7. Power up DACs	Once a DAC channel is powered, the clock generation tree will be activated unless another block that depends on the clock generation tree is already powered. Powering up a DAC will power the internal modulator as well as the associated processing blocks and the miniDSP_D (AIC3256 only, if applicable). The master clock and audio serial interface (ASI) bus should be active at this point. Register(s): • p0_r63_b7-6 = 11b (power up both DACs)
8. Power up NDAC (sync mode)	To guarantee miniDSP synchronization (if p0_r60_b7 = 1), NDAC should be powered at this point. The sync mode should be used when passing data between miniDSP_A and miniDSP_D. ***Whenever p0_r60_b7 = 1, IDAC = IADC = MDAC * DOSR = MADC * AOSR.*** Register(s): • p0_r11_b7 = 1b (power up NDAC divider)
9. Power up internal amplifiers	To prevent clicks/pop when powering the NDAC divider, the headphone (HP), line (LO), and/or mixer (MA) amplifiers can be powered at this point. Register(s): • p1_r9_b5-0 = xxxxxxb (power up HP/LO/MA)

2 References

For more information about these two operating modes for these devices, see the respective product data sheet (available for download at www.ti.com).

TLV320AIC3206 product data sheet. Literature number SLAS649.
TLV320AIC3256 product data sheet. Literature number SLOS630.

3 Appendix A: Example Sleep Mode Script

It should be noted that, in the end system, the PLL, clock dividers, and other values will differ from this script. It is suggested to use bit-wise operators to mask unrelated bits (see Table 1).

Example 1. Sleep Mode Script

```
# -- TABLE 1, STEP 1: Power down internal amplifiers
w 30 00 01 # Switch to Page 1
w 30 09 00 # Power off HP/LO/MA amps
w 30 3B 00 # Set MicPGA_L Gain D7 = 0
w 30 3C 00 # Set MicPGA_R Gain D7 = 0
# -- TABLE 1, STEP 2a: Set reference to automatic mode
w 30 7b 01 # Set the REF charging time to 40ms (automatic)
# -- TABLE 1, STEP 3: Disable AGCs
w 30 00 00 # Switch to Page 0
w 30 57 00 # Disable LAGC noise gate
w 30 56 00 # Disable LAGC
w 30 5f 00 # Disable RAGC noise gate
w 30 5e 00 # Disable RAGC
# -- TABLE 1, STEP 4: Power off ADCs
w 30 51 00 # Power off LADC/RADC
# f 30 24 x0xxx0xx # Wait for p0_r36_b6/b2 to clear
# -- TABLE 1, STEP 5: Power off DACs
w 30 3F 14 # Power off LDAC/RDAC
# f 30 25 000x000x # Wait for p0_r36_b7-5/3-1 to clear
# -- TABLE 1, STEP 6: Disconnect all output amplifier routings
w 30 00 01 # Switch to Page 1
w 30 0C 00 # Disconnect HPL routings
w 30 0D 00 # Disconnect HPR routings
w 30 0E 00 # Disconnect LOL routings
w 30 0F 00 # Disconnect LOR routings
# -- TABLE 1, STEP 7: Power off additional blocks
w 30 33 00 # Power off MICBIAS
w 30 3A 00 # Disable weak input common mode
w 30 00 00 # Switch to Page 0
w 30 1D 00 # Disable forced ASI output
w 30 1A 01 # Power down CDIV_CLKIN M divider
w 30 1E 01 # Power down BCLK N divider
w 30 43 00 # Disable headset detection
# -- TABLE 1, STEP 8: Power off clock generation tree
w 30 13 08 # Power down MADC = 8
w 30 0C 08 # Power down MDAC = 8
w 30 12 02 # Power down NADC = 2
w 30 0B 02 # Power down NDAC = 2
w 30 05 11 # Power down PLL
# -- TABLE 1, STEP 9a: Configure AVDD
w 30 00 01 # Switch to Page 1
w 30 01 08 # Power down charge pump, keep weak AVDD to DVDD connection disabled
w 30 02 08 # Disable Master Analog Power Control
w 30 01 00 # Enable weak AVDD to DVDD connection
```

4 Appendix B: Example Wake Up from Sleep Script

The script below assumes that analog inputs (already pre-configured) are desired for the ADC channel and headphone and line outputs are used for the DAC channel.

This script is organized to support miniDSP sync mode requirements (that is, NDAC powered after ADC/DAC power up). It should be noted that in the end system, the PLL, clock dividers, and other values will differ from this script. It is suggested to use bit-wise operators to mask unrelated bits (see Table 2).

Example 2. Wake Up from Sleep Script

```
# -- TABLE 2, STEP 1a: Configure AVDD Supply and charge pump
w 30 00 01 # Switch to Page 1
w 30 01 08 #  Disable weak AVDD to DVDD connection
w 30 02 00 #  Enable master analog power control
w 30 01 0a #  Power up charge pump (if ground centered headphone mode is used)
# -- TABLE 2, STEP 2: Power up clock generation tree
w 30 00 00 # Switch to Page 0
w 30 05 91 # Power up PLL
w 30 12 02 # Keep NADC = 2, powered down for sync mode
w 30 13 88 # Power up MADC = 8
w 30 0C 88 # Power up MDAC = 8
# -- TABLE 2, STEP 5: Configure output amplifier routing
w 30 00 01 # Switch to Page 1
w 30 0C 08 # Re-connect LDAC_P to HPL
w 30 0D 08 # Re-connect RDAC_P to HPR
w 30 0E 08 # Re-connect LDAC_P to LOL
w 30 0F 08 # Re-connect RDAC_P to LOR
# -- TABLE 2, STEP 6: Power up ADCs
w 30 00 00 # Switch to Page 0
w 30 51 C0 # Power up LADC/RADC
# -- TABLE 2, STEP 7: Power up DACs
w 30 3F D4 # Power up LDAC/RDAC
# -- TABLE 2, STEP 8: Power up NDAC
w 30 0b 82 # Power up NDAC = 2, sync mode
# -- TABLE 2, STEP 9: Power up internal amplifiers
w 30 00 01 # Switch to Page 1
w 30 09 3c # Power HPs/LOs
```

5 Appendix C: Example Standby Mode Script

It should be noted that, in the end system, the PLL, clock dividers, and other values will differ from this script. It is suggested to use bit-wise operators to mask unrelated bits (see Table 1).

Example 3. Standby Mode Script

```
# -- TABLE 1, STEP 1: Power down internal amplifiers
w 30 00 01 # Switch to Page 1
w 30 09 00 # Power off HP/LO/MA amps
w 30 3B 00 # Set MicPGA_L Gain D7 = 0
w 30 3C 00 # Set MicPGA_R Gain D7 = 0
# -- TABLE 1, STEP 2b: Set reference to forced mode
w 30 7b 05 # Force REF charging time to 40ms
# -- TABLE 1, STEP 3: Disable AGCs
w 30 00 00 # Switch to Page 0
w 30 57 00 # Disable LAGC noise gate
w 30 56 00 # Disable LAGC
w 30 5f 00 # Disable RAGC noise gate
w 30 5e 00 # Disable RAGC
# -- TABLE 1, STEP 4: Power off ADCs
w 30 51 00 # Power off LADC/RADC
# f 30 24 x0xxx0xx # Wait for p0_r36_b6/b2 to clear
# -- TABLE 1, STEP 5: Power off DACs
w 30 3F 14 # Power off LDAC/RDAC
# f 30 25 000x000x # Wait for p0_r36_b7-5/3-1 to clear
# -- TABLE 1, STEP 6: Disconnect all output amplifier routings
w 30 00 01 # Switch to Page 1
w 30 0C 00 # Disconnect HPL routings
w 30 0D 00 # Disconnect HPR routings
w 30 0E 00 # Disconnect LOL routings
w 30 0F 00 # Disconnect LOR routings
# -- TABLE 1, STEP 7: Power off additional blocks
w 30 33 00 # Power off MICBIAS
w 30 3A 00 # Disable weak input common mode
w 30 00 00 # Switch to Page 0
w 30 1D 00 # Disable forced ASI output
w 30 1A 01 # Power down CDIV_CLKIN M divider
w 30 1E 01 # Power down BCLK N divider
w 30 43 00 # Disable headset detection (unless needed)
# -- TABLE 1, STEP 8: Power off clock generation tree
w 30 13 08 # Power down MADC = 8
w 30 0C 08 # Power down MDAC = 8
w 30 12 02 # Power down NADC = 2
w 30 0B 02 # Power down NDAC = 2
w 30 05 11 # Power down PLL
```

6 Appendix D: Example Wake Up from Standby Script

The script below assumes that analog inputs (already pre-configured) are desired for the ADC channel and headphone and line outputs are used for the DAC channel.

This script is organized to support miniDSP sync mode requirements (that is, NDAC powered after ADC/DAC power up). It should be noted that in the end system, the PLL, clock dividers, and other values will differ from this script. It is suggested to use bit-wise operators to mask unrelated bits (see Table 2).

Example 4. Wake Up from Standby Script

```
# -- TABLE 2, STEP 2: Power up clock generation tree
w 30 00 00 # Switch to Page 0
w 30 05 91 # Power up PLL
w 30 12 02 # Keep NADC = 2, powered down for sync mode
w 30 13 88 # Power up MADC = 8
w 30 0C 88 # Power up MDAC = 8
# -- TABLE 2, STEP 5: Configure output amplifier routing
w 30 00 01 # Switch to Page 1
w 30 0C 08 # Re-connect LDAC_P to HPL
w 30 0D 08 # Re-connect RDAC_P to HPR
w 30 0E 08 # Re-connect LDAC_P to LOL
w 30 0F 08 # Re-connect RDAC_P to LOR
# -- TABLE 2, STEP 6: Power up ADCs
w 30 00 00 # Switch to Page 0
w 30 51 C0 # Power up LADC/RADC
# -- TABLE 2, STEP 7: Power up DACs
w 30 3F D4 # Power up LDAC/RDAC
# -- TABLE 2, STEP 8: Power up NDAC
w 30 0b 82 # Power up NDAC = 2, sync mode
# -- TABLE 2, STEP 9: Power up internal amplifiers
w 30 00 01 # Switch to Page 1
w 30 09 3c # Power HPs/LOs
```

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