Application Report
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Coefficient RAM Access Mechanisms

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ABSTRACT

The Texas Instruments new family of audio converters feature enhanced filtering capabilities, which include writing coefficients as needed using a double-buffered coefficient mechanism. This mechanism and other aspects of coefficient memory access are discussed in this application report.

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1 Introduction

For clarity, this application report organizes several devices into two families that share a common coefficient RAM (C-RAM) access mechanism:

- Family 1:
  - TSC2117
  - TLV320AIC3111
  - TLV320AIC3100
  - TLV320AIC3120
  - TLV320DAC3120
  - TLV320DAC3101
  - TLV320DAC3100
  - TLV320AIC36
  - TLV320ADC3101
  - TLV320ADC3001
- Family 2:
  - TLV320AIC3254
  - TLV320AIC3204
  - TLV320AIC3253
  - TLV320AIC3256

Note that some features do not apply to some devices within a family. For instance, the TLV320ADC3101 does not have digital-to-analog converter (DAC) channels, therefore, any mention of DAC channel filtering does not apply for this device. In a similar fashion, the TLV320AIC3204 does not have a programmable miniDSP, therefore, any miniDSP mention does not apply for this device.

Although the C-RAM access mechanism can be the same, some devices differ on the C-RAM size and word length.

The following conventions are used throughout this document:

- miniDSP_D – miniDSP associated with the DAC channel.
- miniDSP_A – miniDSP associated with the analog-to-digital converter (ADC) channel.
- PRB_Px – DAC processing block x, where x denotes any processing block for playback.
- PRB_Ry – ADC processing block y, where y denotes any processing block for recording.
- DAC(s) – it means that a statement applies if an action is performed to one or both DACs.
- DACs – it means that a statement applies if an action is performed to both DACs.
- ADC(s) – it means that a statement applies if an action is performed to one or both ADCs.
- ADCs – it means that a statement applies if an action is performed to both ADCs.
- Page X or Page Y – X refers to the first page of DAC Buffer A whereas Y refers to the first page of ADC Buffer A.

2 C-RAM Access Mechanisms

The following sections explain how to access the C-RAM of both families of audio converters. The two fundamental differences between both families with regards to C-RAM access are:

- Adaptive filtering is only available on the DAC channel for Family 1.
- C-RAM and page locations vary between both families.

Table 1 summarizes the differences between adaptive and nonadaptive modes:

Table 1. Adaptive Mode vs Nonadaptive Mode

Adaptive	Nonadaptive
• Coefficients can be changed as needed. • C-RAM size is half when compared to nonadaptive mode.	• Coefficients cannot be changed as needed (ADCs or DACs need to be powered down for access). • C-RAM size is doubled when compared to adaptive mode.

Refer to Appendix A for register write sequence information.

2.1 DAC C-RAM Access

The DAC channel coefficient memory space (C-RAM) consists of two buffers: Buffer A and Buffer B. Control interface access to these buffers depends on the mode of operation (i.e., nonadaptive or adaptive) as well as the power status of the PRB or the miniDSP_D.

Figure 1 shows three components related to coefficient memory access:

- PRB or miniDSP_D – they access the coefficient memory to perform signal processing. C-RAM access depends on the mode of operation.
- C-RAM – it stores coefficient data to be accessed by either the PRB (or the miniDSP_D) or the control interface.
- Control Interface – the control interface has two multipurpose banks of pages that provide access to the C-RAM buffers. These banks are denoted as Buffer A and Buffer B, although they do not necessarily access the labeled buffers in some modes of operation.

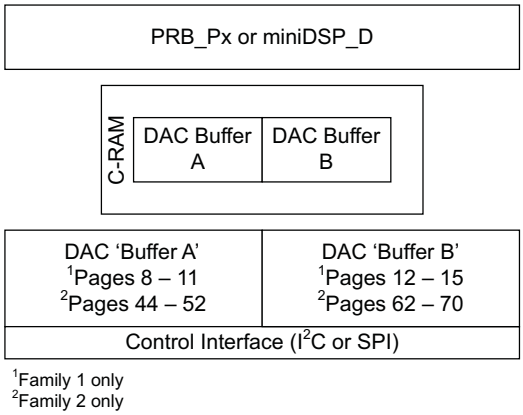


Figure 1. Components Related to DAC C-RAM Access

2.1.1 DAC Channel Nonadaptive Mode, Both Families

The DAC channel nonadaptive mode merges Buffer A and Buffer B into a single large buffer. In this mode, access to these buffers is mutually exclusive – the control interface does not have access to the buffers if the PRB_Px or miniDSP_D has access and vice-versa.

Adaptive Mode is disabled by writing a 0 (zero) to Page X / Register 1, Bit D2.

Table 2 summarizes C-RAM access based on DAC status in nonadaptive mode.

Table 2. DAC Channel C-RAM Access Table – Nonadaptive

DAC Status (1)	PRB_Px or miniDSP_D C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up	Yes (Buffer A and Buffer B)	No (C-RAM registers return 0x00)

(1) See the relevant product data sheet for DAC power-up control and status registers.

This concept is shown in Figure 2. After a reset condition occurs (either a software reset or $\overline{\text{RESET}}$ is released) or both DACs are powered down, the control interface has access to both buffers. Once the DAC(s) is powered up, the control interface loses access to these buffers.

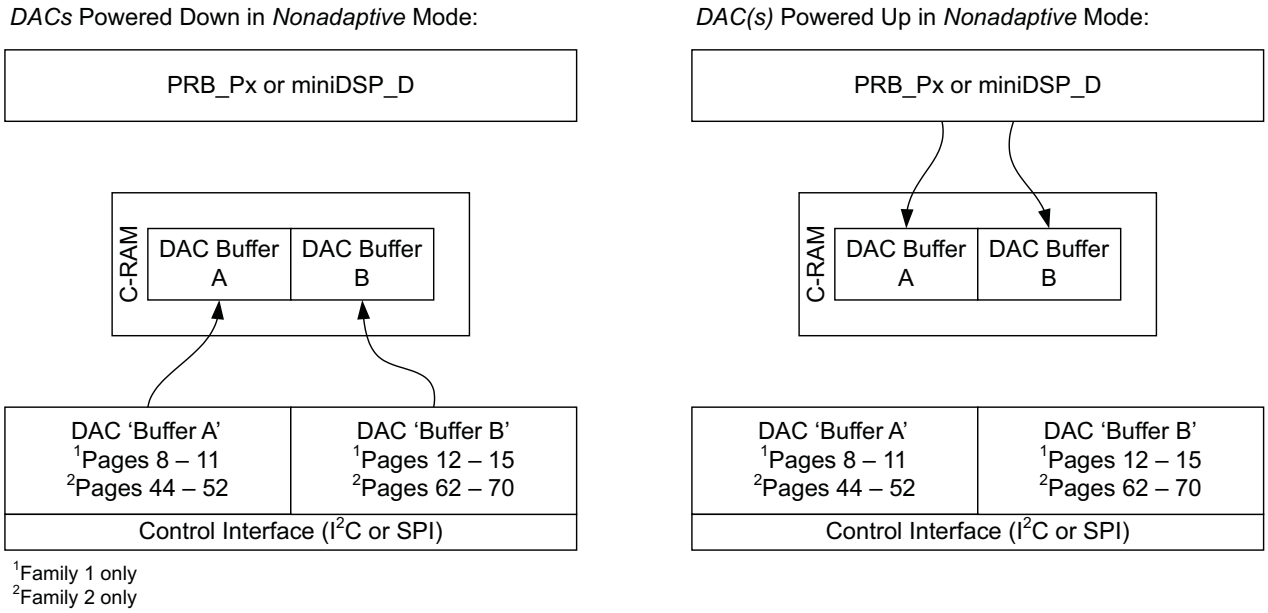


Figure 2. DAC C-RAM Access at Power-Down and Power-Up Modes

2.1.2 DAC Channel Adaptive Mode, Both Families

The DAC channel adaptive mode allows filter coefficients to be changed as needed by using a double buffered scheme. C-RAM access in adaptive mode is similar to the nonadaptive mode when both DACs are powered down. Both banks of pages point to their respective C-RAM buffer, as shown in Figure 3.

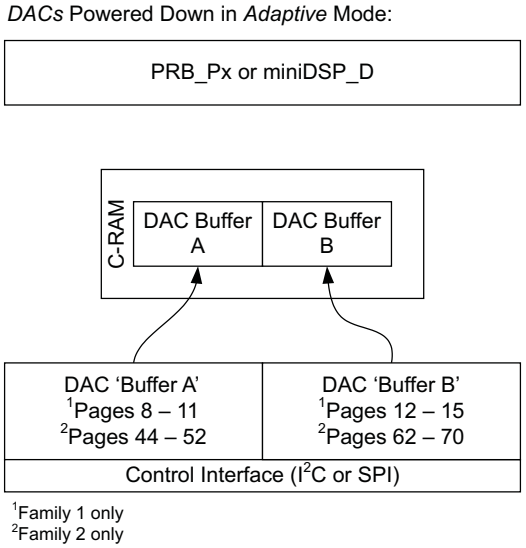


Figure 3. DAC C-RAM Access at Power-Down Mode – Adaptive

However, when the DAC(s) is powered up, the PRB_Px or miniDSP_D has access to one buffer whereas the control interface has access to the other buffer.

Adaptive Mode is enabled by writing a 1 (one) to Page X / Register 1, Bit D2.

Table 3 summarizes C-RAM access in adaptive mode.

Table 3. DAC Channel C-RAM Access Table – Adaptive

DAC(s) Status	PRB_Px or miniDSP_D C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up(1) (pX_r1_b1 = 0)(2)	Buffer A only	Buffer B only
Powered Up (1) (pX_r1_b1 = 1)(2)	Buffer B only	Buffer A only

(1) See the relevant product data sheet for DAC power-up control and status registers.
(2) pX_r1_b1 is short for Page X / Register 1, Bit D1, where X denotes the first page of Buffer A.

Figure 4 illustrates buffer access in adaptive mode when the DAC(s) is powered up. The buffer that the PRB_Px (or miniDSP_D) and the control interface has access to depends on the value of Page X / Register 1, Bit D1 (or pX_r1_b1), where X denotes the first page of Buffer A.

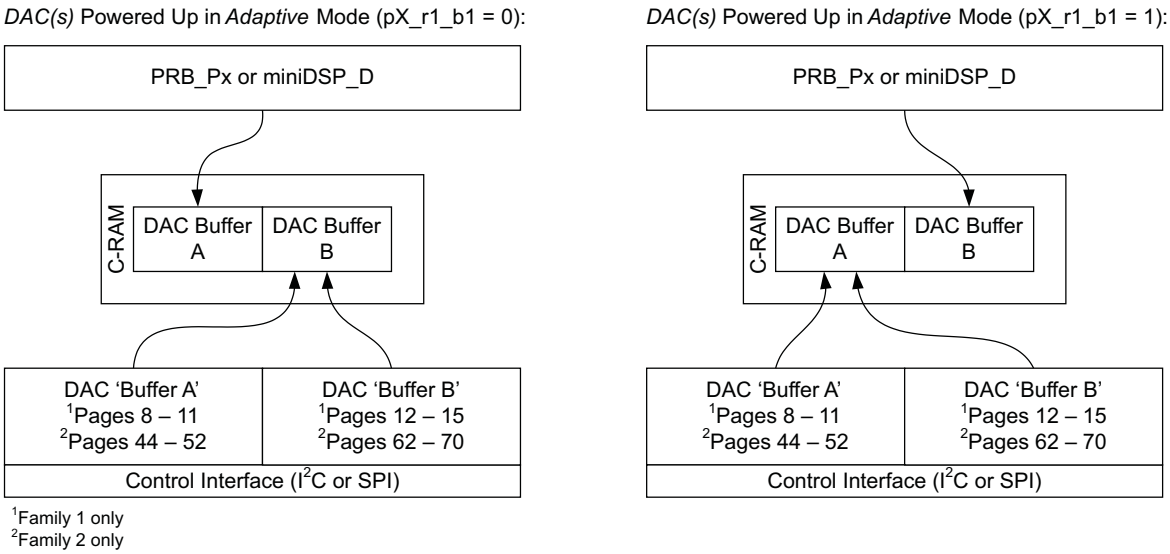


Figure 4. DAC C-RAM Access at Power-Up Mode – Adaptive

Note that both banks of pages point to the same buffer. This means that writing to, for example, coefficient location 1 (or C1) of Buffer A is the same as writing to C1 of Buffer B. This eliminates the need to keep track of which buffer is being written at a time, making the process transparent to the user.

Buffer switching is accomplished by writing a 1 (one) to Page X / Register 1, bit D0. Once this bit is set, the buffer is switched at the end of a frame boundary. To prevent data mismatch between buffers, it is important to wait for this bit to clear by reading the same, especially when using fast communication protocols, such as SPI. Also, the audio bus must be active (externally or internally); otherwise, the buffers do not switch until the bus is activated. See Appendix B for additional use cases.

Figure 5 shows a coefficient write process example using processing block PRB_P2 of the AIC32x4 (Family 2). In this case, the first two left-channel filters (Biquad A and Biquad B) of the biquad chain are being written with coefficients.

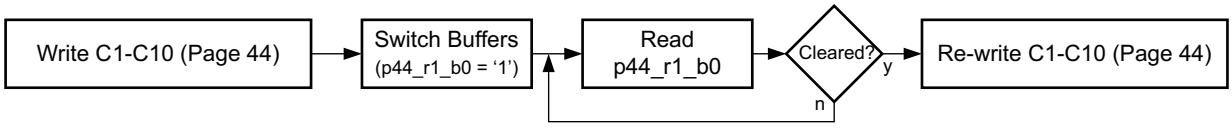


Figure 5. Writing DAC C-RAM Coefficients in Adaptive Mode Example – AIC32x4

C-RAM locations can be read in adaptive mode by reading the corresponding registers. Some algorithms write C-RAM continuously – the most recent data can be obtained by switching the buffers as shown in Figure 6.

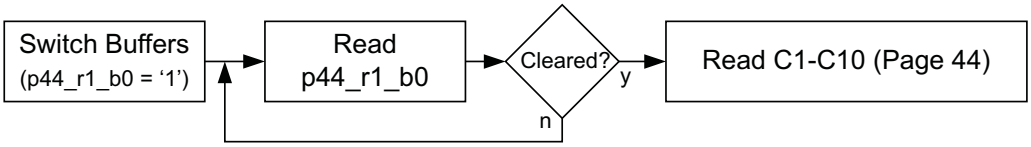


Figure 6. Reading DAC C-RAM Coefficients in Adaptive Mode Example – AIC32x4

2.2 ADC Channel C-RAM Access

The ADC C-RAM access mechanism for Family 1 differs from its DAC C-RAM access mechanism, as it does not feature the double-buffered adaptive scheme. The ADC C-RAM access mechanism for Family 2 is identical compared to its DAC C-RAM access. The following subsections explain these mechanisms in detail.

2.2.1 ADC Channel C-RAM Access - Family 1

The ADC channel C-RAM of Family 1 consists of a single coefficient memory buffer. Access to C-RAM based on ADC power status is shown in Table 4.

Table 4. ADC Channel C-RAM Access Table – Family 1

ADC Status (1)	PRB_Ry or miniDSP_A C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes
Powered Up	Yes	No (C-RAM registers return 0x00)

(1) See the relevant product data sheet for ADC power-up control and status registers.

This concept is shown in Figure 7. After a reset condition occurs (either a software reset or $\overline{\text{RESET}}$ is released) or both ADCs are powered down (one ADC if the device has a mono ADC), the control interface has access to C-RAM. Once the ADC(s) is powered up, the control interface loses access to C-RAM.

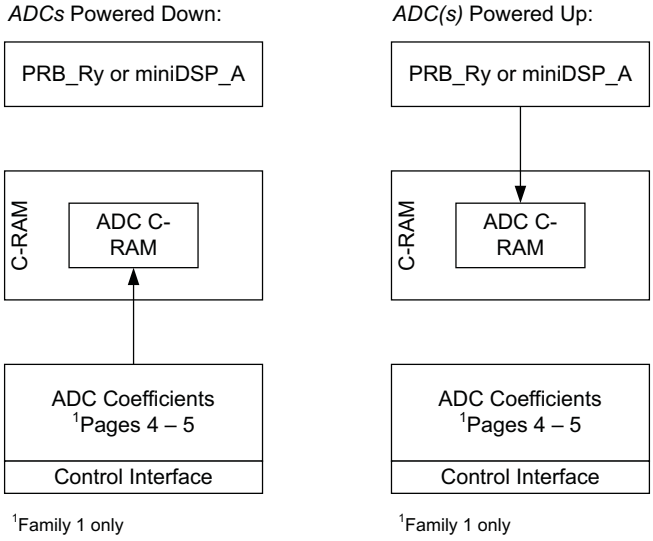


Figure 7. ADC C-RAM Access at Power-Down Mode – Family 1

2.2.2 ADC Channel Nonadaptive Mode - Family 2

The ADC channel nonadaptive mode merges Buffer A and Buffer B into a single large buffer. In this mode, access to these buffers is mutually exclusive – the control interface does not have access to the buffers if the PRB_Ry or miniDSP_A has access and vice-versa.

Adaptive Mode is disabled by writing a 0 to Page Y / Register 1, Bit D2.

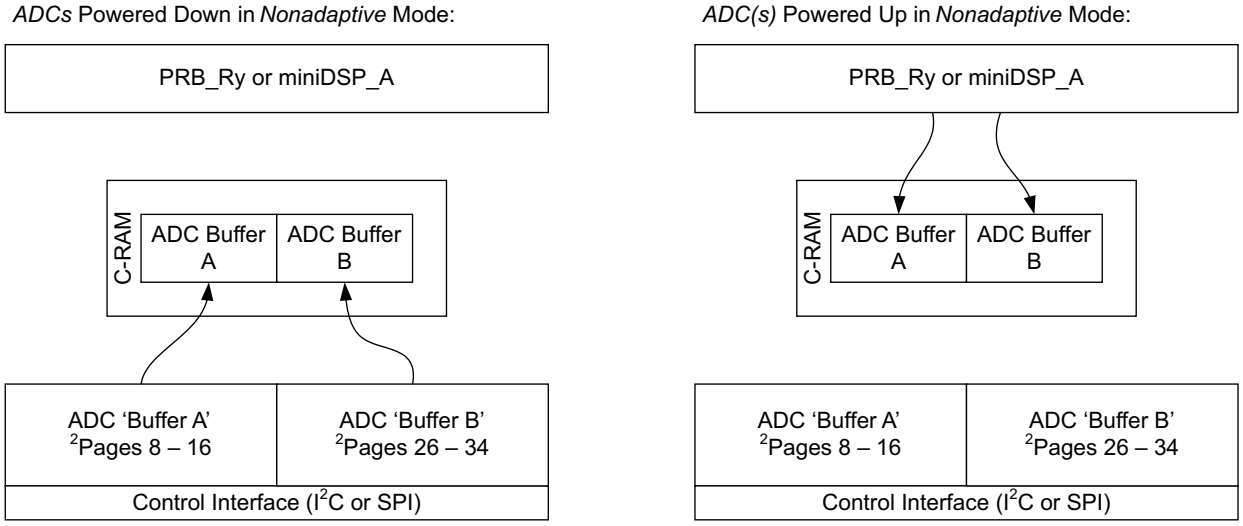
Table 5 summarizes C-RAM access based on ADC status in nonadaptive mode.

Table 5. ADC Channel C-RAM Access Table – Nonadaptive

ADC Status (1)	PRB_Ry or miniDSP_A C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up	Yes (Buffer A and Buffer B)	No (C-RAM registers return 0x00)

(1) See the relevant product data sheet for ADC power-up control and status registers.

This concept is shown in Figure 8. After a reset condition occurs (either a software reset or $\overline{\text{RESET}}$ is released) or both ADCs are powered down, the control interface has access to both buffers. Once the ADC(s) is powered up, the control interface loses access to these buffers.



2Family 2 only

Figure 8. ADC C-RAM Access at Power-Down and Power-Up Modes – Nonadaptive

2.2.3 ADC Channel Adaptive Mode - Family 2

The ADC channel adaptive mode allows filter coefficients to be changed as needed by using a double-buffered scheme. C-RAM access in adaptive mode is similar to the nonadaptive mode when both ADCs are powered down. Both banks of pages point to their respective C-RAM buffer, as shown in Figure 9.

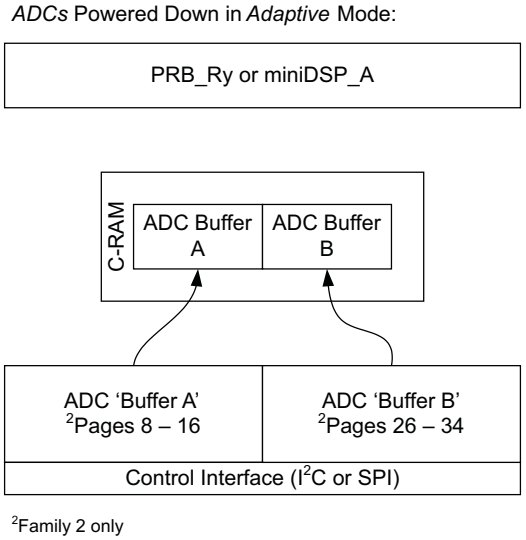


Figure 9. ADC C-RAM Access at Power-Down Mode – Adaptive

However, when the ADC(s) is powered up, the PRB_Ry or miniDSP_A has access to one buffer whereas the control interface has access to the other buffer.

Adaptive Mode is enabled by writing a 1 to Page Y / Register 1, Bit D2.

Table 6 summarizes C-RAM access in adaptive mode.

Table 6. ADC Channel C-RAM Access Table – Adaptive

ADC(s) Status	PRB_Ry or miniDSP_A C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up(1) (pY_r1_b1 = 0)(2)	Buffer A only	Buffer B only
Powered Up (1) (pY_r1_b1 = 1)(2)	Buffer B only	Buffer A only

(1) See the relevant product data sheet for ADC power-up control and status registers.
(2) pY_r1_b1 is short for Page Y / Register 1, Bit D1, where Y denotes the first page of Buffer A.

Figure 10 illustrates buffer access in adaptive mode when the ADC(s) is powered up. The buffer that the PRB_Ry (or miniDSP_A) and the control interface has access to depends on the value of Page Y / Register 1, Bit D1 (or pY_r1_b1), where Y denotes the first page of Buffer A.

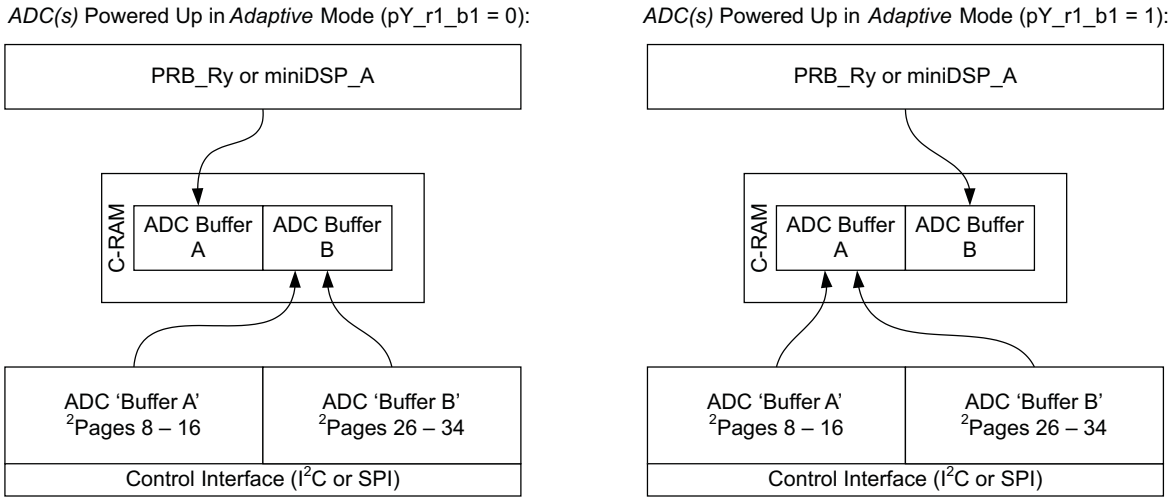


Figure 10. ADC C-RAM Access at Power-Up Mode – Adaptive

Note that both banks of pages point to the same buffer. This means that writing to, for example, coefficient location 1 (or C1) of Buffer A is the same as writing to C1 of Buffer B. This eliminates the need to keep track of which buffer is being written at a time, making the process transparent to the user.

Buffer switching is accomplished by writing a 1 to Page Y / Register 1, bit D0. Once this bit is set, the buffer is switched at the end of a frame boundary. To prevent data mismatch between buffers, it is important to wait for this bit to clear by reading the same, especially when using fast communication protocols, such as SPI. Also, the audio bus must be active (externally or internally); otherwise, the buffers does not switch until the bus is activated.

Figure 11 shows a coefficient write process example using processing block PRB_R2 of the AIC32x4 (Family 2). In this case, the first two left-channel filters (Biquad A and Biquad B) of the biquad chain are being written with coefficients. See Appendix B for additional use cases.

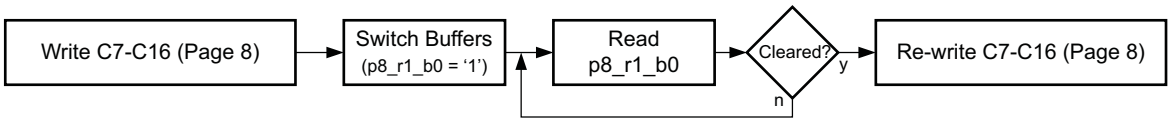


Figure 11. Writing ADC C-RAM Coefficients in Adaptive Mode Example – AIC32x4

C-RAM locations can be read in adaptive mode by reading the corresponding registers. Some algorithms write C-RAM continuously – the most recent data can be obtained by switching the buffers as shown in Figure 12.

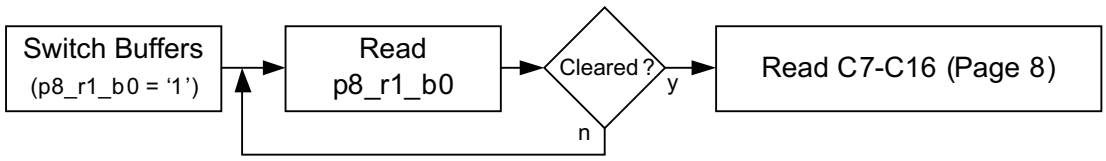


Figure 12. Reading ADC C-RAM Coefficients in Adaptive Mode Example – AIC32x4

3 References

1. *TLV320AIC3254, Ultra Low Power Stereo Audio Codec With Embedded miniDSP* data sheet (SLAS549)
2. *TLV320AIC3204, Ultra Low Power Stereo Audio Codec* data sheet (SLOS602)
3. *TLV320AIC3111, Low-Power Audio Codec With Embedded miniDSP and Stereo Class-D Speaker Amplifier* data sheet (SLAS644)
4. *TLV320ADC3101, Low Power Stereo ADC With Embedded miniDSP for Wireless Handsets and Portable Audio* data sheet (SLAS553)
5. *TLV320ADC3001, Low Power Stereo ADC for Wireless Handsets and Portable Audio* data sheet (SLAS548)
6. *TLV320AIC36, Low Power Stereo Audio Codec With Embedded miniDSP* data sheet (SBAS387)
7. *TSC2117, Low-Power Audio Codec With Embedded miniDSP, Stereo Class-D Speaker Amplifier, and Smart Four-Wire Touch-Screen Controller* data sheet (SLAS550)
8. *TLV320AIC3100, Low-Power Audio Codec With Audio Processing and Mono Class-D Amplifier*,(SLAS667)
9. *TLV320AIC3120, Low-Power Mono Audio Codec With Embedded miniDSP and Mono Class-D Speaker Amplifier*, (SLAS653)
10. *TLV320DAC3120, Low-Power Audio DAC with miniDSP and 2.5W Mono Class-D Speaker Amplifier*, (SLAS659)
11. *TLV320DAC3100, Low-Power Stereo Audio DAC With Mono Class-D Speaker Amplifier* , (SLAS671)
12. TLV320ADC3101, Low Power Stereo Audio CODEC for Portable Audio/Telephony, data sheet (SLAS520E)
13. *TLV320AIC3253, Ultra Low Power Stereo Audio Codec With Embedded miniDSP* (SLOS631)
14. *TLV320AIC3256, Ultra Low Power Stereo Audio Codec with Embedded miniDSP* (SLOS630a)
15. *Design and Configuration Guide for the TLV320AIC32x4 Audio Codecs* application report (SLAA404)

Appendix A Register Write Sequence

When the ADCs and DACs are powered down, the control interface (i.e. I^2C or SPI) has full access to both Buffer A and Buffer B. C-RAM configuration must be done before powering up the ADC(s) and/or DAC(s). Figure 13 shows a typical register write sequence. Strictly speaking, the DAC adaptive mode (Page X / Register 1, bit D2) and the ADC adaptive mode (Page Y / Register 1, bit D2) bits must be configured before powering up the ADC(s) and/or the DAC(s).

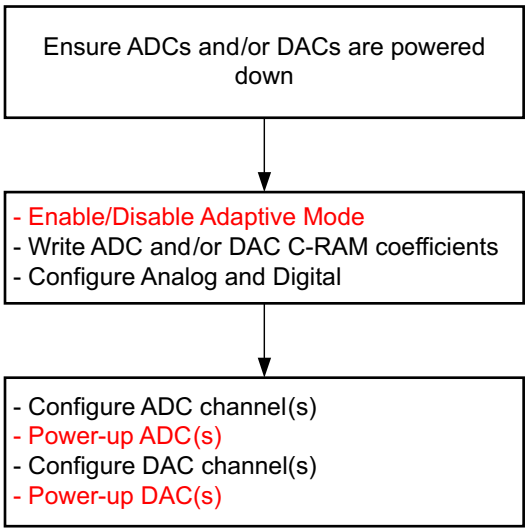


Figure 13. Generalized Configuration Flowchart

Appendix B Additional Adaptive Mode Use Cases

In adaptive mode, C-RAM buffers are typically written as mirrored images in which the user writes the same data to both buffers, keeping them synchronized. However, there are some use cases where it may be desired to have a different set of coefficients between Buffer A and Buffer B. This is useful when having a large set of filter coefficients for two different frequency responses. Instead of writing a new set of coefficients each time a new frequency response is desired, both sets of coefficients can be pre-written before device power-up and its response can be changed by switching buffers. Figure 14 shows such an example, where Buffer A and Buffer B have different coefficient data.

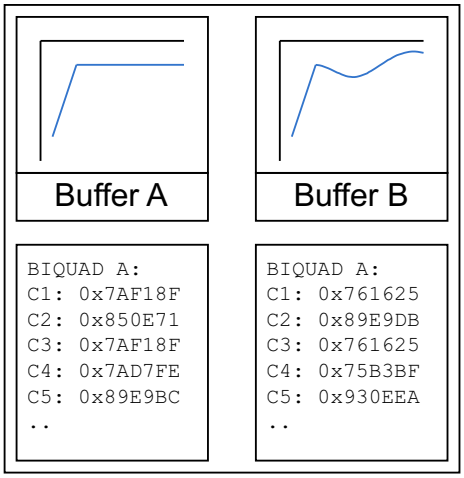


Figure 14. Different Set of Coefficients Between Buffers A and B (AIC32x4)

The first time an ADC or DAC is powered up in adaptive mode, the PRB or miniDSP will have access to Buffer A.

Revision History

This revision history highlights the changes made to the SLAA425 application report.

SLAA425 Revision History

Version	Additions/Modifications/Deletions
SLAA425	Initial release
SLAA425A	Editorial fixes
SLAA425B	Added adaptive mode C-RAM read examples
SLAA425C	Editorial fixes
SLAA425D	Added Appendix A and B Added additional information to tables 2, 4 and 5 Changed PRB_Rx to PRB_Ry in section 2.2.2 Changed PRB_Px to PRB_Ry, 'DAC Status' to 'ADC Status' in table 5 and miniDSP_D to miniDSP_A Changed PRB_Py to PRB_Ry and 'DAC(s) Status' to 'ADC(s) Status' in table 6 Added additional part numbers to the Introduction

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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