Application Report
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An Accurate Thermal-Evaluation Method for the TLV62065

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ABSTRACT

The increase of power density has resulted in the need for accurate measurement of die junction temperature. This application report is a basic overview of thermal evaluation and provides an accurate evaluation method of junction temperature in a real application. The evaluation method described in this application is confirmed with bench measurements. This method is proven to be easy to use and have good accuracy and relevance to real applications.

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1 Introduction

As power densities increase, the amount of heat generated on the silicon imposes significant challenges to thermal management. Temperature becomes a more dominant factor in device performance and reliability. Therefore, the meticulously assessment of the thermal-management design of each device is important of the device to perform safely under the intended operating conditions and environments.

However, thermal evaluation in the system-level of an electronic circuit board is generally a difficult task. This type of evaluation requires knowledge of the major heat dissipaters in the system, the environmental conditions, some theoretical calculations, and some amount of guesswork. Because of this guesswork and uncertainty, the tolerance on accurate junction-temperature measurement and prediction is typically poor. The purpose of this application report is to minimize the guesswork required and deliver a more accurate method of thermal evaluation.

2 Thermal Metrics in the Data Sheet

2.1 JEDEC PCB Specifications

Many thermal metrics exist for semiconductor and integrated circuit (IC) packages. These thermal metrics are often misapplied by users who try to use the metrics to estimate junction temperatures in their systems. The thermal resistance ($R_{\theta JA}$ which is from junction to ambient and $R_{\theta JC}$ which is from junction to case) in a data sheet is a measurement of the thermal performance of an IC package mounted on a specific test board as listed in Table 1. Sometimes, however, the conditions outlined in the JEDEC documentation are not followed and the deviations from the standards are not documented. These test board variations can have an effect on the measured values of thermal resistance. Therefore, unless test conditions are reported with the $R_{\theta JA}$ and $R_{\theta JC}$ value, these conditions should be used of thermal evaluation or calculation. Ideally, the thermal performance of a TI device can be compared to a device from another company which is true when both companies use a standardized test to measure $R_{\theta JA}$, such as that specified by JEDEC in the EIA/JESD 51 series of documents. The TLV62065 device used in this application report follows the high-K standard.

Table 1. Critical PCB Design Factors for JEDEC 1s and 2s2p Test Boards

TEST BOARD DESIGN	JEDEC LOW-K 1s (inch)	JEDEC HIGH-K 2s2p (inch)
Trace thickness	0.0028	0.0028
Trace length	0.98	0.98
PCB thickness	0.062	0.062
PCB width	4	4
PCB length	4.5	4.5
Power-plane and ground-plane thickness	No internal copper planes	0.0014 (2 planes)

2.2 Estimating the Junction Temperature by Thermal Metric

This section defines specific thermal metrics. Table 2 lists the TLV62065 thermal metrics.

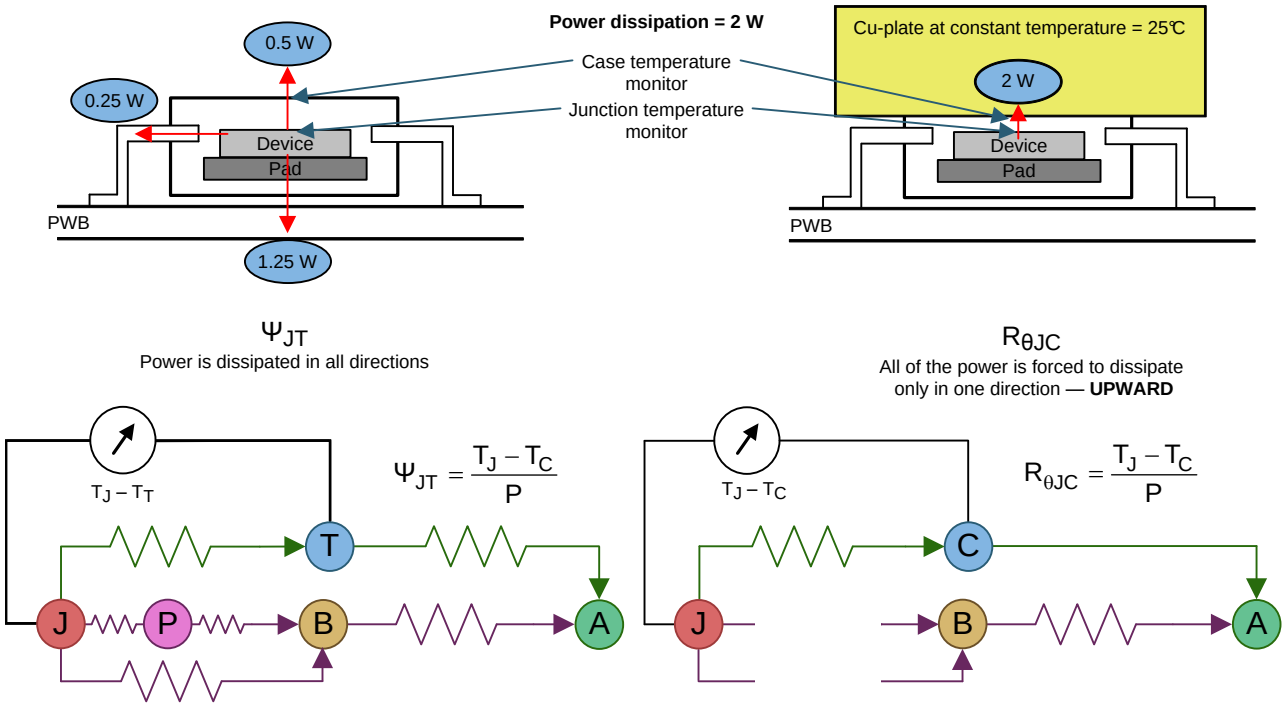
Table 2. TLV62065 Thermal Metrics

THERMAL METRIC		TLV62065	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	
ψ_{JT}	Junction-to-top characterization parameter	12.8	
ψ_{JB}	Junction-to-board characterization parameter	2.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	36	

Thermal Resistance — is the temperature drop from the packaged device to the primary heat-sink per watt of power dissipated in the package. The primary heat sink may be the ambient air, the PCB itself, or a heat sink that is mounted on the package. Thermal resistance is denoted by the symbol $R_{\theta Jx}$ (or ThetaJx) where *x* denotes the external reference point where the temperature is measured.

Characterization Parameter — is different from thermal resistance because the referenced external temperature is not the ultimate heat sink for the package. A thermal characterization parameter can be used to estimate junction temperatures for a device in the end-use environment. A thermal parameter is denoted by the symbol ψ_{Jx} (or PsiJx) where *x* denotes the referenced point where the temperature is measured.

Figure 1 shows the measurement of ψ_{JT} and $R_{\theta JC}$.



NOTE: A = Ambient, B = Board, C = Case, J = Junction, P = Pin

Figure 1. Measurement of Ψ_{Jx} and $R_{\theta Jx}$

$R_{\theta Jx}$ is a variable function of the package and many other system-level factors such as the design and layout of the printed circuit board (PCB) on which the device is mounted. In effect, the test board is a heat sink that is soldered to the leads of the device. Changing the design or configuration of the test board also changes the heat flow and therefore the measured value of $R_{\theta Jx}$.

The use of Equation 1 to calculate $R_{\theta Jx}$ results in highly inaccurate values.

$$T_J = T_x + R_{\theta Jx} \times P \quad (1)$$

where

- T_J = junction temperature
- T_x = the point of the temperature to be calculation
- P = power

$R_{\theta Jx}$ is not a characteristic of only the package but of the package, PCB, and other environmental factors. Best practice is to use $R_{\theta Jx}$ as a comparison of the thermal performance of a package between different companies. For example, if TI reports a $R_{\theta Jx}$ of 100°C/W for a similar package for which a competitor reports 125°C/W, the TI device will likely run 20% cooler in an application than the device of the competitor.

In an attempt to provide a more practical thermal metric to estimate junction temperatures in real application from measured case and board temperatures, a new thermal metric, Ψ_{Jx}, has been adopted by the industry (EIA/JESD 51-2). Ψ_{Jx} is defined as dividing the thermal gradient between the junction temperature and surface temperature by the dissipated power. The heat energy generated by the test die is allowed to flow normally along preferential thermal conduction paths. The quantity of heat flowing from the die to the surface temperature is actually unknown in the measurement, but is assumed to be the total power of the device for the purposes of Ψ_{Jx} calculation. However, this assumption is invalid and when calculated with Equation 2, Ψ_{Jx} becomes a very useful number because the experimental configuration is much like the application environment of the IC package. As such, the amount of energy flowing from the die to the top of the package during test is similar to the partitioning of the energy flow in an application environment.

$$T_J = T_x + \Psi_{Jx} \times P \quad (2)$$

As previously mentioned, Ψ_{Jx} is used to accurately estimate the junction temperature of the semiconductor device. If the top case temperature and component power dissipation can be estimated, the junction temperature can be calculated using Equation 2.

The TLV62065 device was selected as for verification. Table 3 lists the TLV62065 specifications based on the standard evaluation module (EVM). See Appendix A for an overview of the TLV62065EVM.

Table 3. TLV62065 Specifications

PARAMETER		VALUE
V_I	Input voltage	3.3 V
V_O	Output voltage	1 V
I_O	Output current	1 A to 2 A

NOTE: The junction-temperature measurement is based on the ratio of the P-N junction forward voltage as described in the following paragraph.

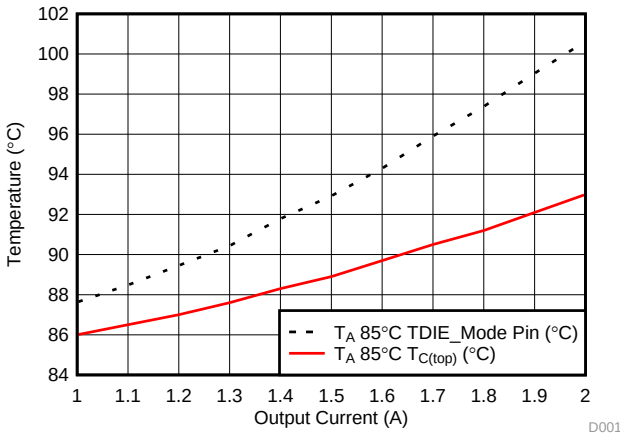


Figure 2. TLV62065 Thermal Measurement

The power loss of the TLV62065 device is obtained from the overall efficiency performance and because the assumed power loss is only generated by the device. Table 4 lists the tested results of the power loss for the specification of V_I = 3.3 V and V_O = 1 V.

Table 4. Power Loss Versus Load

POWER LOSS (W)	LOAD (A)
0.429	1
0.591	1.2
0.808	1.5
1.151	1.8
1.390	2

Table 2 lists the thermal resistance and characterization parameters. Based on these parameters, Figure 3 shows the various calculations based on the measured ambient and top case temperatures. The calculation using ψ_{JT} is much closer to the real measured data.

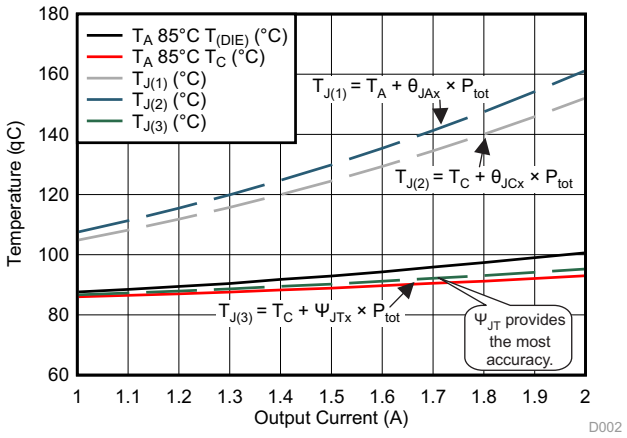


Figure 3. Thermal Calculation with $R_{\theta Jx}$ and ψ_{Jx}

2.3 Accurate Thermal Measurement of the Die Level

2.3.1 P-N Junction Versus Temperature

The ideal measurement method of junction temperature is to monitor the device temperature as close as possible to the heat source. One method is to place a temperature sensor very close to the semiconductor junction and measure the sensor output signal. This method is straightforward, but there are physical limitations to this technique because of the size of the sensor inside the die.

A better method is to use the junction as a temperature sensor. With most materials, a strong correlation exists between the forward voltage drop and the temperature of that junction. This relationship is nearly linear for most devices. Equation 3 is the mathematical expression.

$$T_J = T_{(O)} + m \times V_F \quad (3)$$

where

- T_J = junction temperature (°C)
- m = slope (°C/V)
- V_F = forward voltage drop
- $T_{(O)}$ = Temperature at 0°C

NOTE: The slope, m, is a device-specific parameter.

At a given temperature, $T_{J(X)}$, the semiconductor junction will have a specific forward voltage drop, $V_{F(X)}$. If V_F is measured at two different temperatures, the slope, m, and the intercept for a particular junction can be measured as shown in Figure 4.

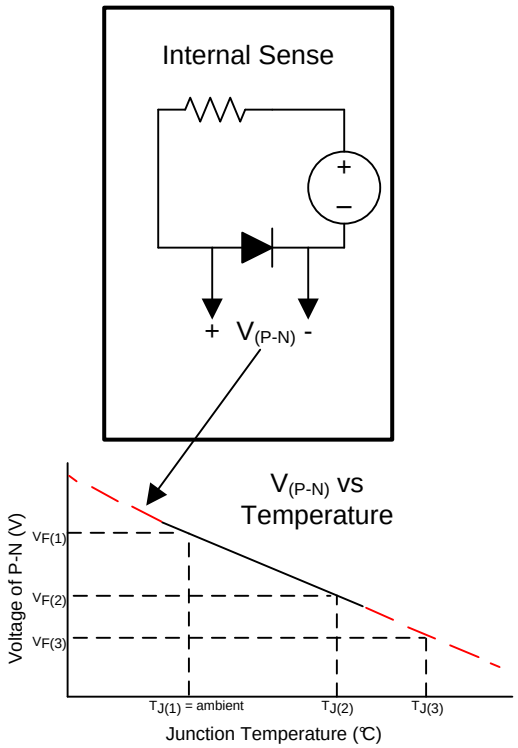


Figure 4. P-N Junction Forward-Voltage Linearity of Temperature

2.3.2 TLV62065 Mode-Pin P-N Junction Voltage Versus Temperature

For the TLV62065 device, the body diode (or ESD diode) of the MODE pin (from the PGND pin to the MODE pin) can be used to measure the die temperature. The pins for measurement should not affect the normal application.

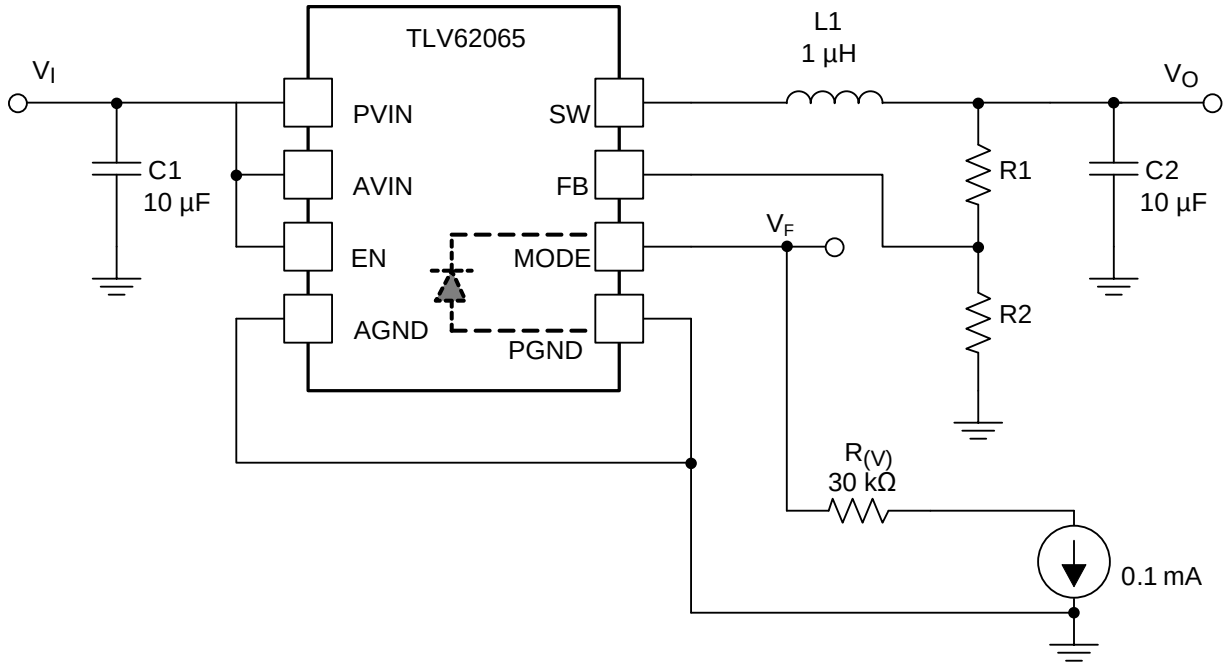


Figure 5. TLV62065 Mode Pin P-N Junction Measurement

For this test, the device-under-test (DUT) is placed in a temperature chamber and connected to the power supply and measurement equipment. Place the DUT into an environmental chamber and set the chamber to an initial temperature (typically at room temperature, such as 25°C). After the junction reaches the thermal equilibrium (monitor the temperature and voltage until the temperature is stable), a very low current is sourced into the DUT and the voltage drop of the P-N junction (from the PGND pin to the MODE pin) is measured.

NOTE: The amplitude of the current that sinks into P-N junction is very important. Delivering a larger amount of power (too much current) may skew the results by heating the junction.

For this setup, use a 100-µA input current (typical), for which the resulting additional temperature could be negligible. The temperature is then increased to a higher value (50°C for example) and the DUT is allowed to reach thermal equilibrium. Then the current is delivered. Voltages recorded at this temperature are labeled the $V_{F(1)}$ at $T_{J(1)}$ (40°C for this example). These steps can be repeated for a number of values and then plotted as voltage versus junction temperature as shown in Figure 6.

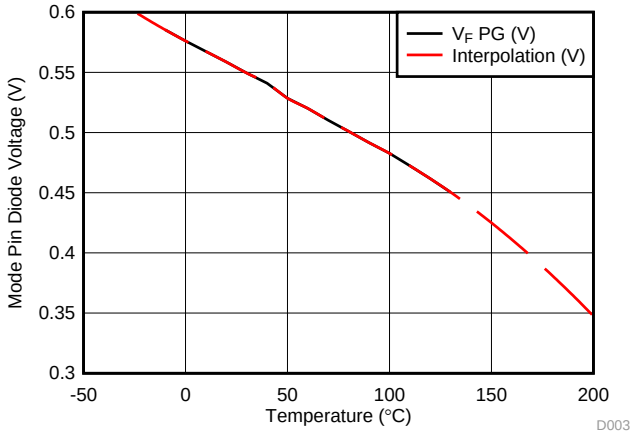


Figure 6. TLV62065 Mode-Pin Diode Voltage Versus Temperature

Equation 4 is a linearized equation for the junction temperature versus forward voltage of the TLV62065 device based on the measured data and curve.

$$T_J\,(°C) = -0.8493 \times V_F\,(mV) + 397.78\,(mV) \quad (4)$$

To evaluate other scenarios, such as variations in PCB layout or environment temperature, measure V_F and use Equation 4 to calculate the actual junction temperature.

2.3.3 Temperature Gradient in the Die

Typically, the temperature is considered to be constant throughout the entire die. However, distinct temperature gradients inside the die have been discovered, specifically in devices with increasing power density.

In the die level, the hottest spot is near the power FET which contributes the highest percentage of the heat. The thermal sensor is also located directly next to the power FET to detect the hottest spot in the application. The most direct method to detect this hot spot is to measure the FET temperature; however, this method has a practical measurement limitation. In real practice, the pin that does not impact normal operation is typically used to monitor the die temperature (such as the MODE pin of the TLV62065 device). Then, temperature gradients between the measured pin and the hottest spot (or thermal sensor) should be considered in order to minimize the tolerance of the real FET temperature. Figure 7 shows the measured pin and thermal sensor (reflecting the FET temperature) location inside the die. A thermal resistance causes the temperature gap.

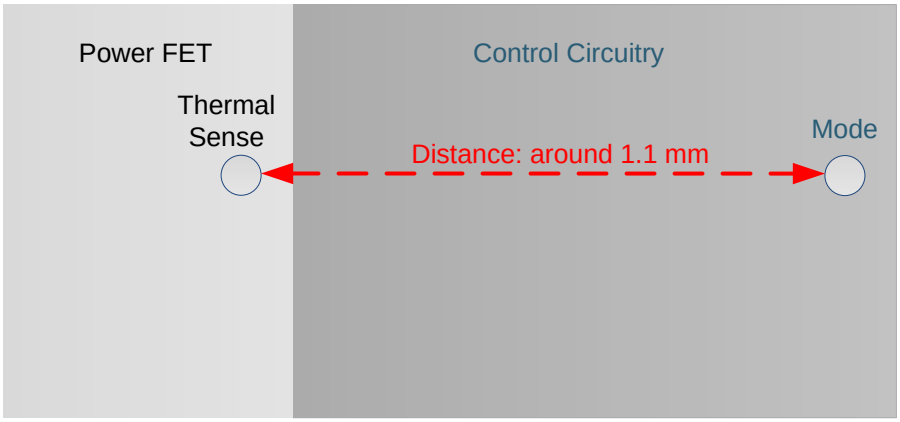


Figure 7. TLV62065 Mode Pin and Thermal Sense Location

2.3.3.1 Thermal Simulation Verification

For a 1-W power loss in the die, the FET temperature (thermal sensor) of the TLV62065 device is 89.29°C and the temperature of the MODE pin is 78.32°C (see Figure 8).

For a 0.5-W power loss, the FET temperature (thermal sensor) is 58.25°C and the temperature of the MODE pin is 52.75°C (see Figure 9).

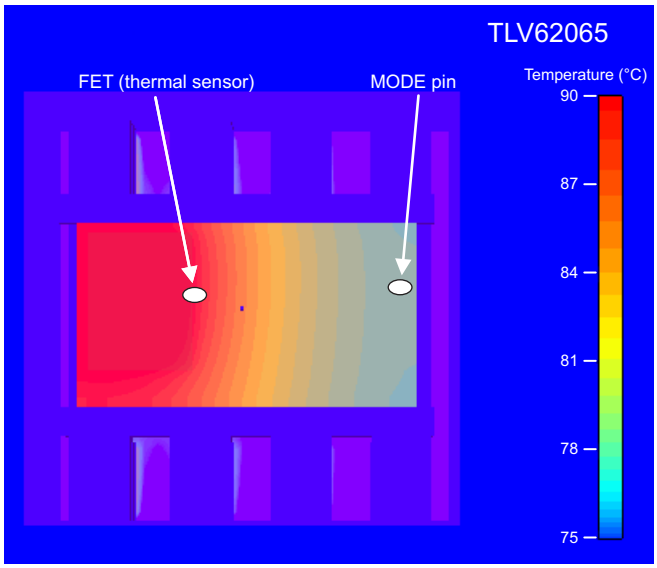


Figure 8. TLV62065 Die Thermal Simulation 1-W Power Loss

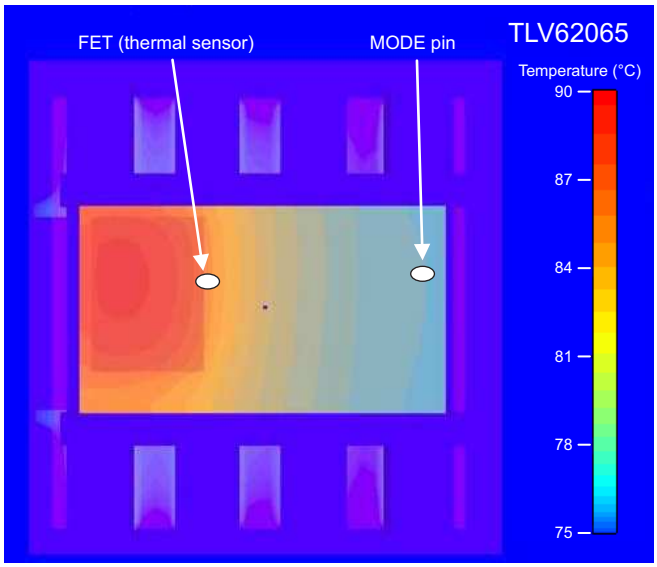


Figure 9. TLV62065 Die Thermal Simulation 0.5-W Power Loss

2.3.3.2 Bench Measurement Verification

At a no-load condition, no power loss is generated in the die and therefore the temperature gap between the FET and MODE pin is almost zero. Heat up the board until thermal protection is triggered (suddenly decreasing the input current) and record the temperature using the symbols $T_{(MODE1)}$ and $T_{(FET1)}$.

For the given power loss, the thermal-sense trip temperature is assumed to be of less variation. The temperature of the MODE pin can be read by measuring the P-N junction voltage. Record the temperature as $T_{(MODE2)}$ and $T_{(FET2)}$ (equal with $T_{(FET1)}$) when thermal protection is triggered. Table 5 lists the measurement of the TLV62065EVM as a result of no load and 1-W power loss.

Table 5. TLV62065 Temperature Measurement (1-W Loss)

NO POWER LOSS		1-W POWER LOSS
$T_{(FET1/FET2)}$ (°C)	$T_{(MODE1)}$ (°C)	$T_{(MODE2)}$ (°C)
147	147	137.5

Based on the simulation result and bench verification, the temperature gradient is approximately 9°C/W between the MODE pin and the thermal sensor (hottest spot in die).

With the given power loss, use Equation 5 to calculate the thermal sensor temperature.

$$T_{(FETx)} = T_{(MODEx)} + 9°C/W \times P_{tot} \quad (5)$$

where

- P_{tot} = total power loss

The power loss can be available based on the overall efficiency of the DC-DC converter. The thermal evaluation would then have less tolerance.

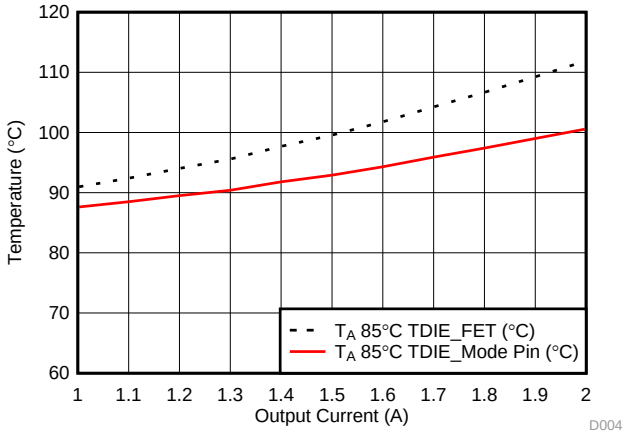


Figure 10. TLV62065 FET and Mode Pin Temperature

With this method, the FET junction temperature of the TLV62065 device is predicted again using the power loss listed in Table 4. The FET temperature is selected based on Figure 10 and the tolerance is lowered further.

3 Conclusion

The thermal metric listed in the device data sheet can be used to estimate the junction temperature while suffering from a large tolerance. To validate the thermal evaluation with less tolerance, the operating junction temperature can be measured directly using the P-N junction linearity with forward voltage. Additionally, the temperature gradient inside the die should be considered. With the method described in this application report, the hot spot across the entire die can be predicted more accurately. The method described in this document was evaluated for accuracy, ease of use, and relevance to a real application. The simulation and bench verification is available using the TLV62065 as an example.

4 About the Author

The author would like to thank Paulo Martin, Oliver Nachbaur, and Gavin Jin for their support on this document.

5 References

1. *PowerPAD™ Thermally Enhanced Package*, SLMA002
2. *Semiconductor and IC Package Thermal Metrics*, SPRA953
3. *Using Forward Voltage to Measure Semiconductor Junction Temperature* (Chonko 2006)
4. *Validation and Application of Different Experimental Techniques to Measure Electronic Component Operating Junction Temperature* by Ohan, Rodgers, Fager, Lehtiniemi, Eveloy, Tiilikka, and Rantala in *IEEE Transactions on Components and Packaging Technology*, Vol 22, No. 2, June 1999

Appendix A PCB Overview

All of the measurements in this application report are based on the standard evaluation module, EVM, for the TLV62065 device. The printed circuit board (PCB) is made up of four layers with a 2-oz copper top layer and a 2-oz copper bottom layer. The two inner layers are 1-oz copper each.

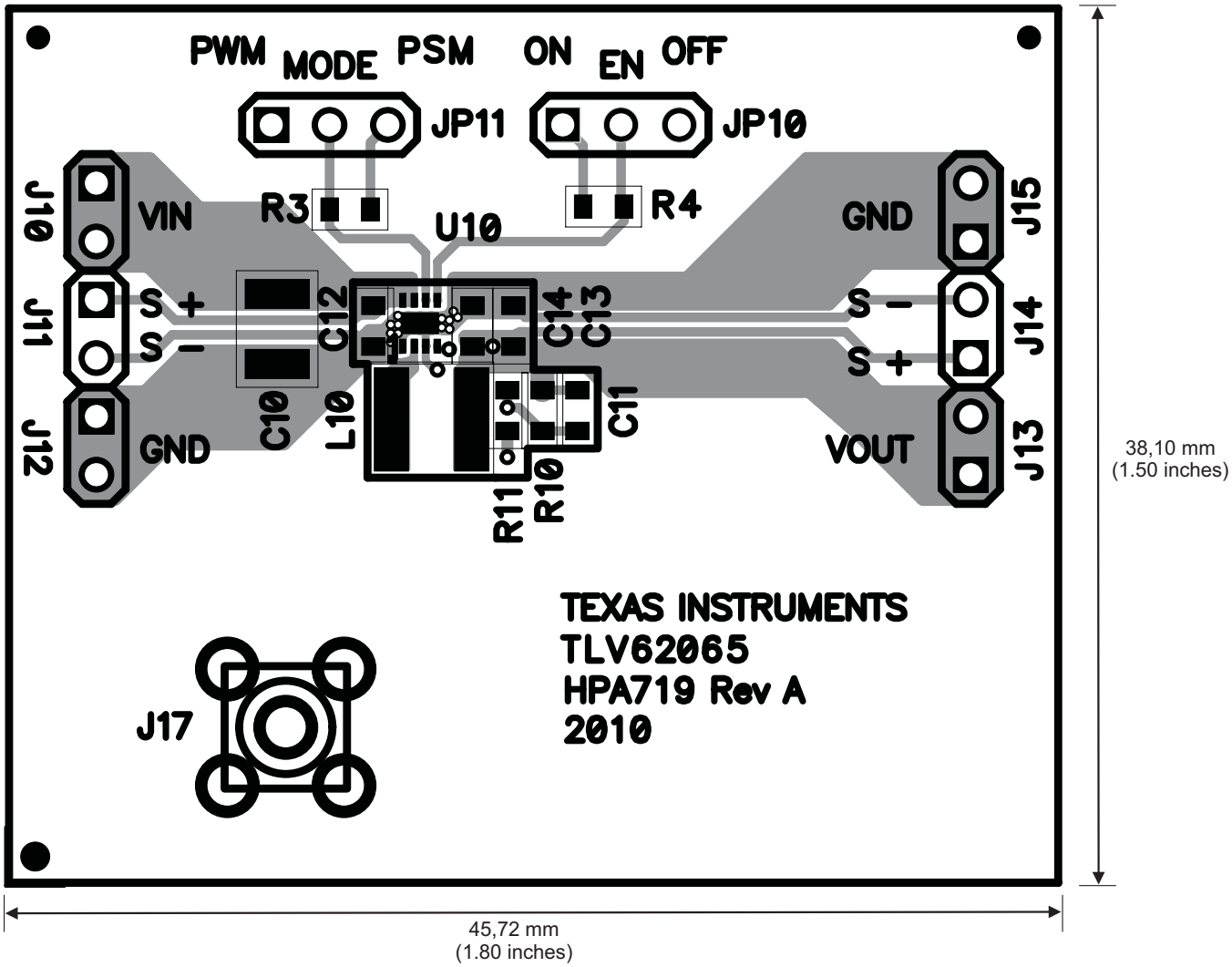


Figure 11. TLV62065EVM

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