Application Report
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TPS6208x and TLV6208x Device Comparison

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Low Power DC/DC

ABSTRACT

This application report presents an overview of the differences among the TPS62080, TPS62081, TPS62082, TPS62080A, TLV62080, TLV62084, and TLV62084A power management integrated circuits (IC). It can assist design engineers in selecting the most suitable IC for their applications. The devices are a family of high frequency synchronous step-down converters, available in a 2-mm × 2-mm QFN package. All devices are pin-to-pin compatible, unless the *Snooze Mode* is used.

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1 Family Members

Table 1. TPS6208x and TLV6208x Family Members

Device	TPS62080	TPS62080A	TLV62080	TLV62084	TLV62084A
Input Voltage Range	2.3 V–6 V	2.3 V–6 V	2.5 V–6 V	2.7 V–6 V	2.7 V–6 V
Output Voltage Range	0.5 V - 4 V TPS62081 fixed 1.8V TPS62082 fixed 3.3V	0.5 V–4 V	0.5 V–4 V	0.5 V–4 V	0.5 V–4 V
Max Output Current	1.2 A	1.2 A	1.2 A	2 A	2 A
Power Good Logic Level (EN = Low)	High Impedance	High Impedance	High Impedance	High Impedance	Low
Output Discharge Resistor	1 kΩ	40 Ω	1 kΩ	1 kΩ	1 kΩ
Power Save Mode	√	√	√	√	√
Snooze Mode	√	√			

2 Feature Explanations

2.1 Power -Good Behavior

All devices from Table 1 have a power-good (PG) output to indicate whether the output voltage has reached its appropriate level or not. The power good goes high impedance once the output is above 95% of the regulated voltage, and is driven low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is an open-drain output and is specified to sink up to 0.5 mA. The power good output requires a pull-up resistor which is recommended to connect to the output voltage of the device. V_{IN} must remain present for the PG pin to stay Low. If not used, the PG pin should be connected to GND but may be left floating.

The TLV62084A device differs from the other devices in how the PG (power good) pin is controlled when the device is disabled, in UVLO, or in thermal shutdown. The TLV62084A holds the PG pin low during these conditions, while the other devices of this family set the PG pin high impedance (floating). This is typically only important in a system that uses multiple voltage rails.

Configuration 1: PG Pin Pulled up to V_{OUT}

Figure 1 and Figure 2 show the difference in PG pin operation when the IC gets disabled without an output load. For these waveforms, the PG pin is connected to the 1.2-V output voltage through a pull-up resistor. In this configuration, there is only a difference in the time it takes for the PG pin to go low. The PG pin goes low in both cases. With an increasing output load, the PG pin goes low faster in the first case.

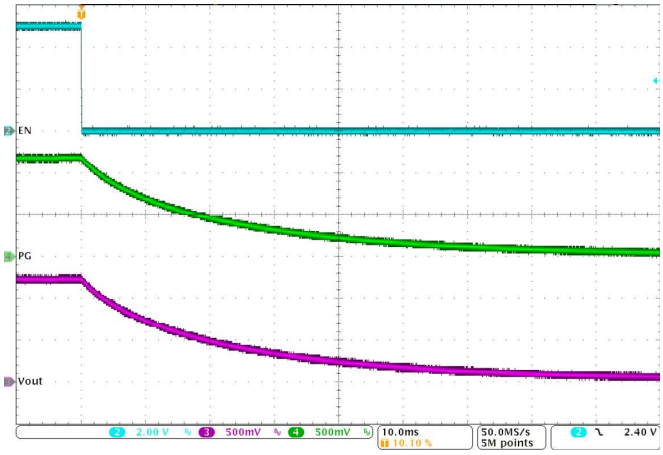

Figure 1. TLV62084 PG Behavior (PG Pulled up to V_{OUT})

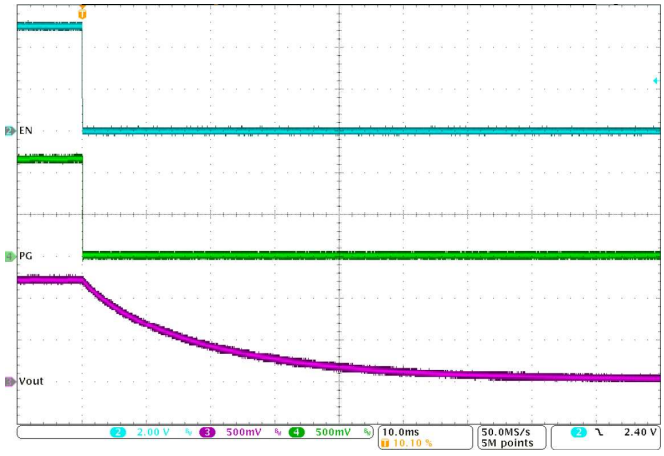

Figure 2. TLV62084A PG Behavior (PG Pulled up to V_{OUT})

Configuration 2: PG Pin Pulled up to a System Rail

Figure 3 and Figure 4 show the difference in PG pin operation when the IC gets disabled without an output load. The PG pin is connected, through a pull-up resistor, to a 5-V system rail which is not the 1.2-V output voltage of the IC. In this configuration, there is an important difference between the performance of the device, as the PG pin goes low with the TLV62084A but remains high with the TLV62084.

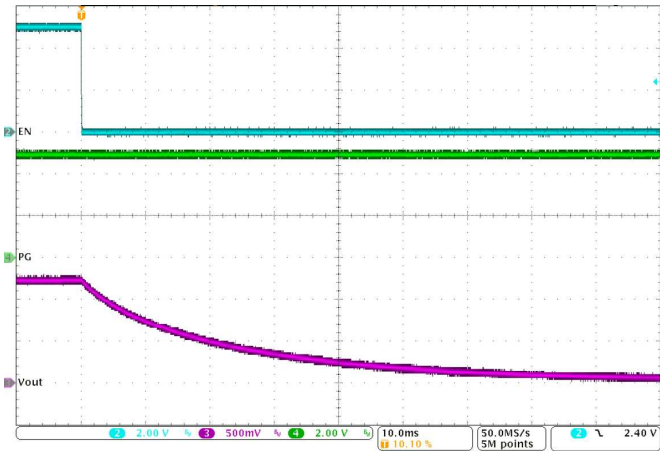

Figure 3. TLV62084 PG Behavior (PG Pulled up to Vsys)

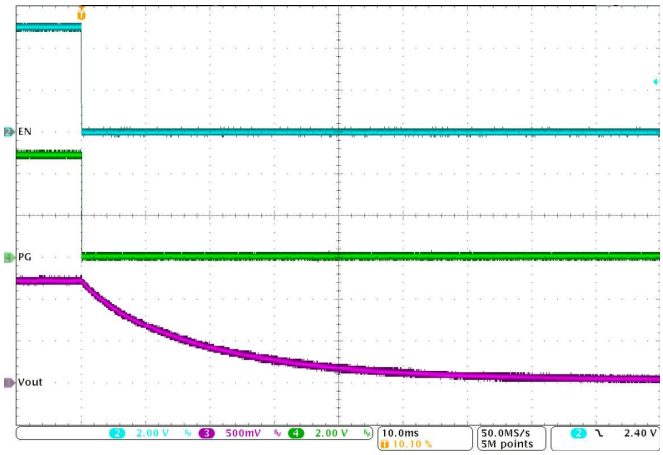

Figure 4. TLV62084A PG Behavior (PG Pulled up to Vsys)

2.2 Output Discharge

Figure 5 and Figure 6 show the difference in output discharge operation when the IC gets disabled without an output load. The TPS62080A has a smaller discharge resistor value and thus the output gets discharged faster compared to the TPS62080.

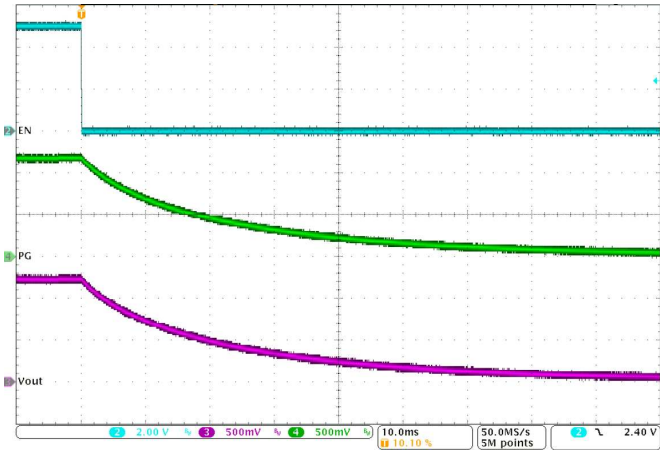

Figure 5. TPS62080 Output Discharge

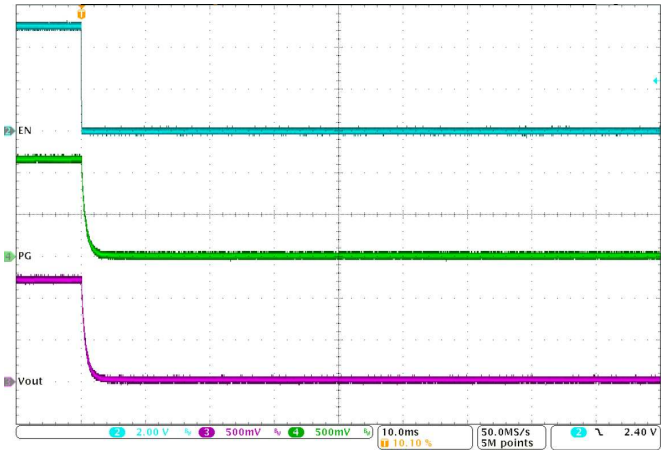

Figure 6. TPS62080A Output Discharge

2.3 Snooze Mode

While all devices from Table 1 have a *Power Save Mode*, only the TPS62080, TPS62081, TPS62082, and TPS62080A implement an additional *Snooze Mode*. If *Snooze Mode* is enabled (by setting the MODE pin to HIGH), the quiescent current consumption of the device is reduced even further compared to the *Power Save Mode*. This results in higher efficiency at lowest output currents. See the TPS62080 data sheet (SLVSAE8) for more details.

3 Conclusion

The TLV62084A device provides easier integration into multi-rail systems due to its PG behavior. For this reason, the TLV62084A device is generally recommended over the TLV62084 since the devices are pin-to-pin compatible. If the *Snooze Mode* is desired, the TPS6208x device can be used.

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