TLV6256x 1.5-A High Efficiency Step-Down Converters in SOT-23 5-Pin Package

1 Features

- 2.7-V to 5.5-V Input Voltage Range
- 1.5-MHz Typical Switching Frequency
- Output Current up to 1.5 A (Max)
- Adaptive On-Time Current Control
- Power Save Mode for Light Load Efficiency
- 50-µA Operating Quiescent Current
- Up to 95% Efficiency
- Over Current Protection
- 95% Maximum Duty Cycle
- Excellent AC and Transient Load Response
- Power Good Output, TLV62566
- Internal Soft Startup of 250 µs (Typ)
- Adjustable Output Voltage
- Thermal Shutdown Protection
- Available in SOT-23 5-Pin Package

2 Applications

- Portable Devices
- DSL Modems
- Hard Disk Drivers
- Set Top Box
- Tablet

3 Description

The TLV62565/6 devices are synchronous step-down converters optimized for small solution size and high efficiency. The devices integrate switches capable of delivering an output current up to 1.5 A.

The devices are based on an adaptive on time with valley current mode control scheme. Typical operating frequency is 1.5 MHz at medium to heavy loads. The devices are optimized to achieve very low output voltage ripple even with small external components and feature an excellent load transient response.

During light load, the TLV62565/6 automatically enter into Power Save Mode at the lowest quiescent current (50 µA typ) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is reduced to less than 1 µA.

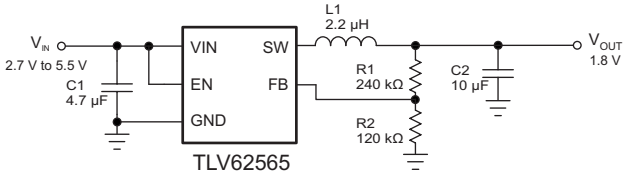
The TLV62565/6 provide an adjustable output voltage via an external resistor divider. The output voltage start-up ramp is controlled by an internal soft start, typically 250 µs. Power sequencing is possible by configuring the Enable (TLV62565) and Power Good (TLV62566) pins. Other features like over current protection and over temperature protection are built-in. The TLV62565/6 devices are available in a SOT-23 5-pin package.

Device Information(1)

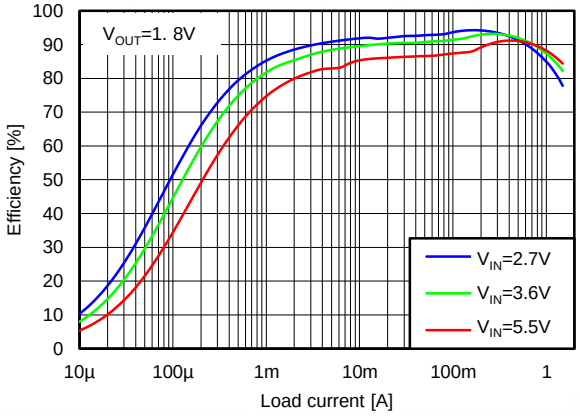
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV62565 TLV62566	SOT-23 (5)	2.90 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Load Current



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2015) to Revision D — **Page**

- Added typical value of valley current limit for the $I_{LIM,LS}$ spec ... 5
- Added typical value of peak current limit for the $I_{LIM,HS}$ spec ... 5
- Updated *Power Save Mode* description ... 8
- Updated *Switch Current Limit* description ... 9
- Updated maximum output voltage setting in the *Setting the Output Voltage* section ... 12
- Added *Receiving Notification of Documentation Updates* section. ... 17

Changes from Revision B (December 2014) to Revision C — **Page**

- Changed device From: TLV62566 to TLV62565 for EN in the *Device Comparison Table* ... 3

Changes from Revision A (November 2014) to Revision B — **Page**

- Added Storage temperature to Absolute Maximum Ratings ... 4
- Changed Handling Ratings to ESD Ratings ... 4
- Deleted Storage temperature from ESD Ratings ... 4
- Changed Thermal Information to Thermal Considerations and moved to Layout section ... 16

Changes from Original (October 2013) to Revision A — **Page**

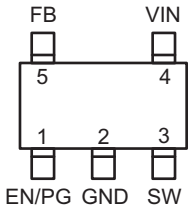
- Changed Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ... 1
- Added "T_A = -40°C to 85°C" to the V_{FB}, Feedback regulation voltage Test Conditions ... 5
- Added V_{FB}, Feedback regulation voltage Test Conditions and values for "PWM operation, T_A = 85°C" ... 5

6 Device Comparison Table

PART NUMBER	FUNCTION
TLV62565	EN
TLV62566	PG

7 Pin Configuration and Functions

5-Pin SOT-23
DBV Package
(Top View)



Pin Functions

PIN			I/O/PWR	DESCRIPTION
NAME	NUMBER			
	TLV62565	TLV62566		
EN	1	—	I	Device enable logic input. Logic HIGH enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
FB	5	5	I	Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
GND	2	2	PWR	Ground pin.
PG	—	1	O	Power Good open drain output. This pin is high impedance if the output voltage is within regulation. It is pulled low if the output is below its nominal value. It is also low when V_{IN} is below UVLO or thermal shutdown triggers.
SW	3	3	PWR	Switch pin connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	4	4	PWR	Power supply voltage input.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PG	–0.3	7	V
	SW	–0.3	V_{IN}+0.3	V
	FB	–0.3	3.6	V
Sink current, I_{PG}	PG		660	µA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage, VIN	2.7		5.5	V
T_A	Operating ambient temperature	–40		85	°C

(1) Refer to the *Application and Implementation* section for further information.

8.4 Thermal Information

THERMAL METRIC(1)		TLV62565, TLV62566 DBV (5 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	208.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_{IN} = 3.6 V, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage		2.7		5.5	V
I_Q	Quiescent current into VIN pin	I_{OUT} = 0 mA, Not switching		50		uA
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.2	2.3	V
	Under voltage lock out hysteresis			200		mV
T_{JSD}	Thermal shutdown	Junction temperature rising		150		°C
	Thermal shutdown hysteresis	Junction temperature falling below T_{JSD}		20		
LOGIC INTERFACE, TLV62565						
V_{IH}	High-level input voltage	2.7 V ≤ V_{IN} ≤ 5.5 V	1.2			V
V_{IL}	Low-level input voltage	2.7 V ≤ V_{IN} ≤ 5.5 V			0.4	V
I_{SD}	Shutdown current into VIN pin	EN = LOW		0.1	1	µA
$I_{EN,LKG}$	EN leakage current			0.01	0.16	µA
POWER GOOD, TLV62566						
V_{PG}	Power Good low threshold	V_{FB} falling referenced to V_{FB} nominal		90%		
	Power Good high thresholdv	V_{FB} risng referenced to V_{FB} nominal		95%		
V_L	Low level voltage	I_{sink} = 500 µA			0.4	V
$I_{PG,LKG}$	PG Leakage current	V_{PG} = 5.0 V		0.01	0.17	µA
OUTPUT						
V_{OUT}	Output voltage		0.6		$D_{MAX}.V_{IN}$	V
V_{FB}	Feedback regulation voltage	PWM operation, T_A = -40°C to 85°C	0.588	0.6	0.612	V
		PWM operation, T_A = 85°C	0.594	0.6	0.606	V
		PFM comparator threshold		0.9%		
I_{FB}	Feedback input bias current	V_{FB} = 0.6 V		10	100	nA
$R_{DS(on)}$	High-side FET on resistance	I_{SW} = 500 mA, V_{IN} = 3.6 V		173		mΩ
	Low-side FET on resistance	I_{SW} = 500 mA, V_{IN} = 3.6 V		105		
$I_{LIM,LS}$	Low-side FET valley current limit		1.5	1.7		A
$I_{LIM,HS}$	High-side FET peak current limit		1.8	2.0		A
f_{SW}	Switching frequency			1.5		MHz
D_{MAX}	Maximum duty cycle			95%		
$t_{OFF,MIN}$	Minimum off time			40		ns

8.6 Typical Characteristics

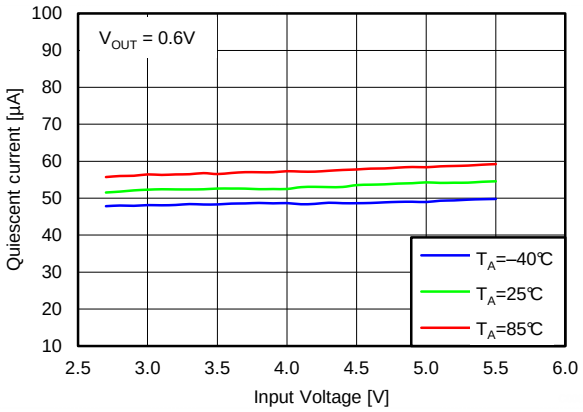


Figure 1. Quiescent Current vs Input Voltage

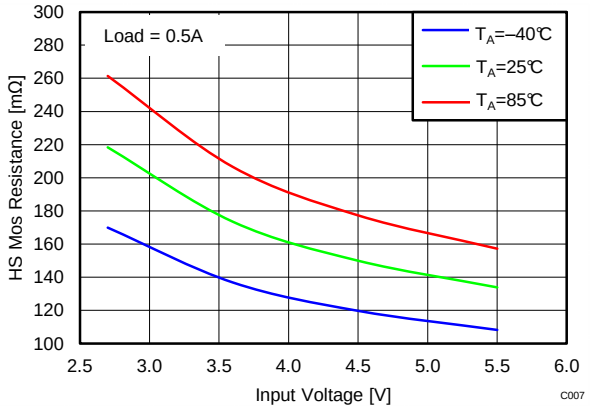


Figure 2. High-Side FET $R_{DS(on)}$ vs Input Voltage

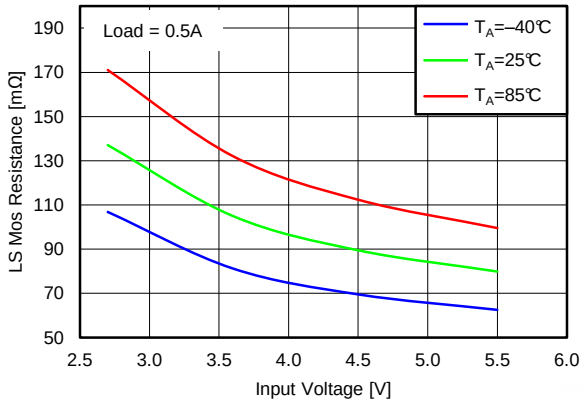


Figure 3. Low-Side FET $R_{DS(on)}$ vs Input Voltage

9 Detailed Description

9.1 Overview

The TLV62565/6 device family includes two high-efficiency synchronous step-down converters. Each device operates with an adaptive on-time control scheme, which is able to dynamically adjust the on-time duration based on the input voltage and output voltage so that it can achieve relative constant frequency operation. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required on time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current. At the beginning of each switching cycle, the high-side switch is turned on and the inductor current ramps up to a peak current that is defined by on time and inductance. In the second phase, once the on time expires, the high-side switch is turned off while the low-side switch is turned on. The current through the inductor then decays until triggering the valley current level determined by the output of the error amplifier. Once this occurs, the on timer is set to turn the high-side switch back on again and the cycle is repeated.

The TLV62565/6 device family offers excellent load transient response with a unique fast response constant on-time valley current mode. The switching frequency changes during load transition so that the output voltage comes back in regulation faster than a traditional fixed PWM control scheme. Internal loop compensation is integrated which simplifies the design process while minimizing the number of external components. At light load currents the device automatically operates in Power Save Mode with pulse frequency modulation (PFM).

9.2 Functional Block Diagrams

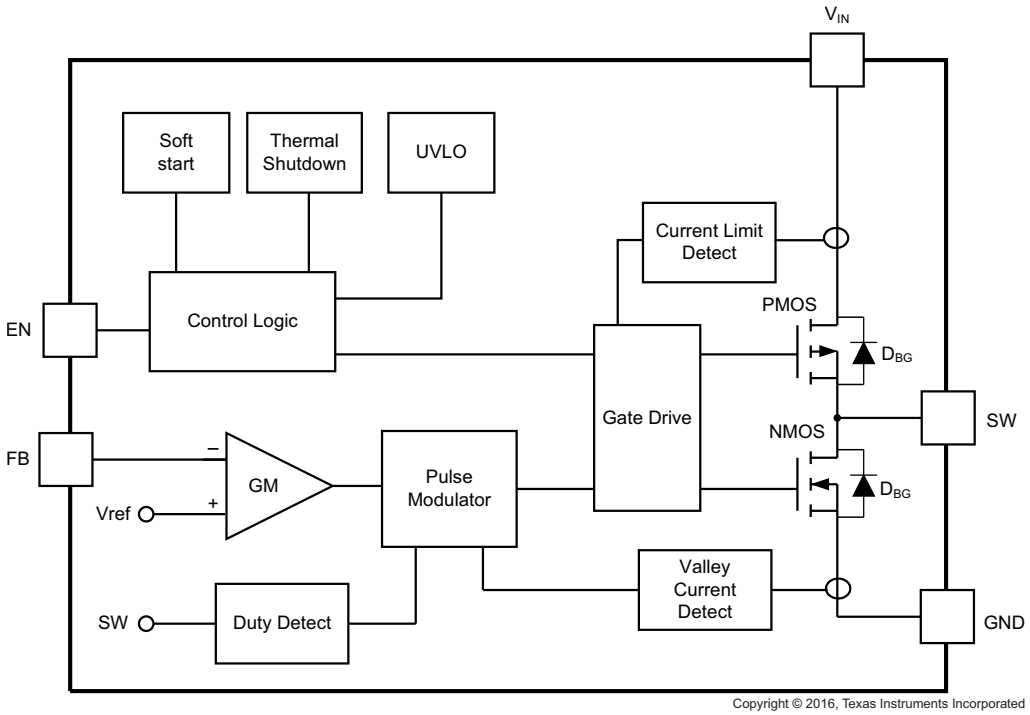


Figure 4. TLV62565 Functional Block Diagram

Functional Block Diagrams (continued)

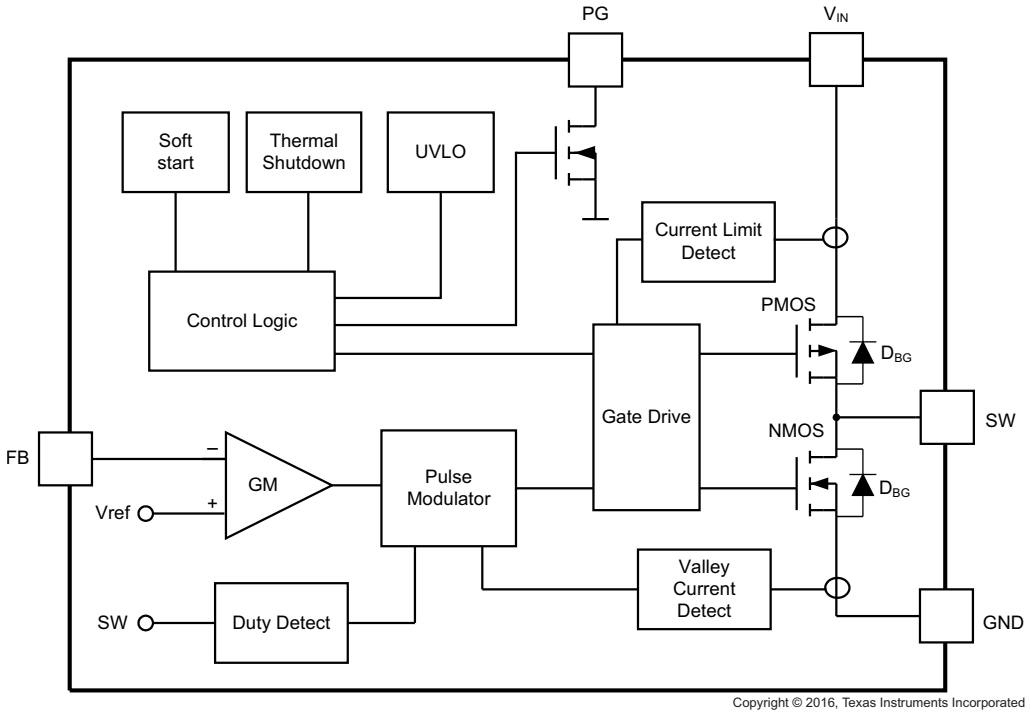


Figure 5. TLV62566 Functional Block Diagram

9.3 Feature Description

9.3.1 Power Save Mode

The device integrates a Power Save Mode with PFM to improve efficiency at light load, as shown in Figure 6

When the inductor current becomes discontinuous, the device enters Power Save Mode. In Power Save Mode, the FB voltage is typically 0.9% higher than the nominal value of 0.6 V. Thus the device ramps up the output voltage with several pulses, and the device stops switching when the output voltage reaches 0.9% above the nominal output voltage.

When the inductor current becomes continuous again, the device leaves Power Save Mode and the FB voltage is back to the norminal value of 0.6 V.

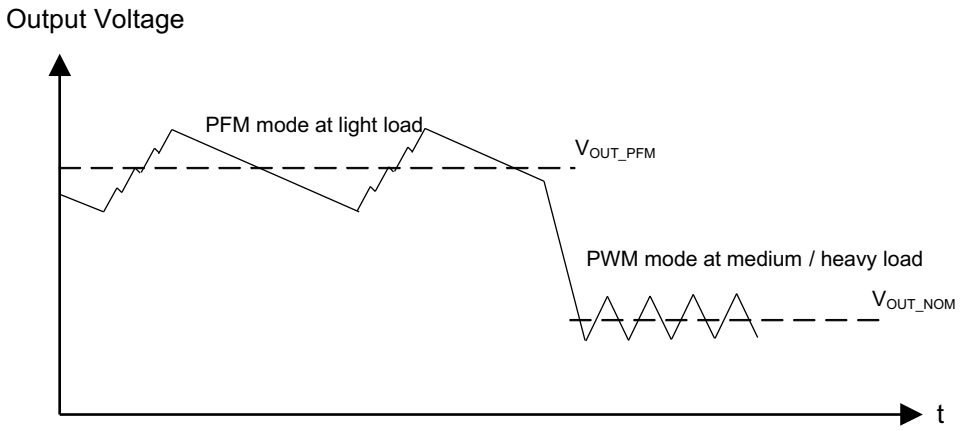


Figure 6. Output Voltage in PFM/PWM Mode

Feature Description (continued)

9.3.2 Enabling/Disabling the Device

The TLV62565 is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

9.3.3 Soft Start

After enabling the device, internal soft-start circuitry monotonically ramps up the output voltage which reaches nominal output voltage during a soft-start time of 250 µs (typical). This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

If the output voltage is not reached within the soft-start time, such as in the case of a heavy load, the converter enters regular operation. The TLV62565/6 are able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

9.3.4 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition.

The TLV62565/6 adopt valley current control by sensing the current of the low-side FET. If the inductor current reaches the low-side FET valley current limit $I_{LIM,LS}$ (typical 1.7 A), the low-side FET is turned off and the high-side FET is turned on to ramp up the inductor current. The current ramping up time is controlled by the on time setting of the device, as shown in Figure 7. For example, the peak current is 1.97 A when the switch current limit is triggered with 3.6 V_{IN} to 1.8 V_{OUT} and 2.2-µH application.

To prevent the inductor current from running away, the devices implement an additional high-side peak current limit $I_{LIM,HS}$ (typical 2 A), which is shown in Figure 7. It forces to turn off the high side FET immediately once the peak inductor current reaches the threshold. Due to the internal propagation delay, the real current limit value might be higher than the static current limit in the electrical characteristics table.

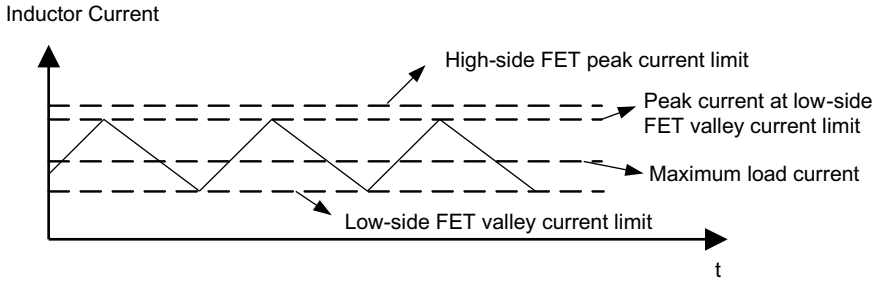


Figure 7. Switch Current Limit

9.3.5 Power Good

The TLV62566 integrates a Power Good output going low when the output voltage is below its nominal value. The Power Good output stays high impedance once the output is above 95% of the regulated voltage and is low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is an open drain output and is specified to sink typically up to 0.5 mA. The Power Good output requires a pull-up resistor connected to any voltage lower than 5.5 V. When the device is off due to UVLO or thermal shutdown, the PG pin is pulled to logic low.

9.4 Device Functional Modes

9.4.1 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

Device Functional Modes (continued)

9.4.2 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds typically T_{JSD}. Once the device temperature falls below the threshold with hysteresis, the device returns to normal operation automatically. Power Good is pulled low when thermal protection is triggered.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLV6256x devices are synchronous step-down converters optimized for small solution size and high efficiency. The devices integrate switches capable of delivering an output current up to 1.5 A.

10.2 Typical Application

TLV62565 2.7-V to 5.5-V input, 1.2-V output converter.

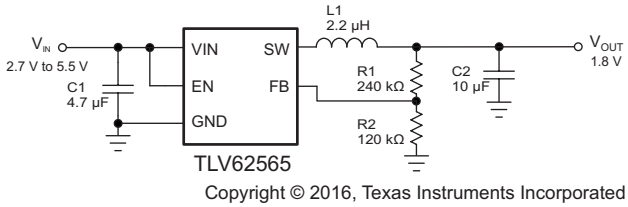


Figure 8. TLV62565 1.2-V Output Application

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 µF, Ceramic Capacitor, 6.3 V, X5R, size 0603, GRM188R60J475ME84	Murata
C2	10 µF, Ceramic Capacitor, 6.3 V, X5R, size 0603, GRM188R60J106ME84	Murata
L1	2.2 µH, Power Inductor, 2.5 A, size 4mmx4mm, LQH44PN2R2MP0	Murata
R1, R2	Chip resistor,1%,size 0603	Std.

10.2.1 Design Requirements

10.2.1.1 Output Filter Design

The inductor and output capacitor together provide a low-pass frequency filter. To simplify this process, Table 2 outlines possible inductor and capacitor value combinations.

Table 2. Matrix of Output Capacitor and Inductor Combinations

L [µH](1)	C_{OUT} [µF](2) (3)				
	4.7	10	22	47	100
1					
2.2		+ (4)	+ (4)	+	
4.7					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) For low output voltage applications (≤ 1.2 V), more output capacitance is recommended (usually ≥ 22 µF) for smaller ripple.
(4) Typical application configuration. '+' indicates recommended filter combinations.

10.2.1.2 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 1 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value (1)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. The recommended inductors are listed in Table 3.

Table 3. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [mA]	DIMENSIONS L x W x H [mm^3]	DC RESISTANCE [mΩ typ]	TYPE	MANUFACTURER
2.2	2500	4 x 3.7 x 1.65	49	LQH44PN2R2MP0	Murata
2.2	3000	4 x 4 x 1.8	50	NRS4018T2R2MDGJ	Taiyo Yuden

10.2.1.3 Input and Output Capacitor Selection

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. The closer the input capacitor is placed to the V_{IN} and GND pins, the lower the switch ring. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The architecture of the TLV62565/6 allow use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. The TLV62565/6 are designed to operate with an output capacitance of 10 µF to 47 µF, as outlined in Table 2.

10.2.2 Detailed Design Procedure

10.2.2.1 Setting the Output Voltage

An external resistor divider is used to set output voltage. By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{FB}. Equation 2, Equation 3, and Equation 4 can be used to calculate R1 and R2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a minimum of 5 µA for the feedback current I_{FB}. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.6V}{5\mu A} = 120k\Omega \quad (3)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \quad (4)$$

Due to the maximum duty cycle limit, the output voltage is out of regulation if the input voltage is too low. For proper regulation, V_{OUT} should be set below V_{IN_MIN} as shown in Equation 5.

$$V_{OUT} \leq V_{IN\_MIN} \times D_{MAX} \quad (5)$$

where

- V_{IN_MIN}, the minimum value of the input voltage;

10.2.2.2 Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination. Applications with the recommended L-C combinations in Table 2 are designed for good loop stability as well as fast load transient response.

As a next step in the evaluation of the regulation loop, the load transient response is illustrated. The TLV62565/6 use a constant on time with valley current mode control, so the on time of the high-side MOSFET is relatively consistent from cycle to cycle when a load transient occurs. Whereas the off time adjusts dynamically in accordance with the instantaneous load change and brings V_{OUT} back to the regulated value.

During recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing which helps judge the stability of the converter. Without any ringing, the loop usually has more than 45° of phase margin.

10.2.3 Application Performance Curves

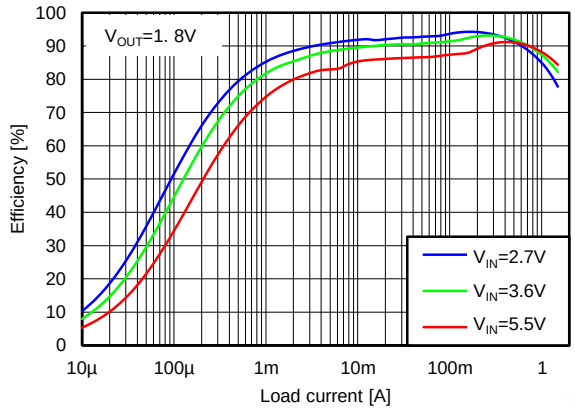


Figure 9. Efficiency vs Load Current

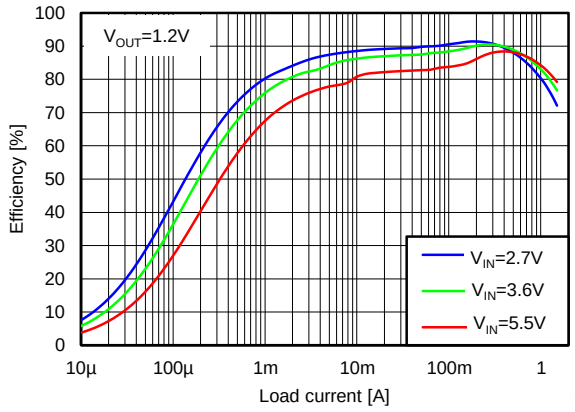


Figure 10. Efficiency vs Load Current

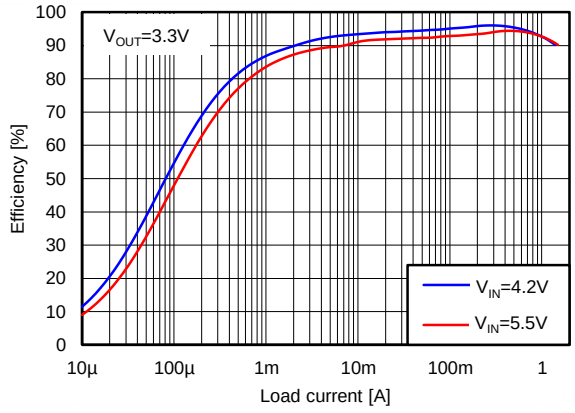


Figure 11. Efficiency vs Load Current

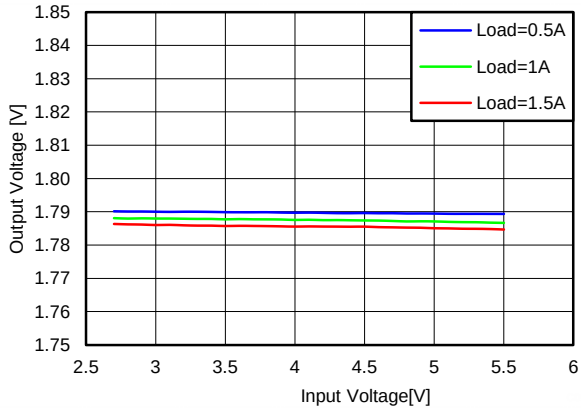


Figure 12. Output Voltage vs Input Voltage

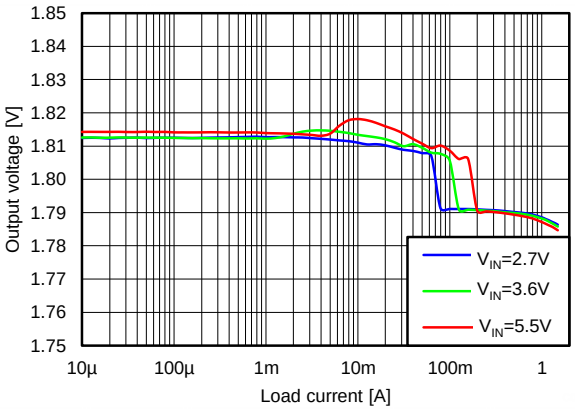


Figure 13. Output Voltage vs Load Current

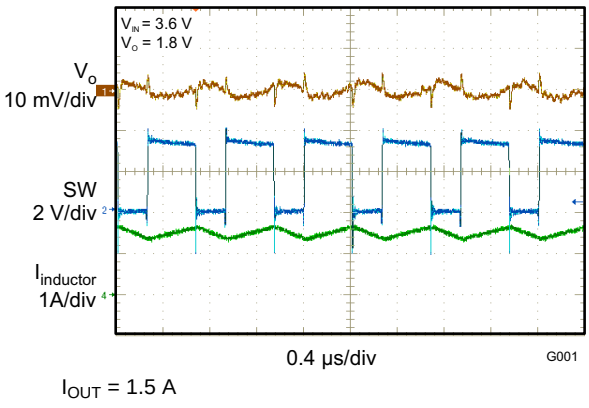


Figure 14. Typical Application (PWM Mode)

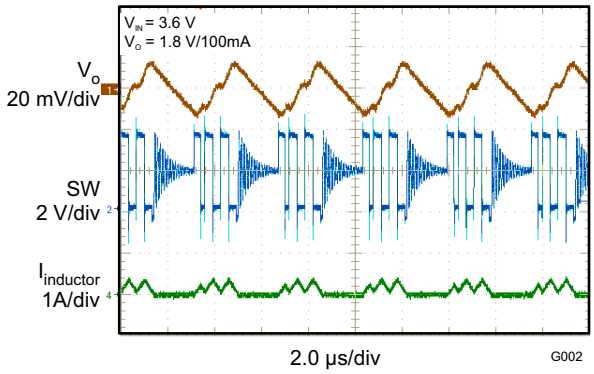


Figure 15. Typical Application (PFM Mode)

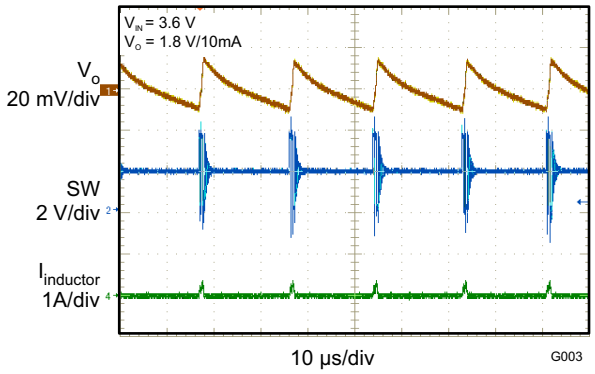


Figure 16. Typical Application (PFM Mode)

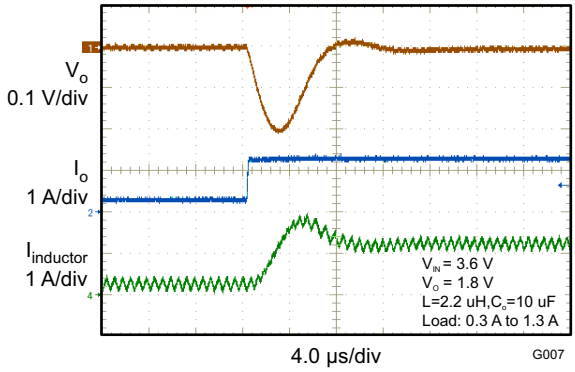


Figure 17. Load Transient

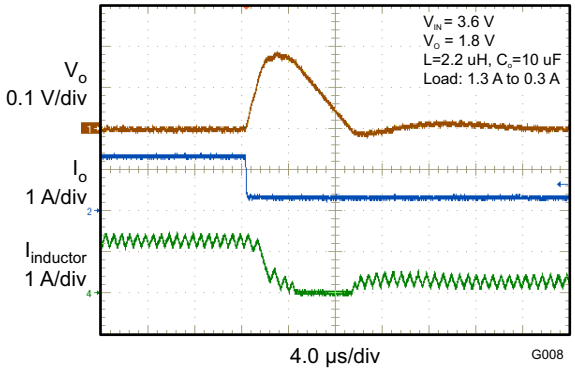


Figure 18. Load Transient

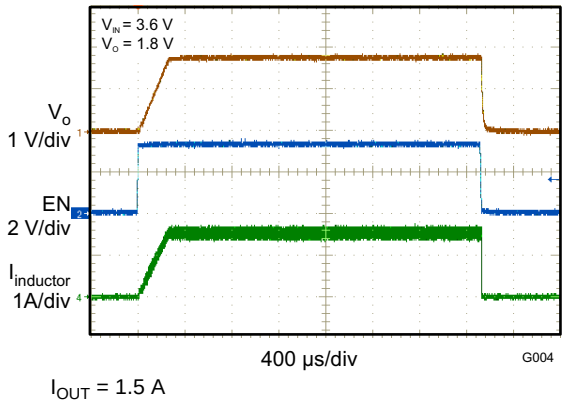


Figure 19. Start Up

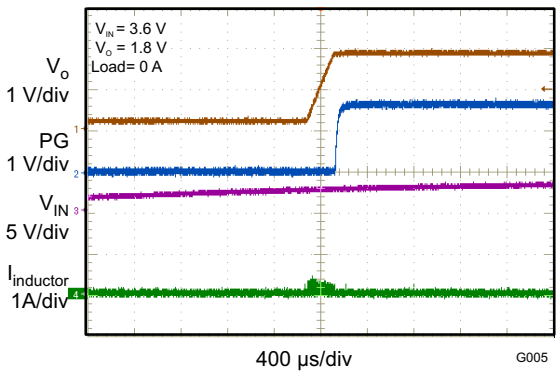
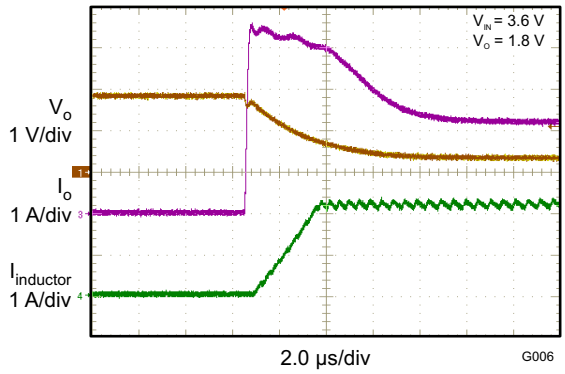


Figure 20. Start Up (Power Good)



No load to short circuit

Figure 21. Short Circuit Protection

11 Power Supply Recommendations

The power supply to the TLV62565 and TLV62566 needs to have a current rating according to the supply voltage, output voltage and output current of the TLV62565 and TLV62566.

12 Layout

12.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62565 devices.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance.
- A common power GND should be used.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

12.2 Layout Example

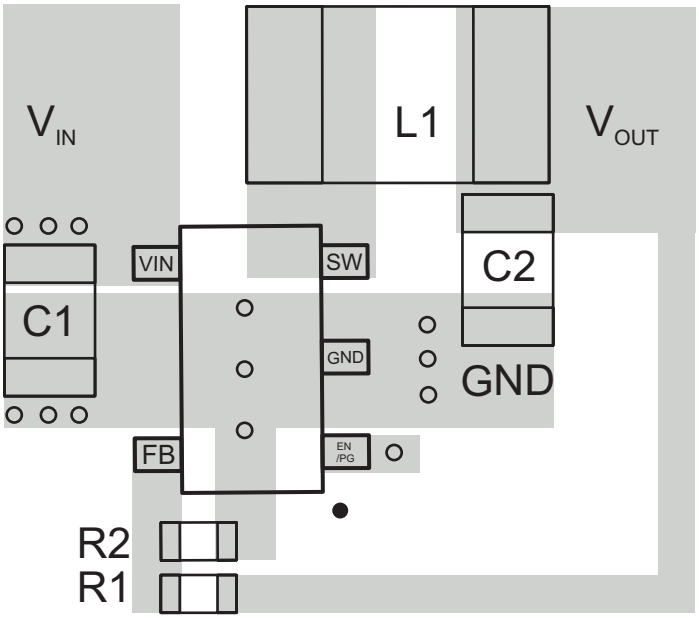


Figure 22. TLV62565/6 Layout

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

Semiconductor and IC Package Thermal Metrics Application Report (SPRA953)

Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report (SZZA017)

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV62565	Click here	Click here	Click here	Click here	Click here
TLV62566	Click here	Click here	Click here	Click here	Click here

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62565DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIK	Samples
TLV62565DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIK	Samples
TLV62566DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	SIL	Samples
TLV62566DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	SIL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

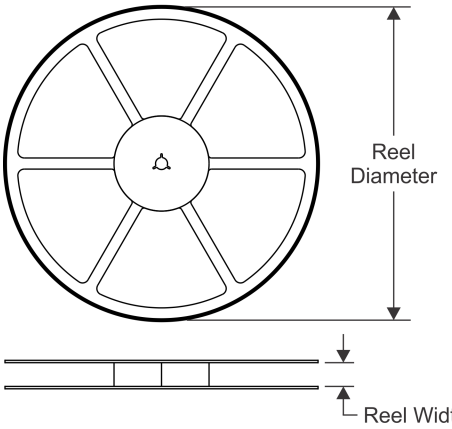
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

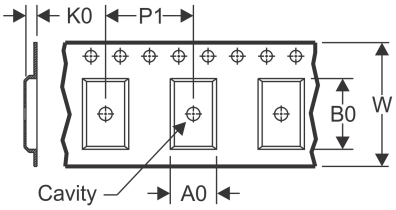
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

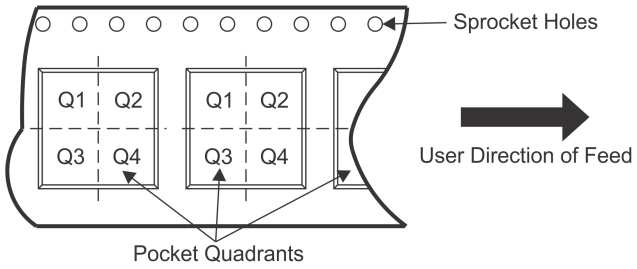


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

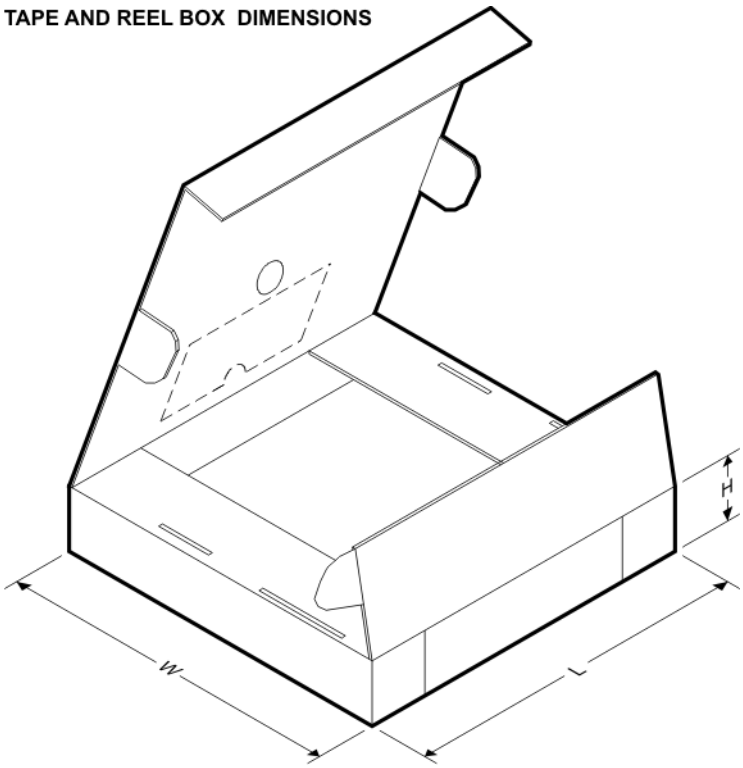
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62565DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62565DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV62565DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62566DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62566DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV62566DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV62566DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

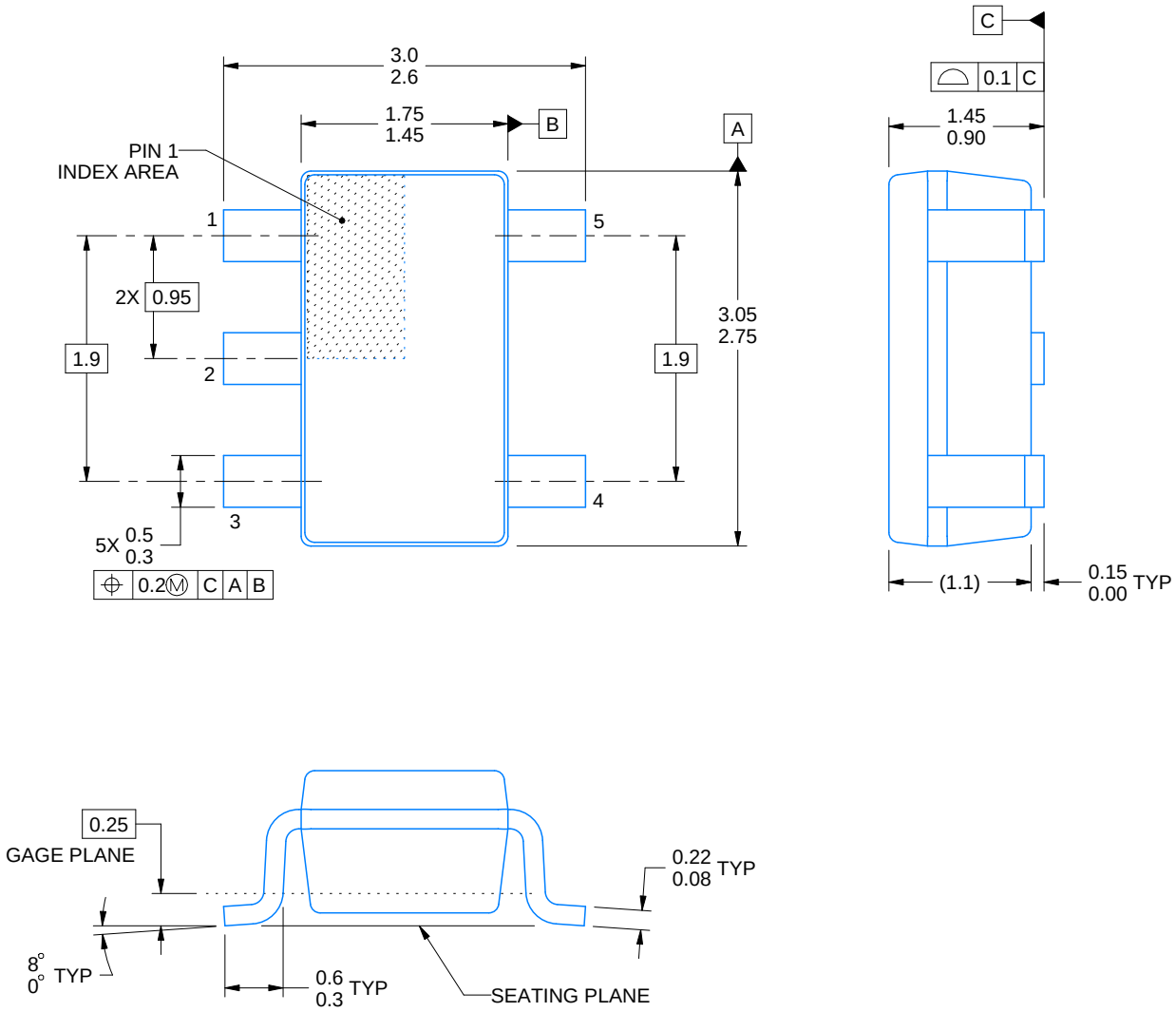
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62565DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62565DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV62565DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62566DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62566DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV62566DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV62566DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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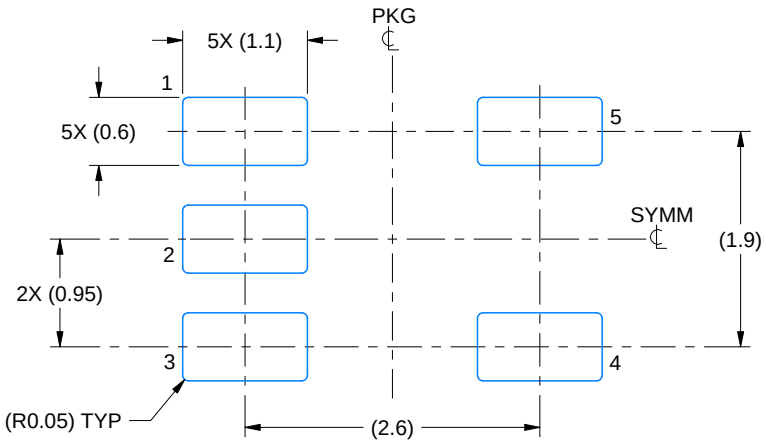
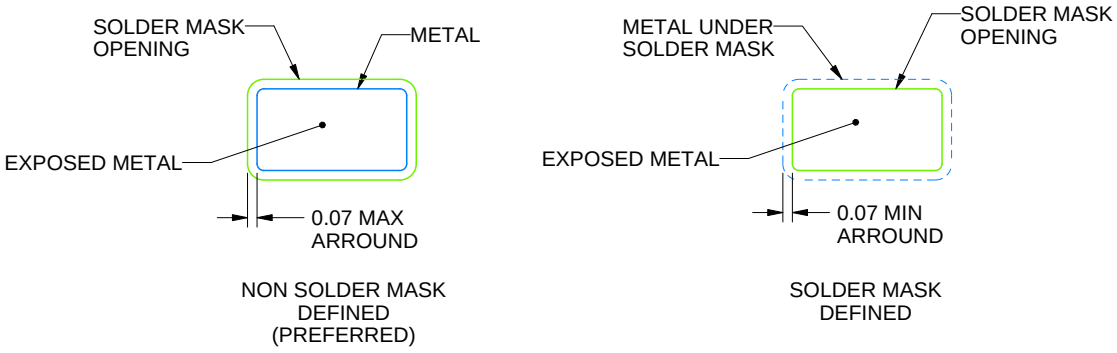
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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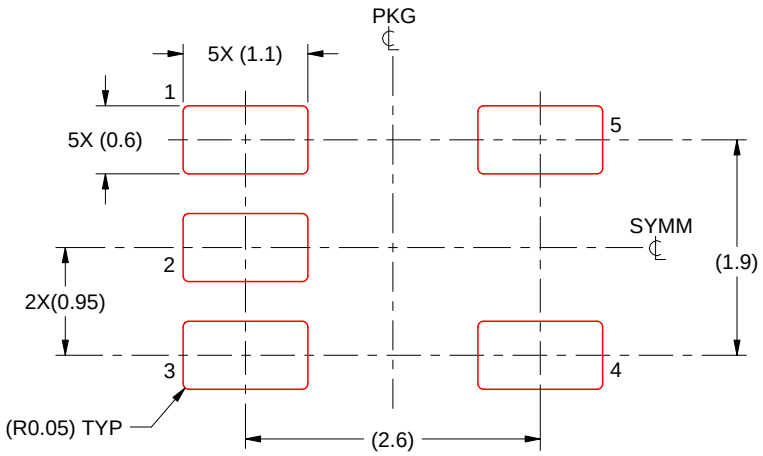
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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