User's Guide

AM273x EVM User's Guide

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Abstract

The AM273x EVM is an Evaluation module designed to develop software and evaluate the AM273x Radar Controller and Processor SoC from Texas Instruments. The AM273x is a multicore SoC designed to provide an integrated control and processing platform for TI AWR mmWave radar front-end devices in both single-device and cascaded modes of operation. The signal interface between the AM273x EVM and the AWR2243BOOST mmWave Radar EVM uses the 60-pin Samtec high density connector.

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1 Preface: Read This First

1.1 If You Need Assistance

If you have any feedback or questions, support for Sitara MCUs and the AM273x EVM development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website.

1.2 Important Usage Notes

Note

A 12-V, > 2.5-A supply brick with a 2.1-mm barrel jack (center positive) is **not** included in the kit and must be ordered seperately. For more information on power requirements go to Section 3.1.

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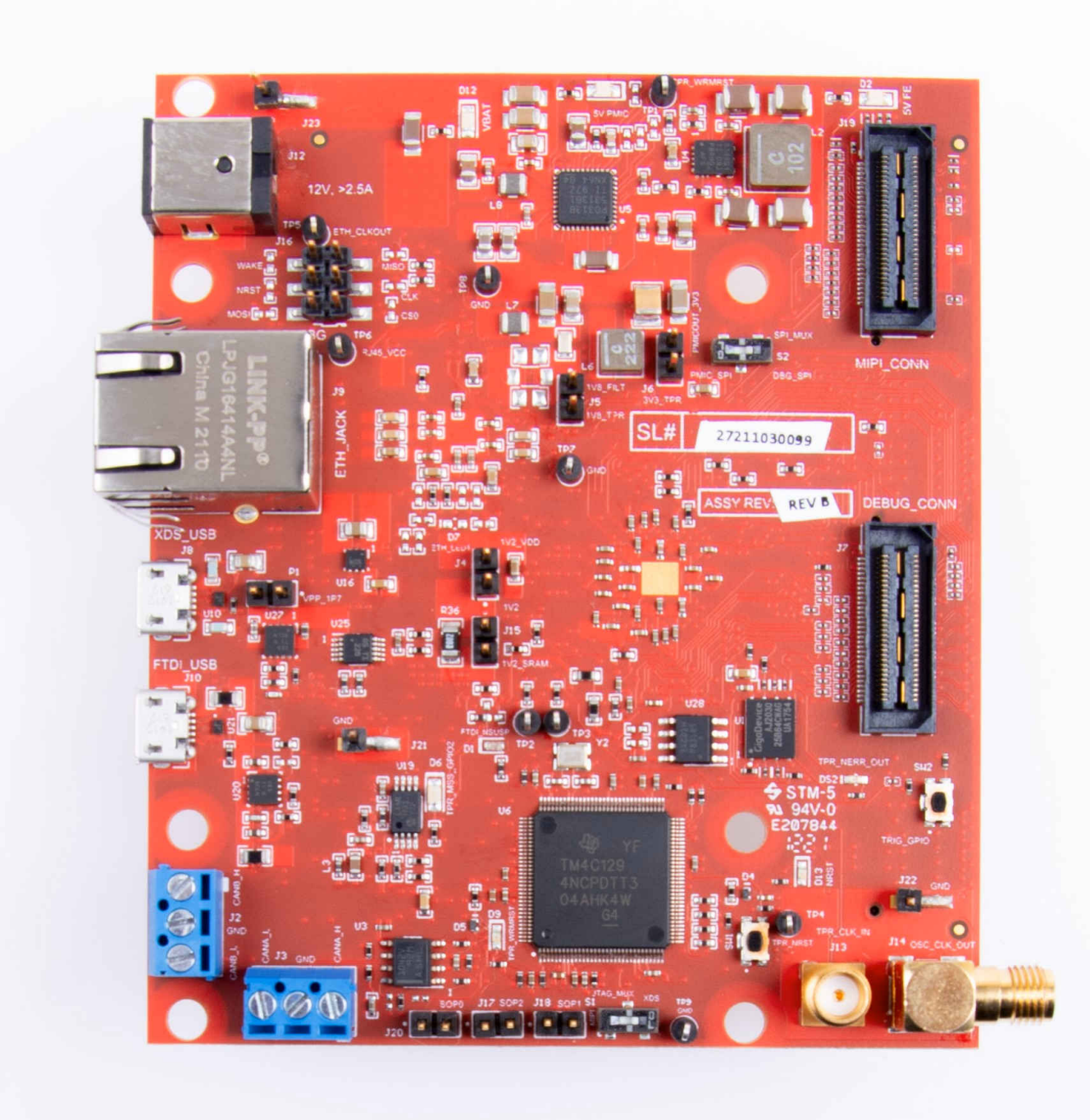
2 Kit Overview



2.1 Kit Contents

The Sitara AM273x EVM Development Kit contains the following items:

- TMDS273GPEVM
- Micro USB cable
- Ethernet Cable
- Samtec coax micro ribbon cable (HQCD-030-02.00-SEU-TBR-1)
- Spacers, screws, and washers

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2.2 Key Features

- Dual 60-pin high density (HD) connector interface with TI's front end radar device EVMs, such as the AWR2243BOOST
- XDS110-based JTAG emulation with Serial port for onboard QSPI flash programming
- UART to USB Debug port for terminal access using FT4232H
- External JTAG/ Emulator Interface with TRACE support over 60-pin MIPI connector
- Debug, SPI, I2C, and LVDS connected to 60-pin Debug connector
- Ethernet interface to stream the captured data over the network to the host PC
- Dual On-board CAN-FD transceiver
- One button and LED for basic user interface
- 12-V power jack to power the board

2.3 Component Identification

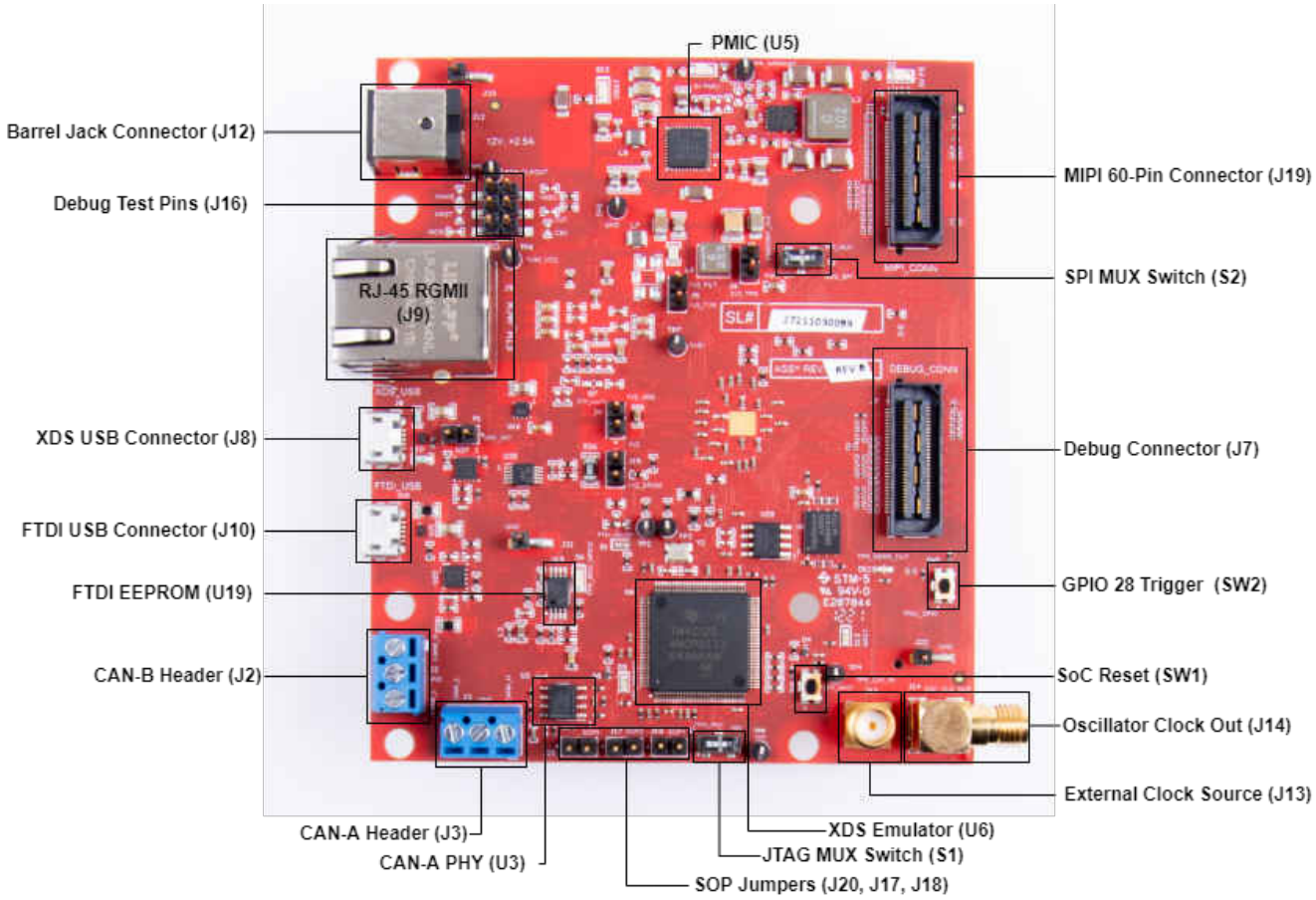

Figure 2-1. AM273x EVM Top Component Identification

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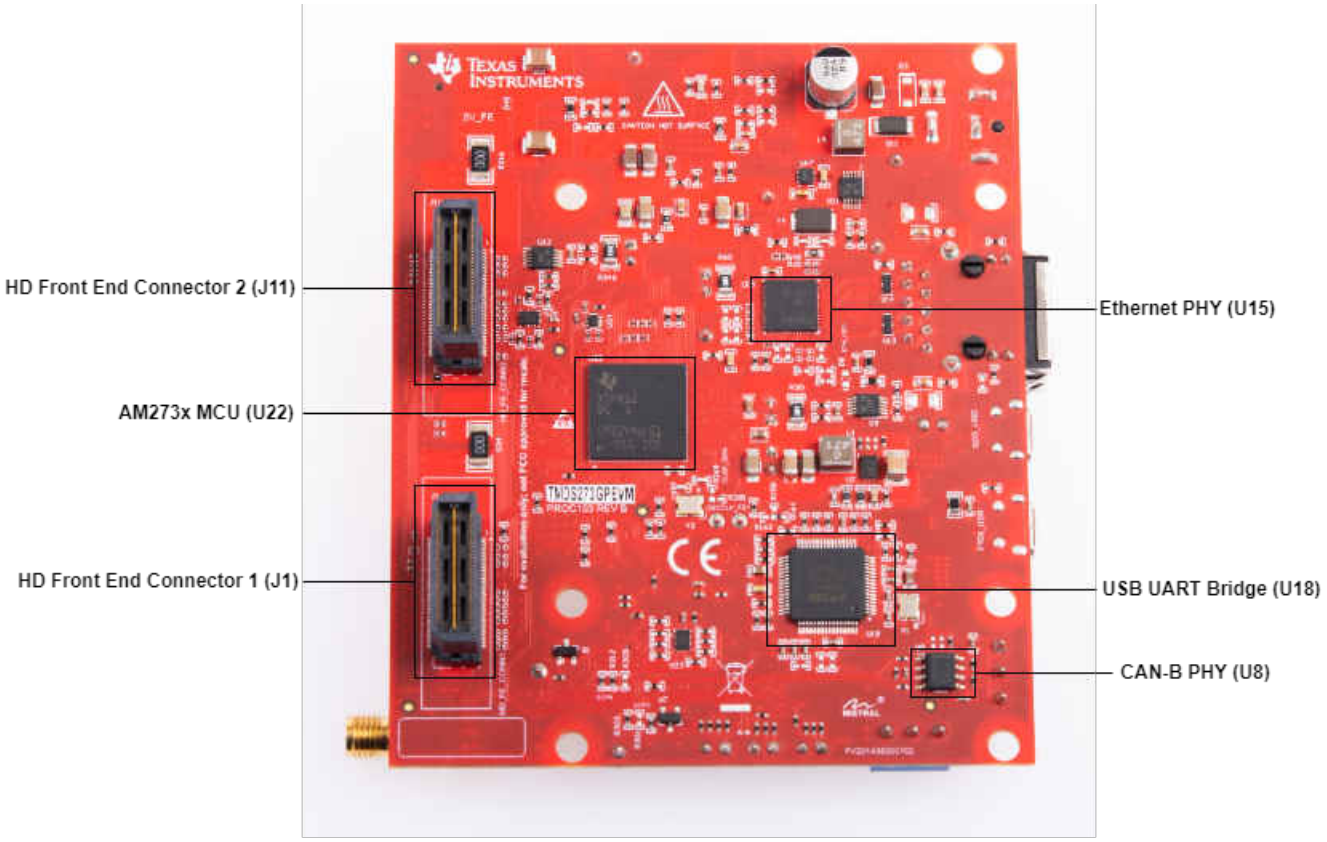

Figure 2-2. AM273x EVM Bottom Component Identification

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2.4 Daughter Cards

The AM273x EVM development kit provides an easy and inexpensive way to develop applications with the AM273x Series microcontroller. Daughter cards are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of daughter cards greatly expands the peripherals and potential applications that you can easily explore with the AM273x EVM.

2.4.1 Connecting the TMDS273GPEVM to the AWR2243BOOST EVM

The TMDS273GPEVM can be connected to the AWR2243BOOST EVM for developing a complete radar system with front end and processor.

2.4.2 Connecting the TMDS273GPEVM to the DCA1000

The TMDS273GPEVM can be connected to the DCA1000 FGPA platform to allow for LVDS data streaming.

TMDS273GPEVM and DCA1000 EVM can be connected with the help of a Samtec ribbon cable connected between Debug Connector J7 (see Table 5-4) on the TMDS273GPEVM and DCA1000EVM 60-pin connector, as shown in Figure 2-3.

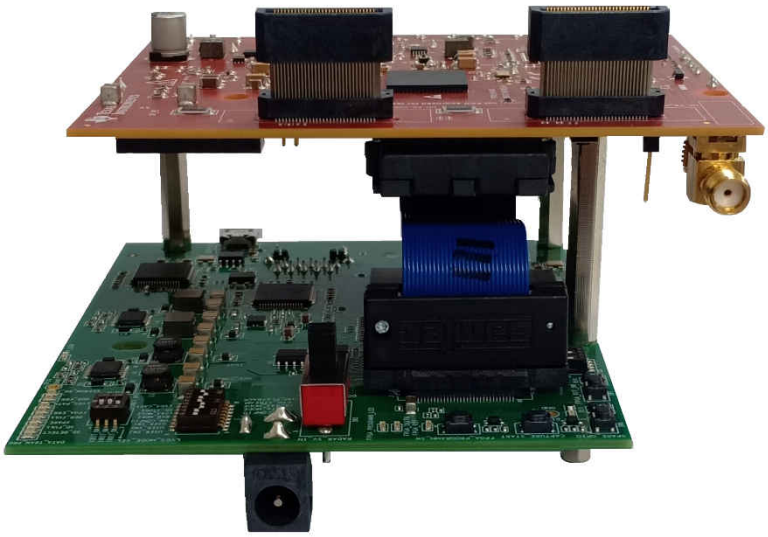

Figure 2-3. Interfacing DCA1000 EVM to Debug Connector of the AM273x EVM

2.5 Compliance

All components selected meet RoHS and REACH compliance.

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3 Board Setup

3.1 Power Requirements

The AM273x EVM is powered through a barrel jack connection. The power source should be capable of providng 2.5A at 12 V. The length of the power cable should be < 3 m.

External Power Supply or Power Accessory Requirements:

Nom Ouput Voltage: 5VDC

Max Output Current: 2500mA

Efficiencty Level V

Note

TI recommendsusing an external power supply or power accessory which complies with applicable regional safety standards such as (by example) UL, CSA, CDE, CCC, PSE, etc.

The following power supply has been tested to work with the TMDS273GPEVM:

https://www.digikey.in/product-detail/en/cui-inc/SDI65-12-U-P5/102-3417-ND/5277850

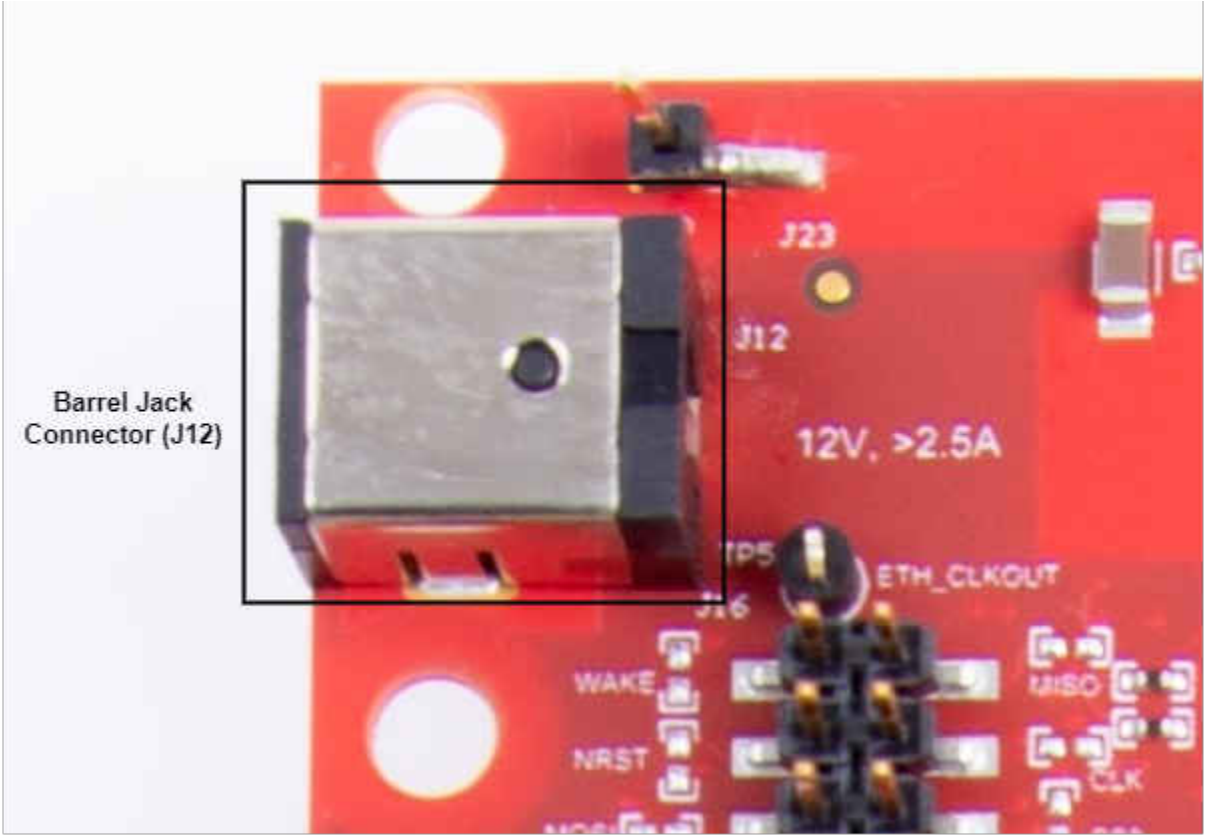

Figure 3-1. Barrel Jack Connector (J12)

The AM273x EVM includes a power solution based on a power management integrated circuit (PMIC) to bring up the power rails according to the power on timing specifications and a LM61460 step-down converter to power the radar front end connector supplies

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3.1.1 Power Status LED's

Multiple power-indication LED's are provided on-board to indicate to users the output status of major supplies.

Table 3-1. Power Status LED's

Name	Default Status	Operation	Function
D12	ON	VBAT_INT	Power indicator for 12-V barrel jack supply input
D16	ON	PMICOUT_5V0	Power indication for 5-V PMIC output
D13	ON	nRESET	Indication of nRESET pin. If LED is glowing, the device is out of reset
D2	ON	5V_FE	Power indicator for 5-V FE connectors

For further information on the TMDS273GPEVM LED's please see Section 3.4.

3.2 Push Buttons

The EVM supports two buttons that provide a reset and user input to the controller.

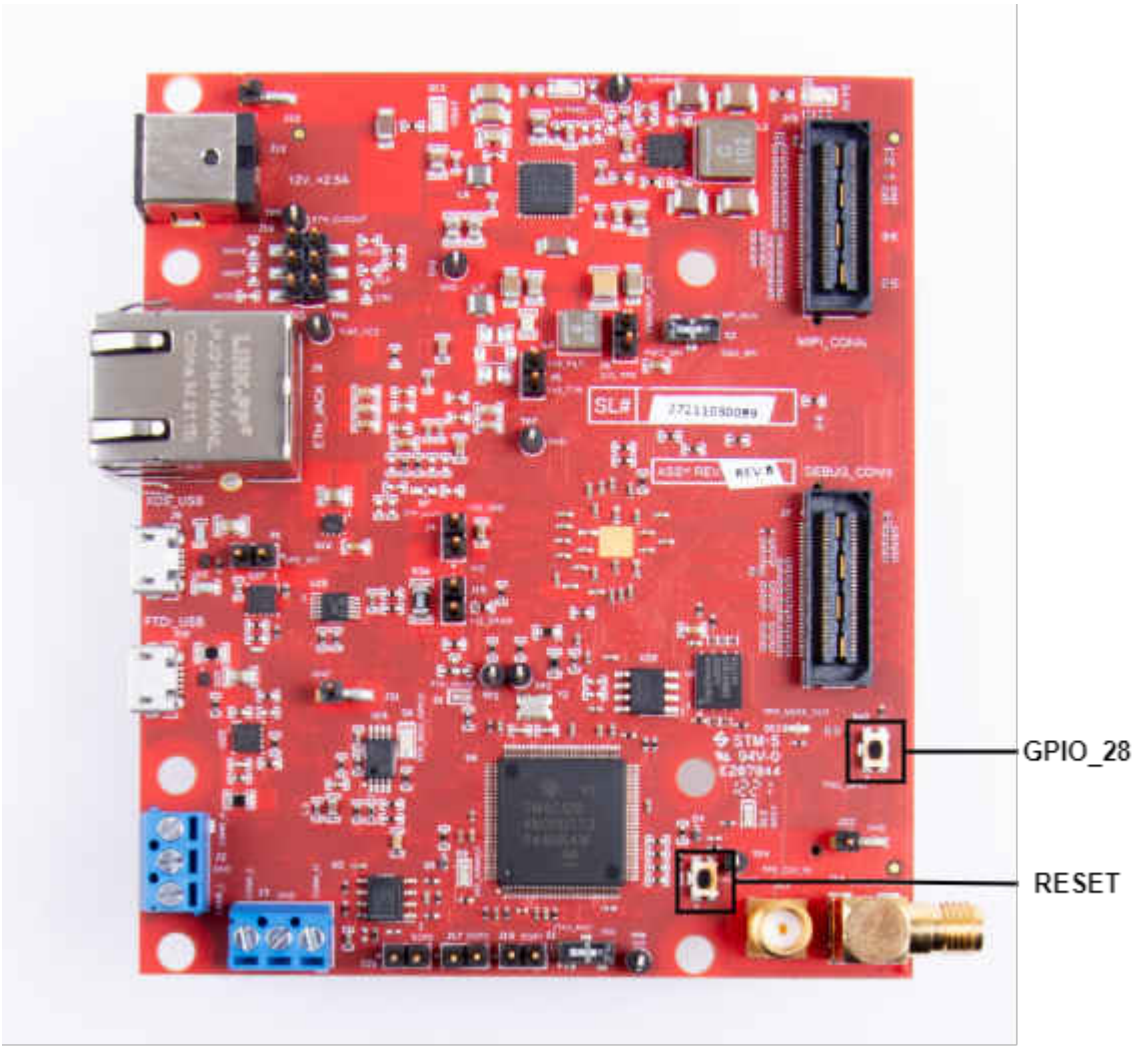

Figure 3-2. AM273x EVM Push Buttons

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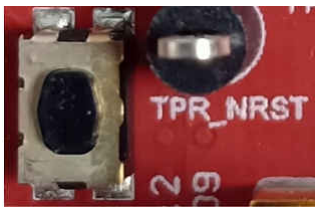
Table 3-2. EVM Push Buttons

Push Button	Signal	Function
SW1	TPR_NRST	AM273x, PMIC, and FTDI device reset
SW2	MSS_GPIO_28	User interrupt input

Table 3-3. Push Buttons Switches Information

Reference	Usage	Comments	Image
SW1	RESET	This Switch is used to RESET the AM2732, PMIC, and FTDI device.	
SW2	GPIO_28	When pushed, the GPIO_28 (net MSS_GPIO_28) is pulled high to PMICOUT_3V3. When idle (not pushed), GPIO_28 (net MSS_GPIO_28) is pulled to ground via a 10 kiloohm resistor.	

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3.3 Switches

The AM273x EVM contains two switches to mux various interfaces to different connectors on the EVM.

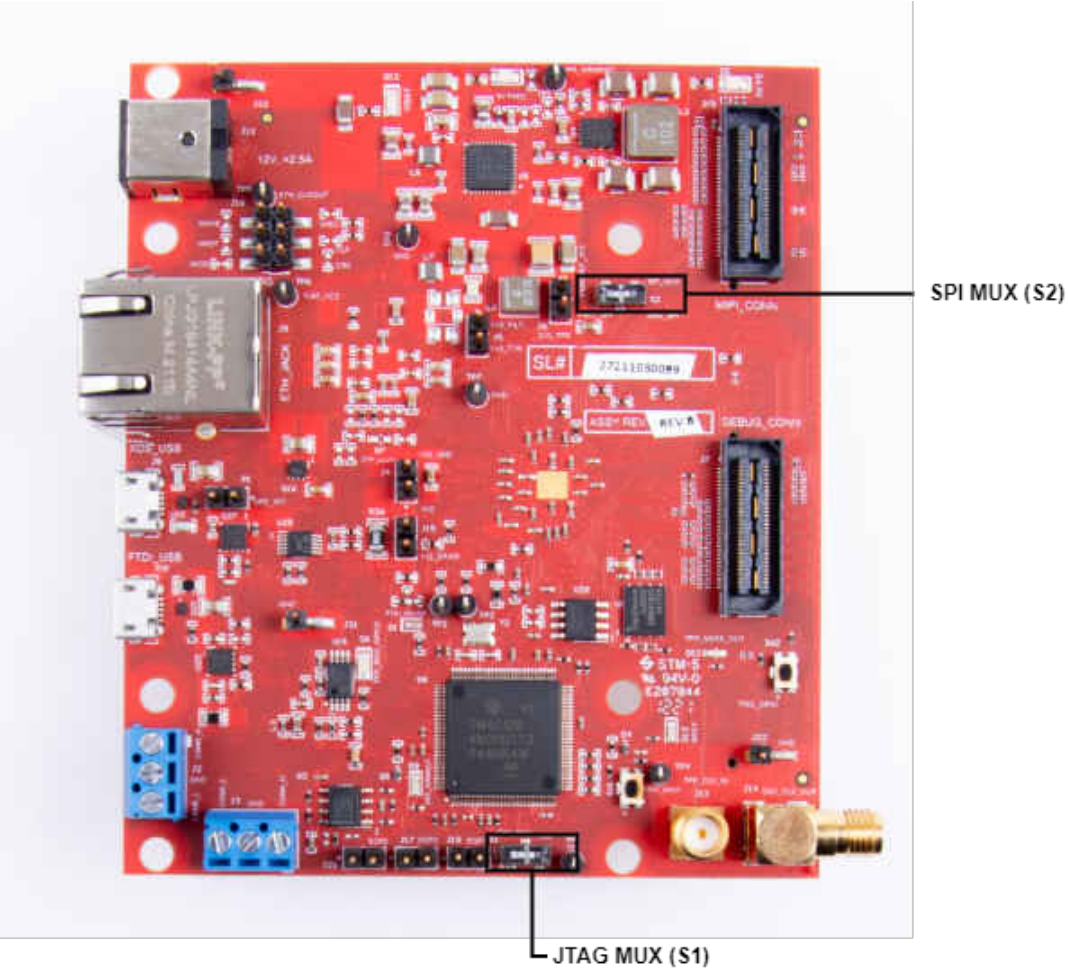

Figure 3-3. AM273x EVM Switches

Table 3-4. Switches Information

Reference	Usage	Comments	Image
S1	JTAG	When set to 'MIPI' position, the JTAG interface is routed to the MIPI 60-pin connector (J19). When set to 'XDS' position, the JTAG interface is routed to the XDS110 USB interface (J8)	
S2	SPI	When set to 'PMIC_SPI' position, the MSS_SPIB interface is routed to the PMIC and to the J16 header. 1 When set to 'DBG_SPI', the MSS_SPIB interface is routed to the 60-pin debug header (J7)	

1. DNP resistors R5, R61, R167, and R176 must be populated to bring the MSS_SPIB interface out to the J16 header.

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3.4 LEDs

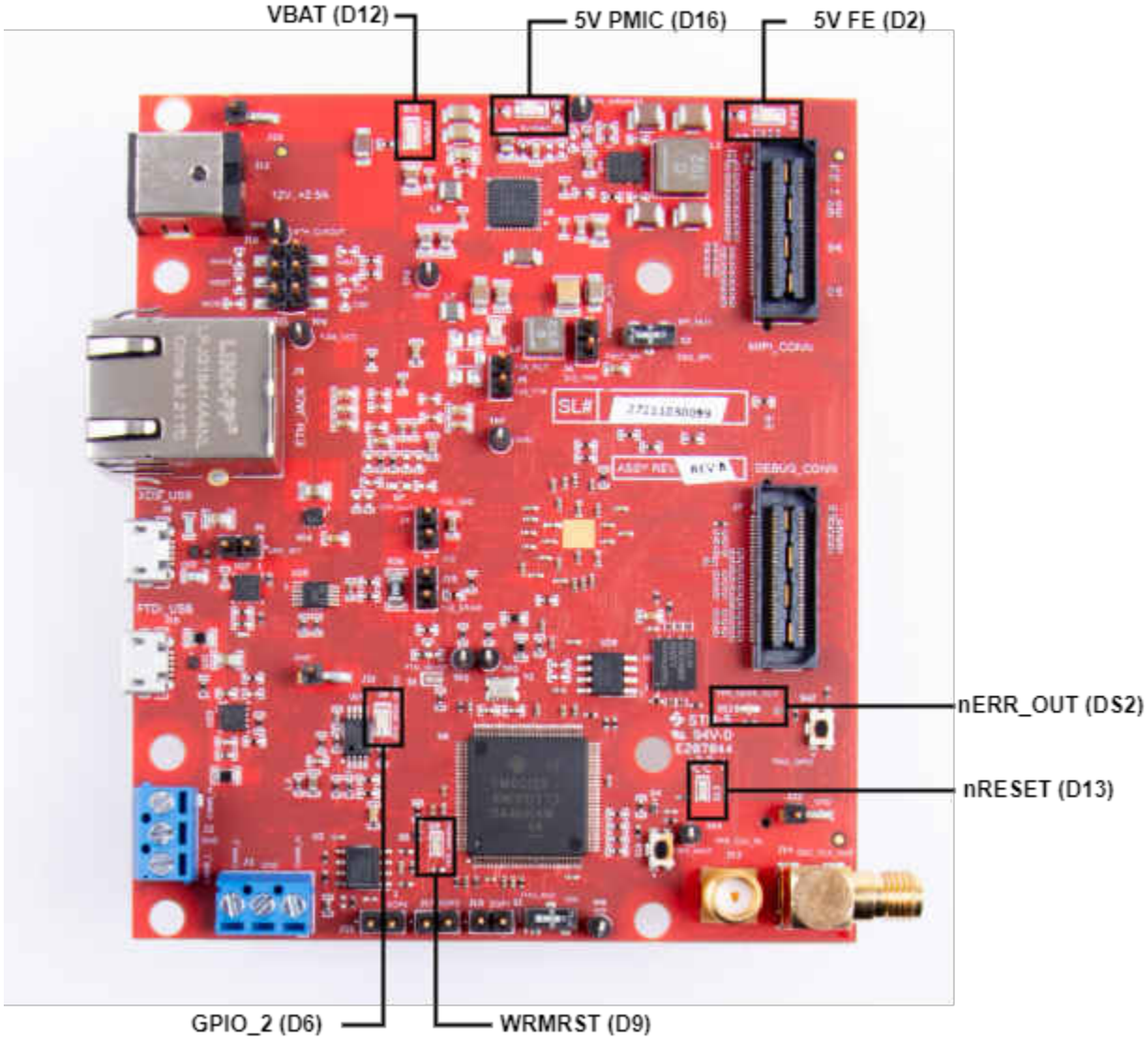

Figure 3-4. AM273x EVM LED's

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Table 3-5. LED Information

Ref	Colour	Usage	Comments	Image
D12	Green	12-V supply indication	This LED indicates the presence of 12-V supply input	
D16	Green	5-V PMIC Supply	This LED indicates the presence of 5-V supply output from PMIC	
D2	Green	5-V FE Supply	This LED indicates the presence of 5-V supply for FE connectors	
D13	Yellow	nRESET	This LED is used to indicate the state of nRESET pin. If this LED is glowing, the device is out of reset.	
DS2	Red	NERR_OUT	Glows if there is any HW error in the AM273x device	
D9	Yellow	WRMRST	Open drain fail safe warm reset signal	
D6	Green	GPIO_2	Glows when the GPIO_2 is logic-1	

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3.5 Boot Mode Selection

The TMDS273GPEVM can be set to operate in three different boot modes based on the state of the Sense On Power (SOP) [2:0] lines. These lines are sensed ONLY during boot up of the AM273x device. The state of the device is described in Table 3-6.

A closed jumper refers to a '1' and an open jumper refers to a '0' state of the SOP signal going to the AM273x device.

Table 3-6. Boot Mode Selection Table

Boot Modes Supported	SOP2 (J17)	SOP1 (J18)	SOP0 (J20)
Dev Management/UART Mode (SOP mode 5)	1	0	1
Functional/QSPI Mode (SOP mode 4)	0	0	1

Figure 3-5. SOP Jumpers

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4 Hardware Description

4.1 Functional Block Diagram

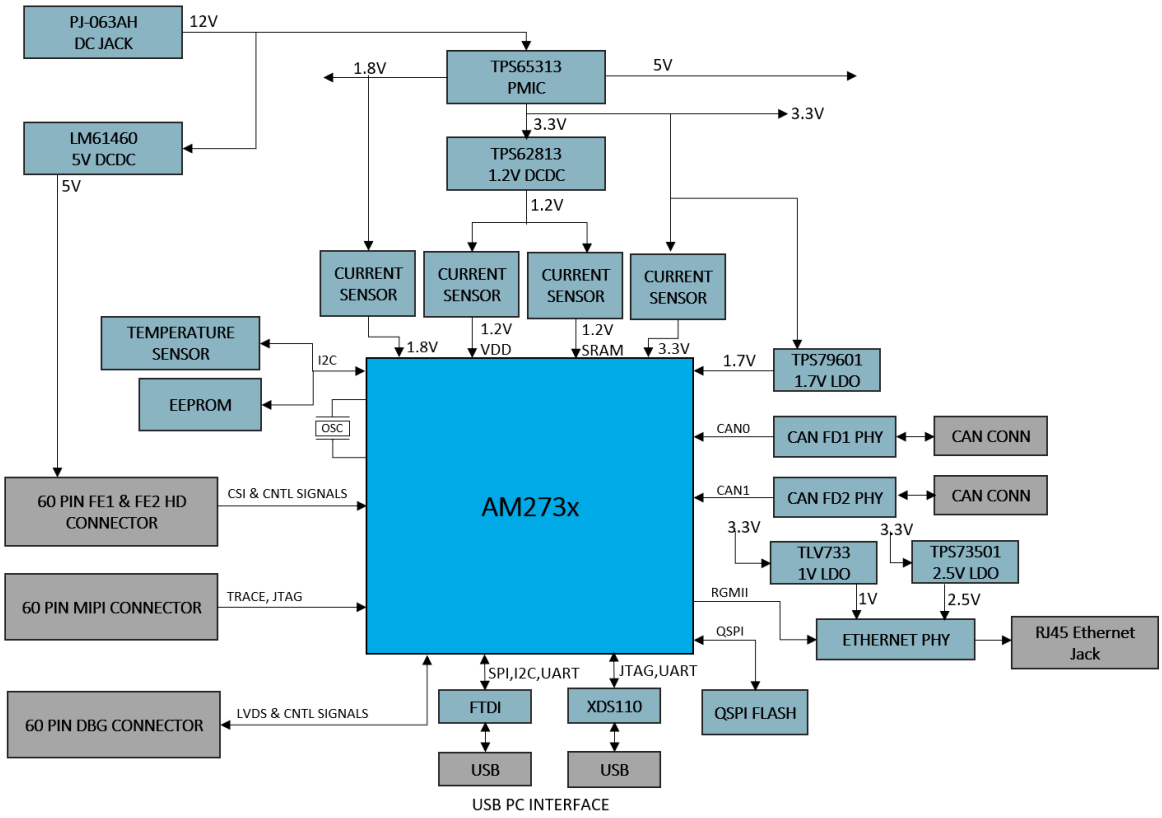

Figure 4-1. AM273x Functional Block Diagram

4.2 Memory Interface

4.2.1 QSPI Interface

The TMDS273GMEVM board has a 64 Mbit QSPI memory device (GD25B64CWAG from GigaDevice), which is connected to the MSS_QSPI interface of the AM273x SoC. This flash device is primarily meant to store the boot image, but can also serve as storage for other data if another boot mode is used.

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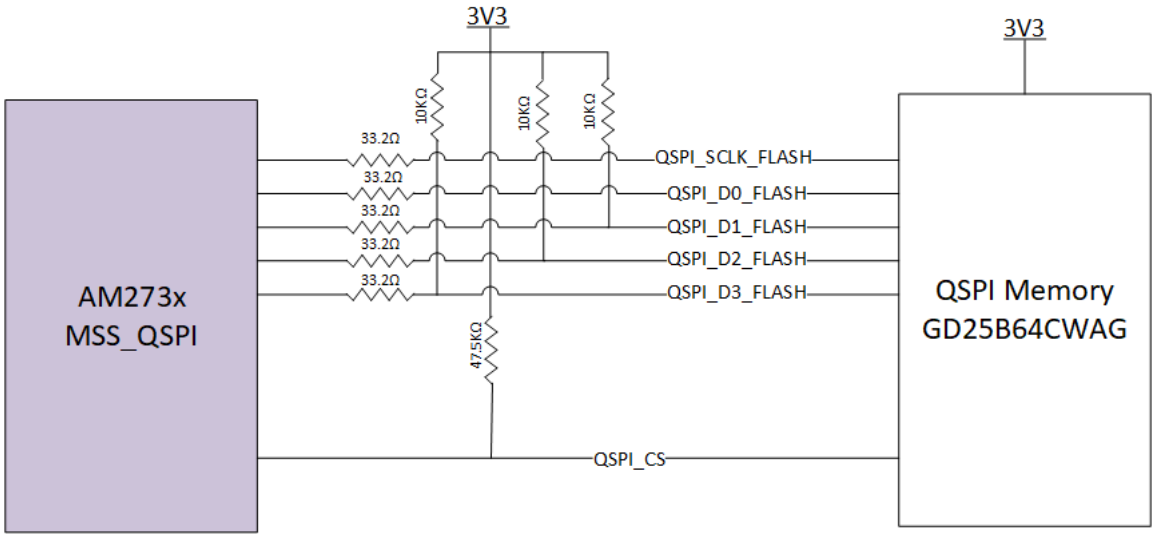

Figure 4-2. QSPI Interface

4.2.2 Board ID EEPROM

The AM273x EVM is a 2 Kbit I2C EEPROM for board ID information. The board ID memory is configured to respond to I2C address 0x50. This EEPROM (CAV24C02WE-GT3 from Onsemi) interfaces with the SoC via the MSS_I2CA port.

As seen in Figure 4-3, pins WP is allowed to float while A0, A1, and A2 are pulled to ground. These pins are pulled low internally. Pins A0, A1, and A2 configure the device address. The WP pin is the Write Protect input. When pulled high, this pin prevents write operations.

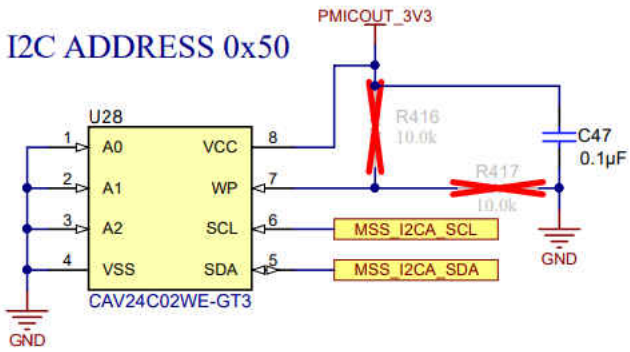

Figure 4-3. Board ID EEPROM

4.3 Ethernet Interface

The TMDS273GPEVM supports an RGMII Ethernet port to provide the connection to the network. This interface is intended to operate primarily as a 100-Mbps ECU interface. It can also be used as an Instrumentation Interface.

It supports following features:

- Full Duplex 10Mbps/100Mbps wire rate Interface to Ethernet PHY over RGMII, parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support

The Ethernet port is interfaced to the AM273x through the Ethernet PHY DP83867ERGZR, and is used to stream the captured data over the network to the host PC.

Figure 4-6 shows the Ethernet RJ45 Mag-Jack connector, and Table 4-1 provides the connector pin details.

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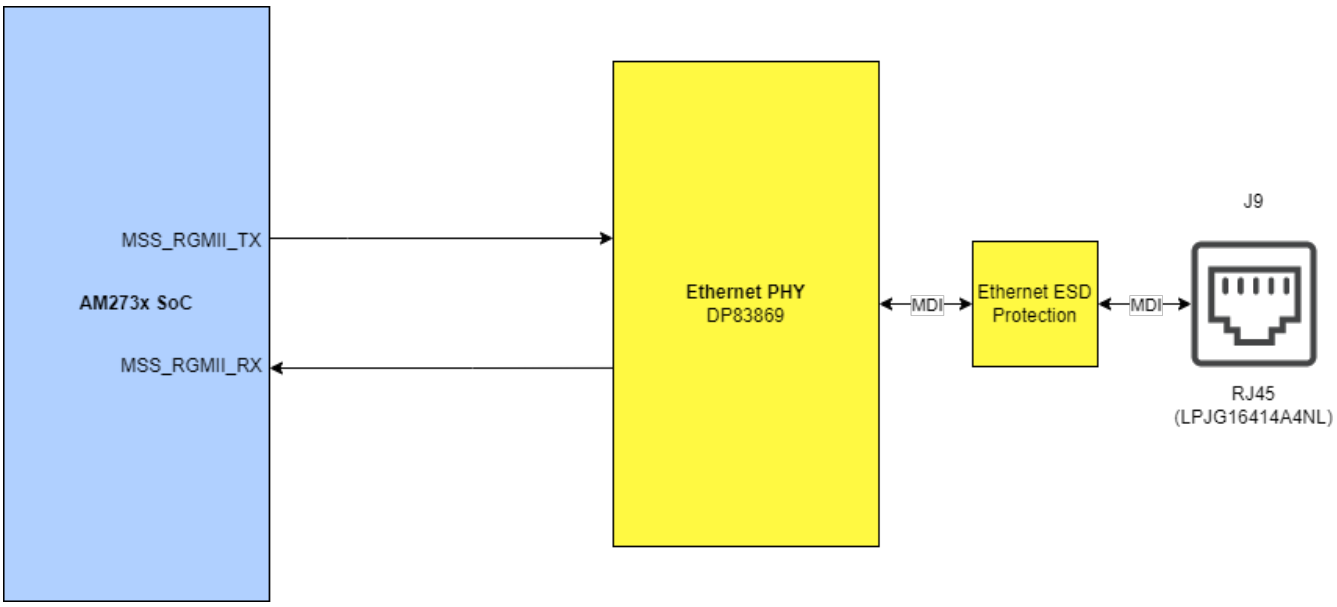

Figure 4-4. Ethernet Interface Block Diagram

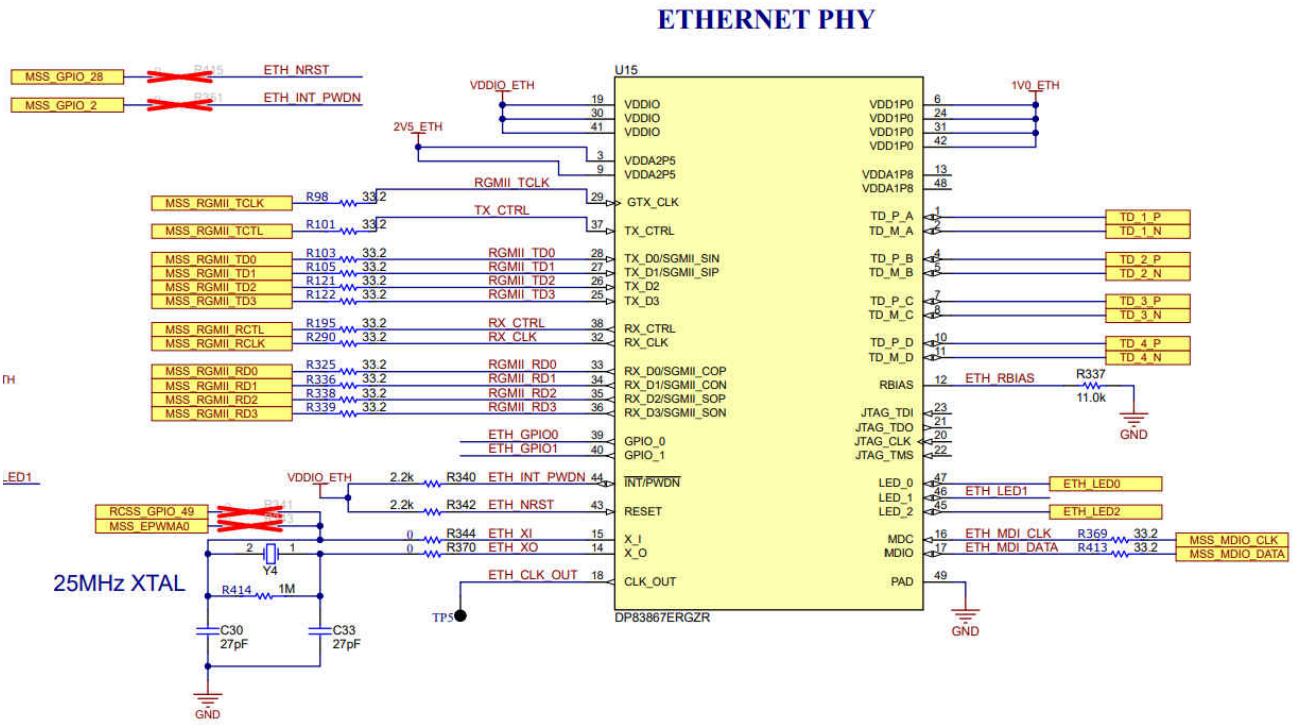

Figure 4-5. Etherney PHY Schematic

Table 4-1. J9 Connector Pin

Pin Number	Description	Pin Number	Description
1	GND	2	Test point
3	ETH_D4P	4	ETH_D4N
5	ETH_D3P	6	ETH_D3N
7	ETH_D2P	8	ETH_D2N
9	ETH_D1P	10	ETH_D1N

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Table 4-1. J9 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
11	LED_ACTn	12	GND
13	GND	14	LED_LINKn
15	ETH_GND	16	ETH_GND

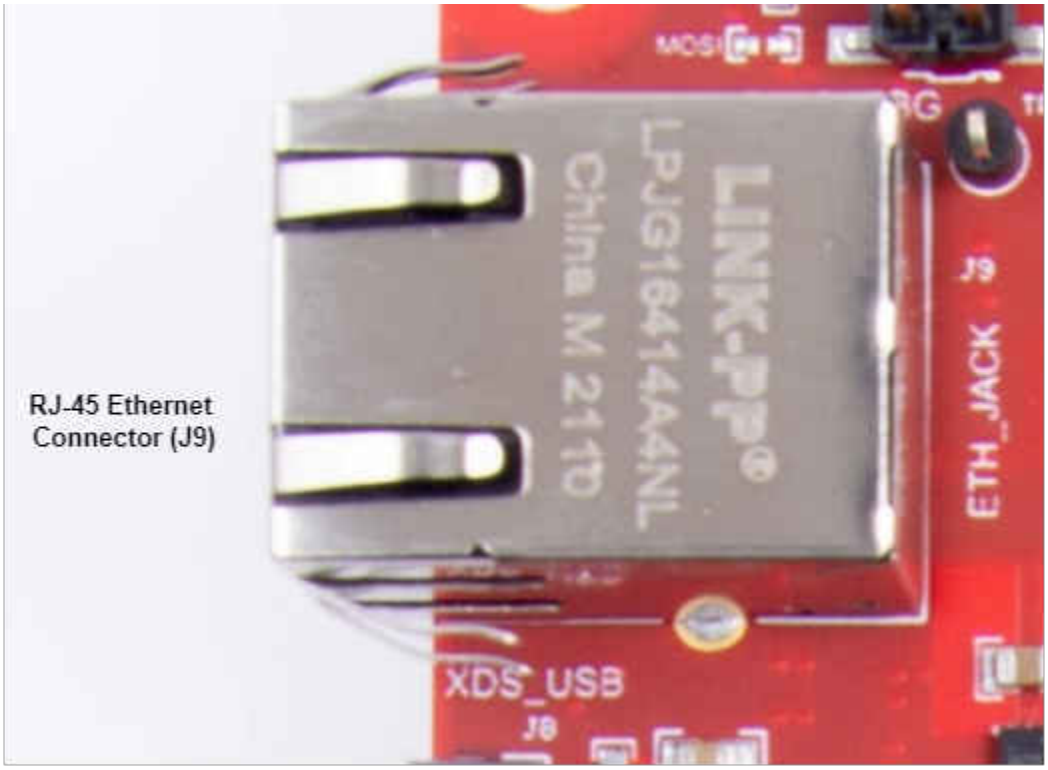

Figure 4-6. RJ45 Connector

4.4 Micro USB Interfaces

The TMDS273GPEVM has two standard micro USB connectors.

Micro USB Connector J10 provides access to the AM273x UART, SPI, I2C, and SOP interfaces through the FTDI chip.

Micro USB connector J8 provides access to the JTAG, MSS_UARTA, and MSS_UARTB interfaces of the AM273x via the XDS110 emulator.

4.4.1 FTDI USB Interface

Micro USB Connector J10 provides access to the AM273x UART, SPI, I2C, and SOP interfaces through the FTDI USB Interface IC (the FT4232HL). The FTDI USB Interface IC is configured by the FTDI EEPROM as described in Section 4.4.1.1.

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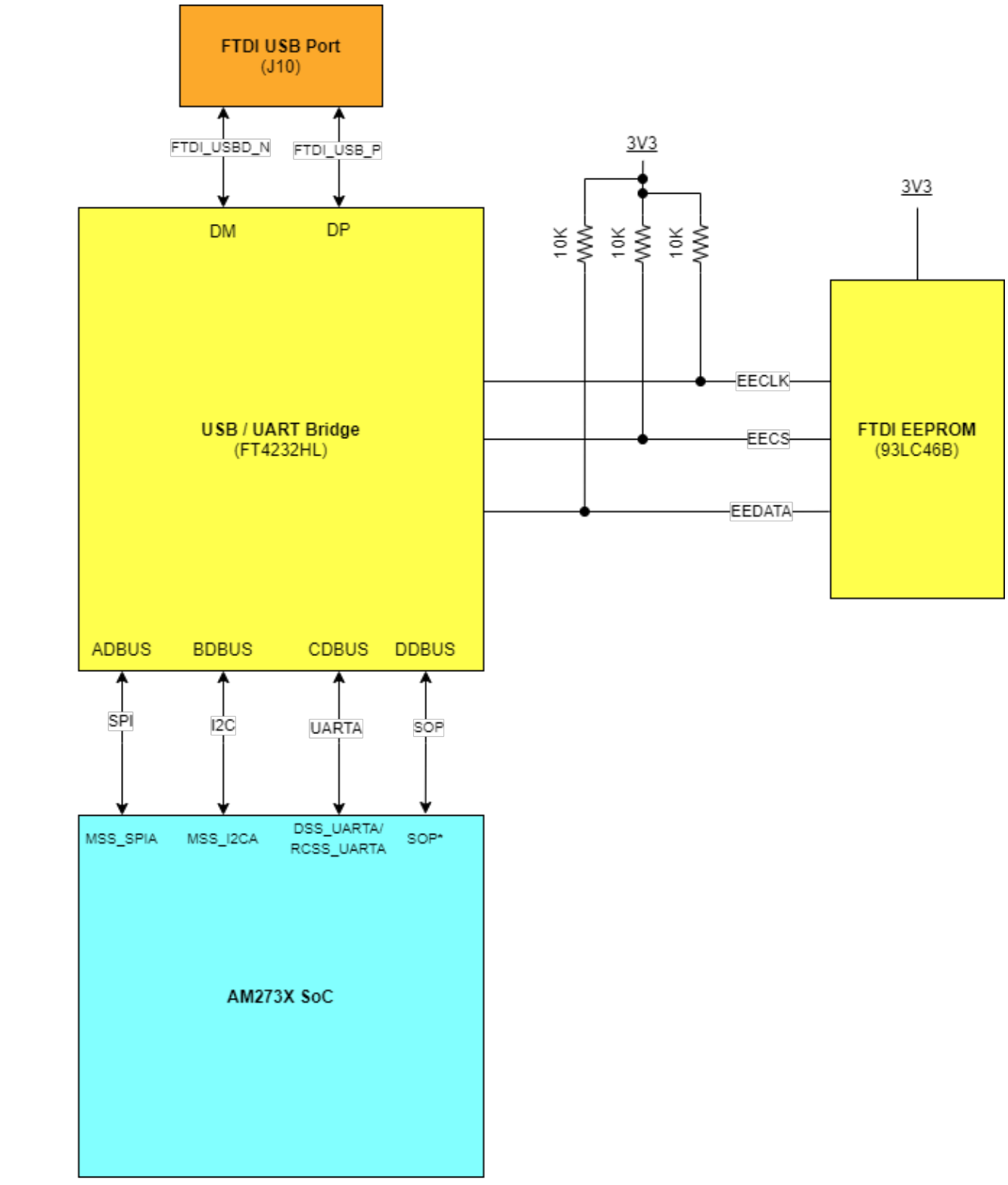

Figure 4-7. FTDI USB Block Diagram

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Table 4-2. J10 Connector Pin

Pin Number	Description	Pin Number	Description
1	FTDI_VBUS	2	FTDI_USBD_N
3	FTDI_USBD_P	4	FTDI_USBID
5	GND	6	GND
7	GND	8	GND
9	GND	10	GND
11	GND		

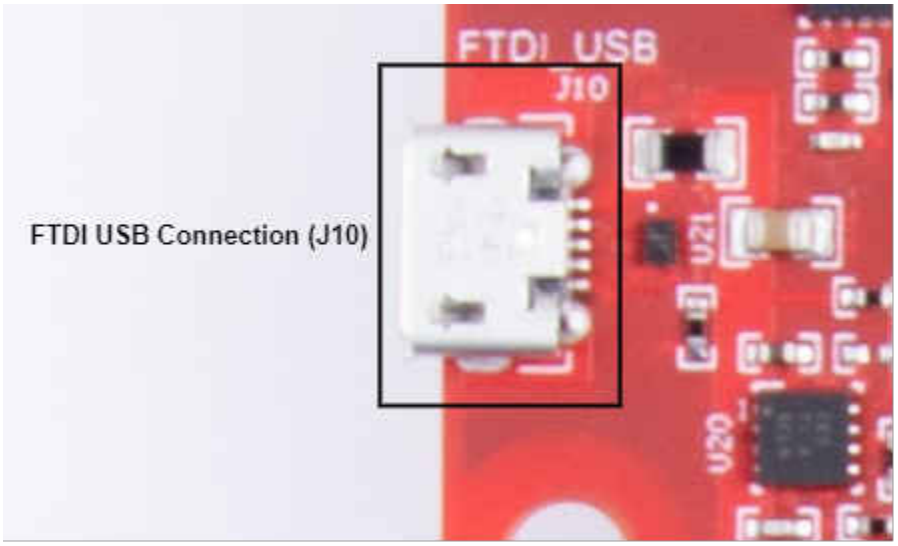

Figure 4-8. FTDI USB Connector

4.4.1.1 FTDI EEPROM Memory Device

The TMDS273GPEVM contains a 1Kb serial EEPROM device (93LC46B from Microchip) that holds the programming information for the FT4232HL USB to UART bridge. By default the 93LC46B contains the power up data for the FT4232HL to boot into a UART configuration.

4.4.2 XDS USB Interface

Micro USB connector J8 provides access to the JTAG and MSS_UARTA interface with the MSS_UARTB transmission line of the AM273x via the XDS110 emulator.

This is the UART interface used to flash the binary to the onboard serial flash and for OOB demo.

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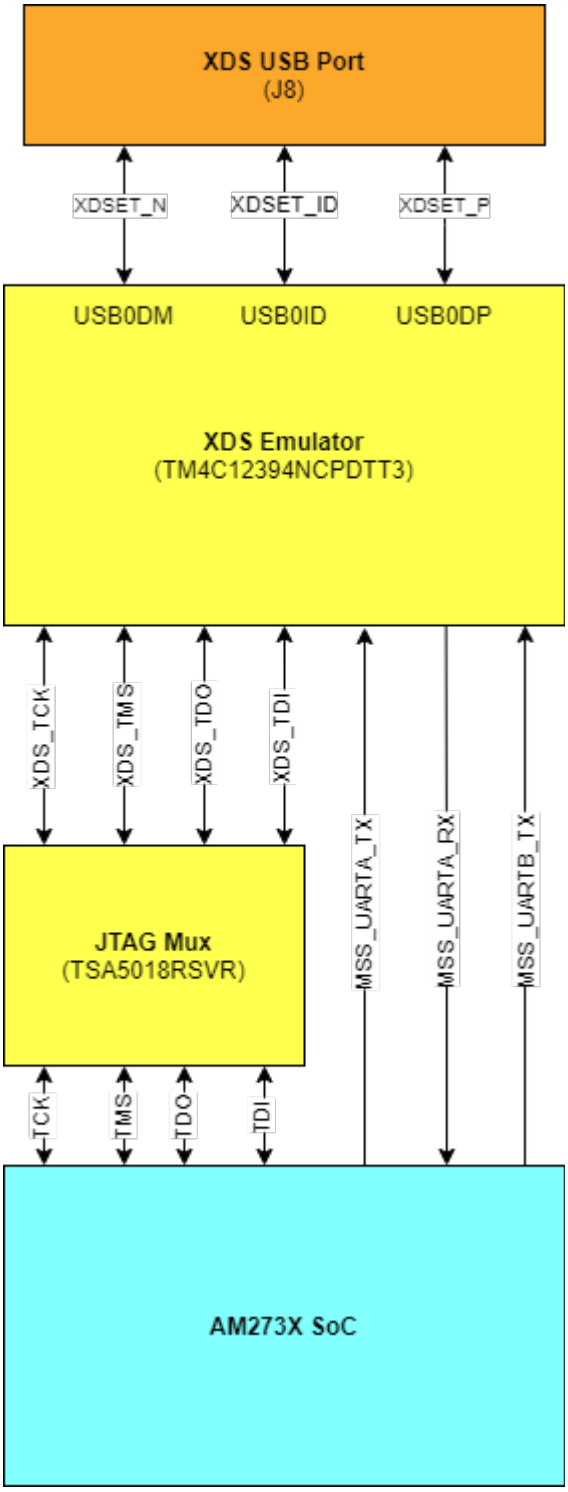

Figure 4-9. XDS USB Interface Block Diagram

Table 4-3. J8 Connector Pin

Pin Number	Description	Pin Number	Description
1	XDSET_VBUS	2	XDSET_D_N
3	XDSET_D_P	4	XDSET_ID
5	GND	6	GND
7	NC	8	NC
9	GND	10	GND

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Table 4-3. J8 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
11	GND		

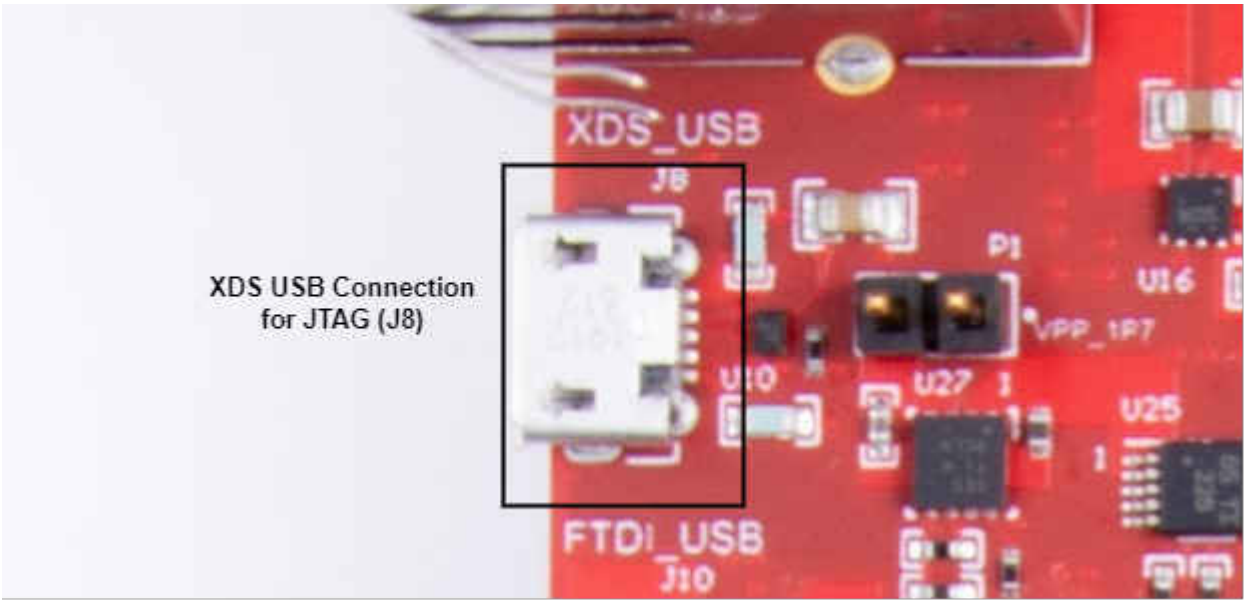


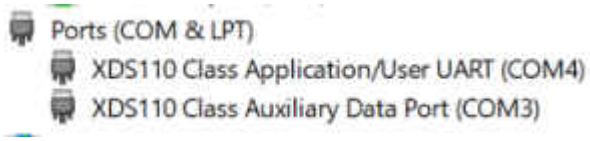
Figure 4-10. XDS USB Connector

4.4.3 PC Connection

The connectivity is provided through the micro USB connector over the onboard XDS110 (TM4C1294NCPDT) emulator. This provides the following interfaces to the PC:

- JTAG for CCS connectivity
- MSS logger UART. This can be used to get MSS code logs on the PC

When the USB is connected to the PC, the device manager should recognize two XDS110 COM ports under Ports (COM and LPT):



XDS110 debug probe and data port are detected under Texas Instructions Debug Probes:

If the PC is unable to recognize the above COM ports, install the EMU pack available at the following link:

https://software-dl.ti.com/ccs/esd/documents/xdsdebugprobes/emu_xds_software_package_download.html

4.5 I2C Interface

The AM273x SoC supports three I2C interfaces: MSS_I2CA, RCSS_I2CA, and RCSS_I2CB. The MSS_I2CA lines are muxed out of the controller by default, while the RCSS_I2CA and RCSS_I2CB lines require pin muxing to be accessible. Information regarding the locations of the I2C modules for the AM273x can be found in the Pin Attributes section of the AM273x datasheet.

- **MSS_I2CA Interface**:

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  - Default pins:
    - MSS_I2CA_SDA: F16
    - MSS_I2CA_SCL: F18
  - Identify the EVM through the Board ID memory device (CAV24C02WE-GT3)
  - Read 1.2V, 1.8V, and 3.3V digital supply current sensors
  - Read 1.2V SRAM supply current sensor
  - Read temp sensor
  - Interface with 60 pin debug connector

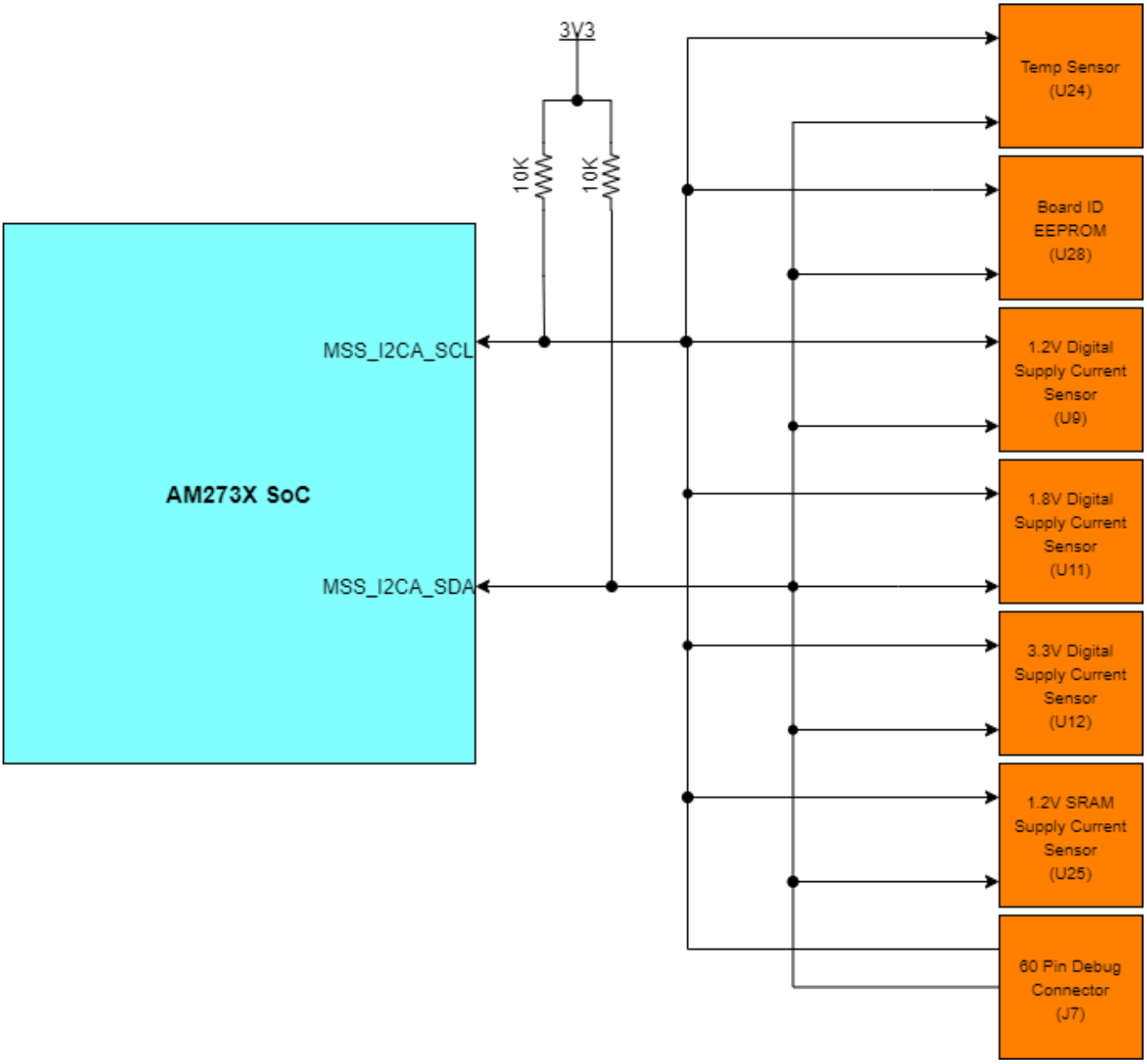

Figure 4-11. MSS_I2CA Block Diagram

- **RCSS_I2CA:**
  - Not available on the TMDS273GPEVM by default
- **RCSS_I2CB:**
  - Not available on the TMDS273GPEVM by default

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4.5.1 I2C Connections

The board features temperature sensor for measuring onboard temperature, current sensors for current measurement for 1.2-V, 1.8-V, and 3.3-V AM273x supply rails, and EEPROM for storing board ID. These are connected to the TMDS273GPEVM through the I2C bus.

Table 4-4 shows the list of I2C devices available in the TMDS273GPEVM board and its address.

Table 4-4. I2C Devices and Addresses

Sensor Type	Reference Designator	Part Number	Slave Address
Temp sensor	U24	TMP112AIDRLR	0x49
Current sensor for 3.3-V rail	U12	INA226AIDGSR	0x44
Current sensor for 1.8-V rail	U11	INA226AIDGSR	0x41
Current sensor for 1.2-V Digital rail	U9	INA226AIDGSR	0x40
Current sensor for 1.2-V SRAM rail	U25	INA226AIDGSR	0x45
EEPROM	U28	CAV24C02WE-GT3	0x50

4.6 UART Interface

The AM273x is composed of four UART interfaces:

- Two Main Subsystem Modules (MSS_UARTA and MSS_UARTB)
  - MSS_UARTA_RX and MSS_UARTA_TX are accessible through the XDS110 USB port (J8) via the XDS emulator.
  - MSS_UARTB_TX is available via the XDS110 USB port (J8) via the XDS emulator while MSS_UARTB_RX is not acessible by the default pin mux on the AM273x EVM.
- One Radar Controller Subsystem Module (RCSS_UARTA)
  - RCSS_UARTA is not available in the standard hardware configuration of the AM273x EVM. However, this port can be accessed if resistors R160 and R164 are depopulated with resistors R156 and R159 populated with 0 ohm resistors. This alteration will make RCSS_UARTA_RX and RCSS_UARTA_TX accessible via the FTDI USB port (J8) as replacements of the DSS_UART interface.
- One DSP Subsystem Module (DSS_UARTA)
  - DSS_UARTA_RX and DSS_UARTA_TX are accessible thorugh the FTDI USB port (J10) via the FT4232HL UART - USB Bridge.

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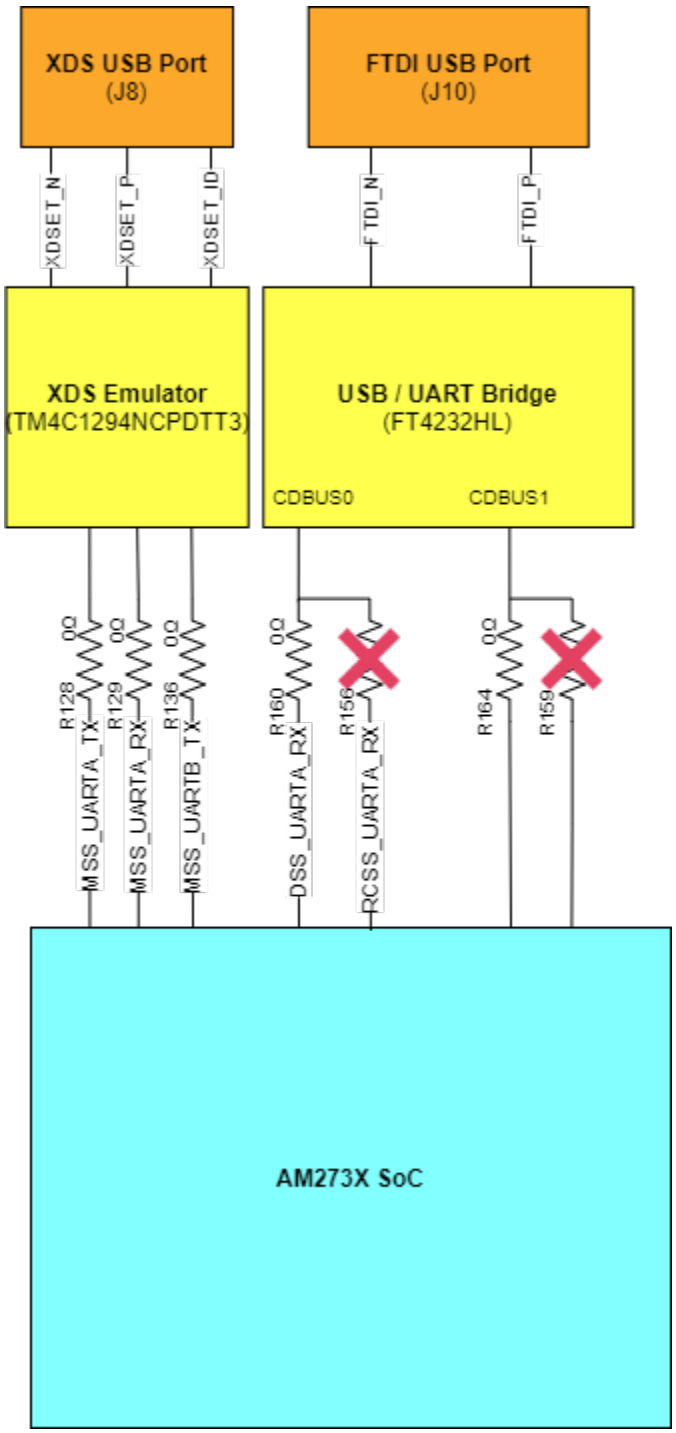

Figure 4-12. UART Interface

4.7 CAN Interfaces

4.7.1 CAN-A Interface

The J3 connector provides the CANA_L and CANA_H signals from the onboard can CAND-FD transceiver (TCAN1042HGVDRQ1). These can be directly wired to the CAN bus.

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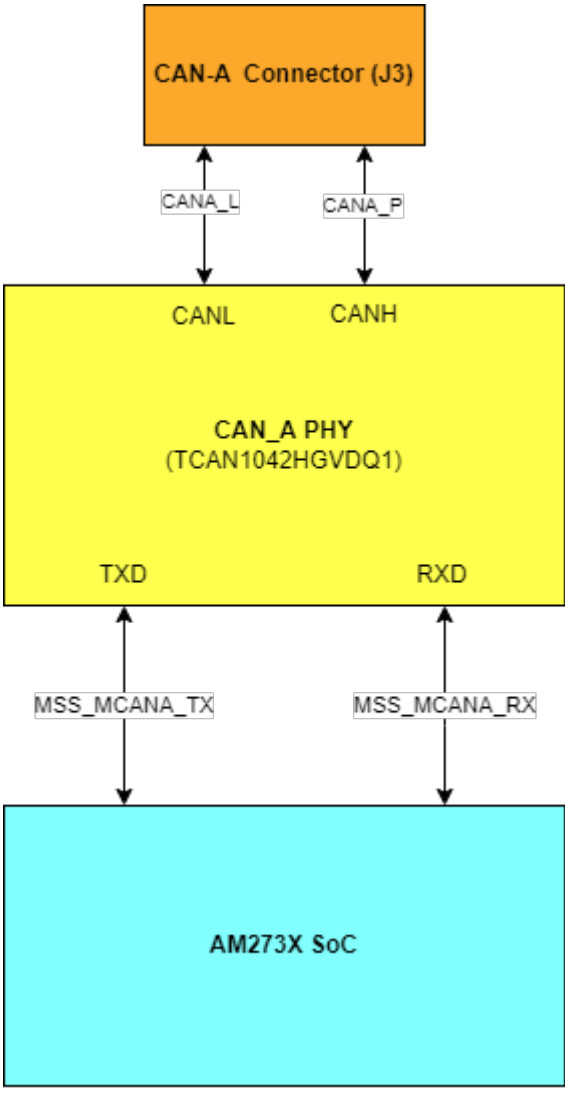

Figure 4-13. CAN-A Interface Block Diagram

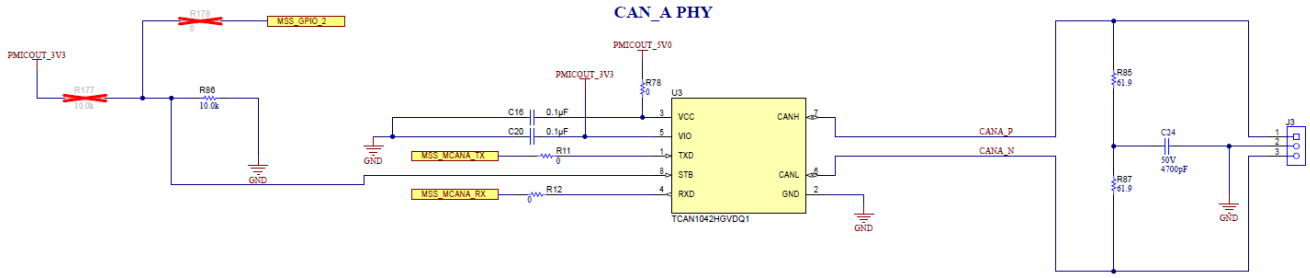

Figure 4-14. CAN-A Schematic

4.7.2 CAN-B Interface

The J2 connector provides the CANB_L and CANB_H signals from the onboard can CAND-FD transceiver (TCAN1042HGVDRQ1). These can be directly wired to the CAN bus.

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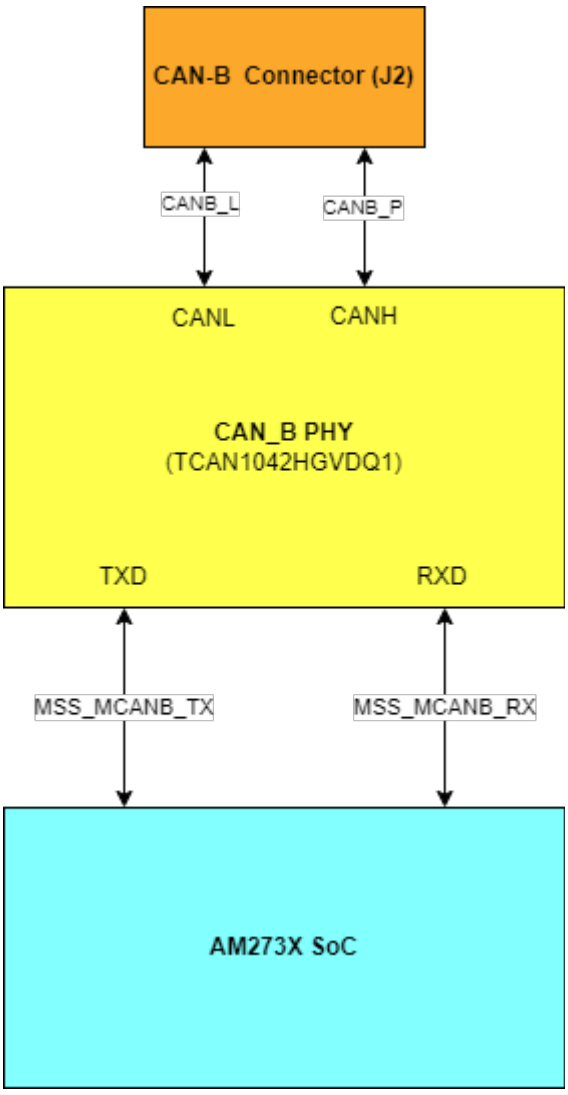

Figure 4-15. CAN-B Interface Block Diagram

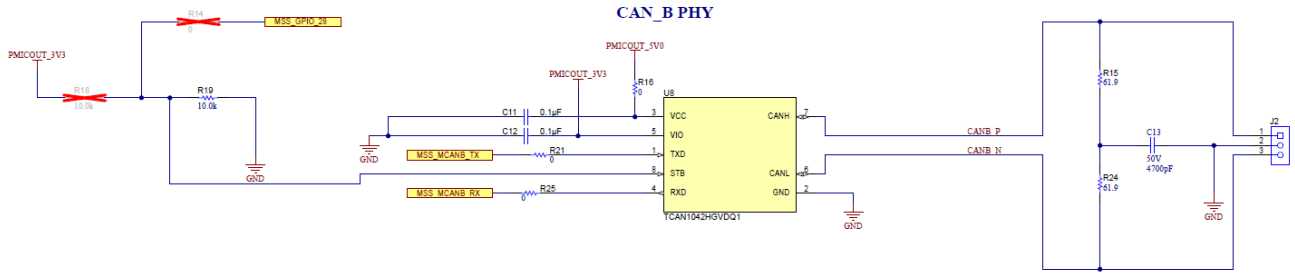

Figure 4-16. CAN-B Schematic

4.8 JTAG Emulation

The AM273x EVM includes the necessary circuitry for XDS110 emulation. The XDS110 class on-board emulation is used to support testing of software builds. The connection for the emulator uses a USB 2.0 micro-B connection (J8).

Alternatively, off-board emulation can be used to interface with the EVM through the MIPI 60 header (J19) or the 60 Pin Debug Header (J7). The XDS USB Port and the 60 pin headers are muxed at the TS3A5018RSVR

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analog switch (U23). The line for this mux selection is determined by the state of switch S1. When S1 is set to 'MIPI,' the signals will be routed to the MIPI 60 Header (J19) and 60 Pin Debug Header (J7). When S1 is set to 'XDS,' the signals will be routed to the emulator and XDS USB port (J8).

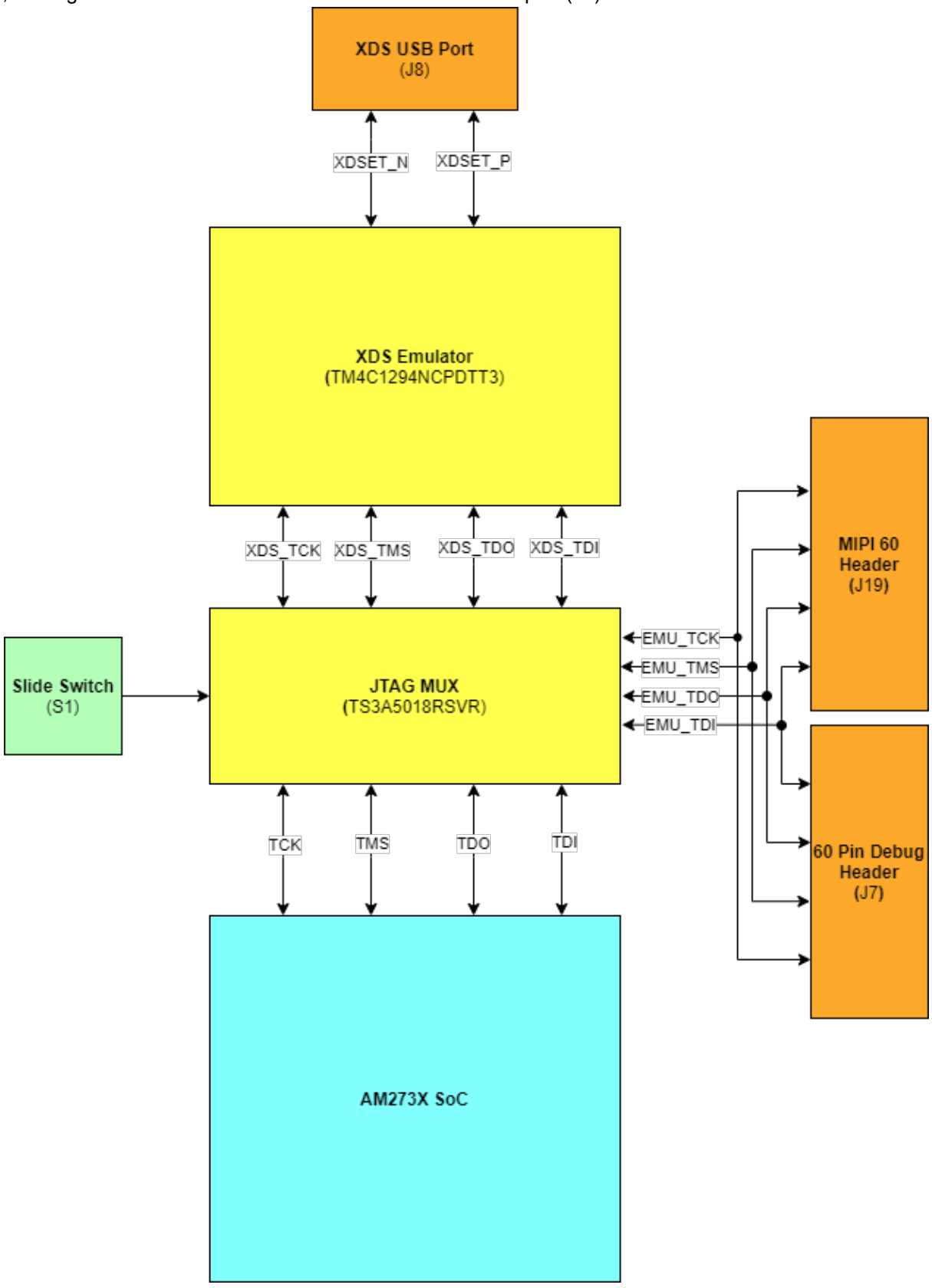

Figure 4-17. JTAG Emulation Block Diagram

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4.9 SPI Interface

The EVM supports four SPI interfaces:

- Two Main Subsystem Interfaces:
  - MSS_SPIA is accessible through the FTDI USB port (J10) via the FT4232HL UART USB bridge.
  - MSS_SPIB is multiplexed out via the TS3A5018RSVR multiplexor to either the PMIC and debug test pins (J16) or the 60 Pin Debug Header (J7). The TS3A5018RSVR mutliplexor is driven by S2 which acts as a select line. When set to 'PMIC_SPI' position, the MSS_SPIB interface is routed to the PMIC and J16 header. When set to ‘DBG_SPI’, the MSS_SPIB interface is routed to the 60-pin debug header (J7). The CS1 line of the MSS_SPIB interface bypasses the multiplexor and is routed directly to the 60 Pin Debug Header.

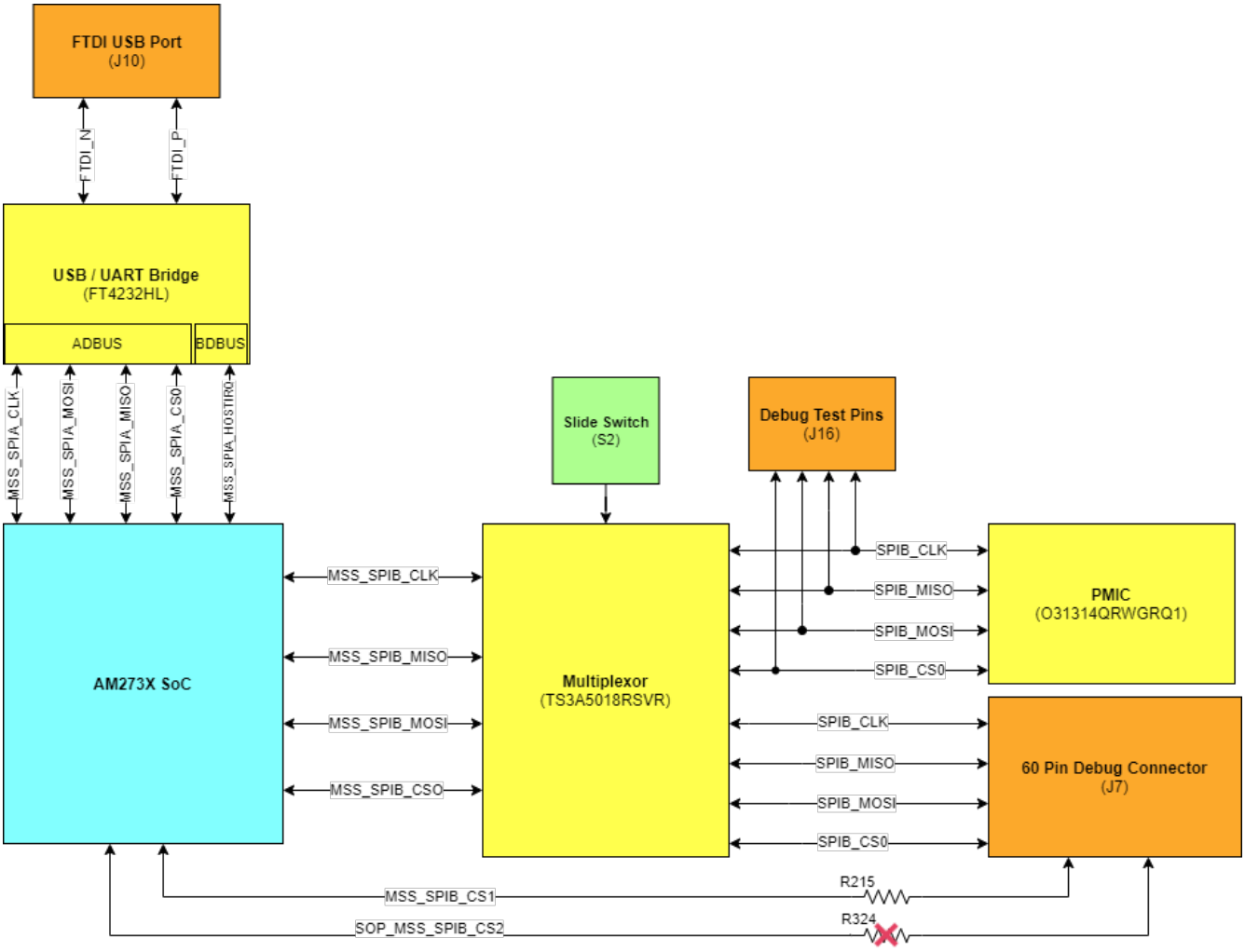

Figure 4-18. MSS SPI Interface

- Two Radar Control Subsystem Intefaces:
  - RCSS_SPIA is routed to the HD front end connector J1.
  - RCSS_SPIB is routed to the HD front end connector J11.

4.10 MDI Interface

The TMDS273GPEVM has a two signal (clock and data) MDI interface. This interface's purpose is to configure the Ethenet PHY. Since a PHY (TI's DP83867ERGZR) is established for the EVM, the EVM's software is set to properly configure this PHY by default.

Please refer to Figure 4-5 for more detail on the Ethernet PHY design.

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4.11 ePWM Interface

The TMDS273GPEVM has one enhanced pulse-width modulator (ePWM) interface available on an external header. MSS_EPWMA0 is routed to pin 6 of the 60 pin debug header.

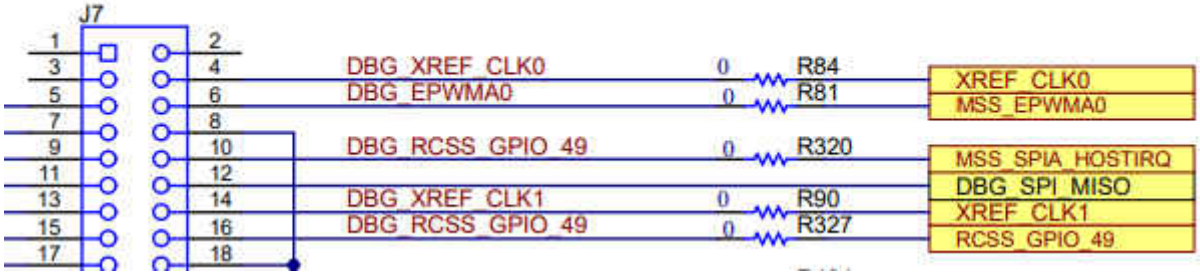

Figure 4-19. ePWM Debug Header Pin

Please see Section 5.4 for further detail on the Debug Connector pinout.

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5 Connectors

5.1 60-Pin High Density (HD) FE Connector-1 (J1)

The 60-pin HD connector-1 provides the high speed 4-lane CSI interface, SPI, UART, I2C, and controls signals (NRST, NERR, WRMRST, REFCLK, OSCCLK, SOPs). This can be connected to the AWR2243BOOST EVM board to interface to the front end radar device.

Figure 5-1. High Density FE Connector-1 Schematic

Table 5-1. J1 Connector Pin

Pin Number	Description	Pin Number	Description
1	5V	2	5V
3	5V	4	NC
5	NC	6	NC
7	RCSS_SPIA_CS	8	NC
9	RCSS_SPIA_CLK	10	RCSS_SPIA_HOSTINT
11	RCSS_SPIA_MOSI	12	RCSS_SPIA_MISO
13	NC	14	NERRIN_FE1
15	NC	16	HW_SYNC_FE1
17	NC	18	GND
19	NC	20	NC
21	NC	22	NC
23	NC	24	GND
25	NC	26	NC
27	NC	28	NC
29	NC	30	GND
31	NC	32	CSI2_RX0_3P
33	SOP0_FE1	34	CSI2_RX0_3N
35	SOP1_FE1	36	GND
37	SOP2_FE1	38	CSI2_RX0_2P

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Table 5-1. J1 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
39	WRMRST_FE1	40	CSI2_RX0_2N
41	GND	42	GND
43	REFCLK_FE1	44	CSI2_RX0_CLKP
45	GND	46	CSI2_RX0_CLKN
47	OSCCLK_FE1	48	GND
49	GND	50	CSI2_RX0_1P
51	I2CA_SDA	52	CSI2_RX0_1N
53	I2CA_SCL	54	GND
55	NC	56	CSI2_RX0_0P
57	NC	58	CSI2_RX0_0N
59	nRESET_FE1	60	GND

5.2 60-Pin High Density (HD) FE Connector-2 (J11)

The 60-pin HD connector-2 provides the high speed 4-lane CSI interface, SPI, UART, I2C, and controls signals (NRST, NERR, WRMRST, REFCLK, SOPs). This can be connected to the AWR2243BOOST EVM board to interface with the second front end radar device in cascade configuration.

Figure 5-2. High Density FE Connector-2 Schematic

Table 5-2. J11 Connector Pin

Pin Number	Description	Pin Number	Description
1	5V	2	5V
3	5V	4	NC
5	NC	6	NC
7	RCSS_SPIB_CS	8	NC
9	RCSS_SPIB_CLK	10	RCSS_SPIB_HOSTINT
11	RCSS_SPIB_MOSI	12	RCSS_SPIB_MISO
13	NC	14	NERRIN_FE2
15	NC	16	HW_SYNC_FE2

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Table 5-2. J11 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
17	NC	18	GND
19	NC	20	NC
21	NC	22	NC
23	NC	24	GND
25	NC	26	NC
27	NC	28	NC
29	NC	30	GND
31	NC	32	CSI2_RX1_3P
33	SOP0_FE2	34	CSI2_RX1_3N
35	SOP1_FE2	36	GND
37	SOP2_FE2	38	CSI2_RX1_2P
39	WRMRST_FE2	40	CSI2_RX1_2N
41	GND	42	GND
43	REFCLK_FE2	44	CSI2_RX1_CLKP
45	GND	46	CSI2_RX1_CLKN
47	NC	48	GND
49	GND	50	CSI2_RX1_1P
51	I2CB_SDA	52	CSI2_RX1_1N
53	I2CB_SCL	54	GND
55	NC	56	CSI2_RX1_0P
57	NC	58	CSI2_RX1_0N
59	nRESET_FE2	60	GND

5.3 MIPI 60-Pin Connector (J19)

This connector provides the standard MIPI 60-pin interface for JTAG and trace capability through emulators such as the XDS560pro. Further information on the emulation and trace header can be found in the Emulation and Trace Headers Technical Reference Manual.

To use this interface, the JTAG lines from the TMDS273GPEVM must be muxed to MIPI 60-pin connector.

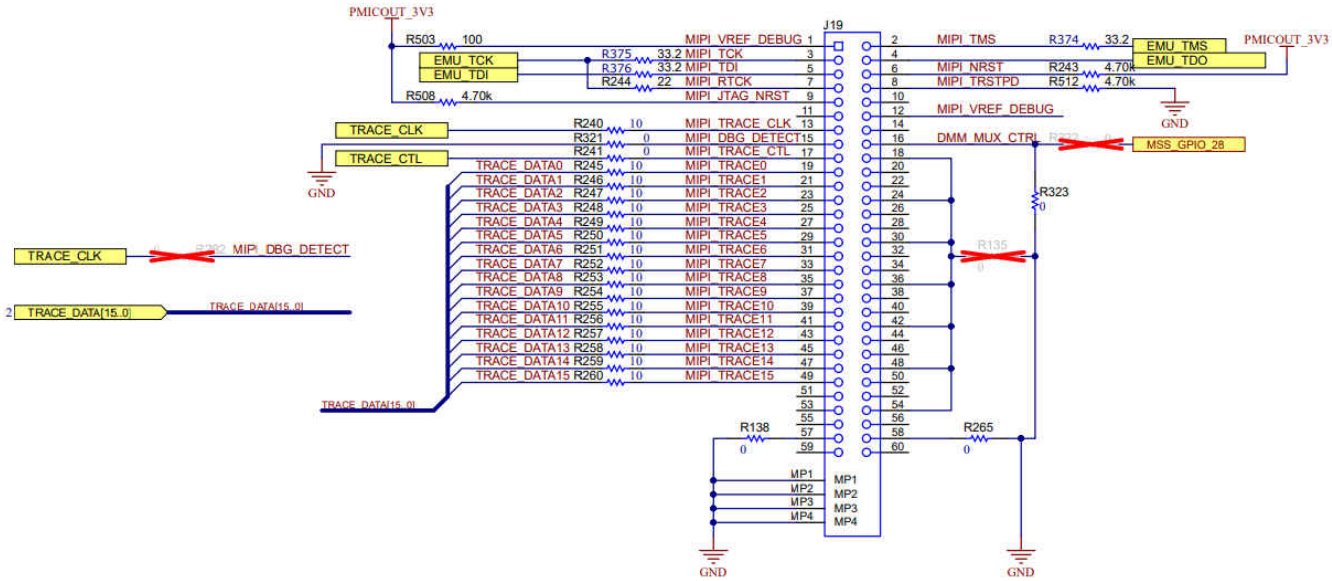

Figure 5-3. MIPI 60 Connector Schematic

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Table 5-3. J19 Connector Pin

Pin Number	Description	Pin Number	Description
1	MIPI_VREF	2	MIPI_TMS
3	MIPI_TCK	4	MIPI_TDO
5	MIPI_TDI	6	MIPI_NRST
7	MIPI_RTCK	8	MIPI_TRSTPD
9	MIPI_JTAG_NRST	10	NC
11	NC	12	MIPI_VREF
13	MIPI_TRACE_CLK	14	NC
15	MIPI_DBG_DETECT	16	GND
17	MIPI_TRACE_CTL	18	NC
19	MIPI_TRACE0	20	NC
21	MIPI_TRACE1	22	NC
23	MIPI_TRACE2	24	NC
25	MIPI_TRACE3	26	NC
27	MIPI_TRACE4	28	NC
29	MIPI_TRACE5	30	NC
31	MIPI_TRACE6	32	NC
33	MIPI_TRACE7	34	NC
35	MIPI_TRACE8	36	NC
37	MIPI_TRACE9	38	NC
39	MIPI_TRACE10	40	NC
41	MIPI_TRACE11	42	NC
43	MIPI_TRACE12	44	NC
45	MIPI_TRACE13	46	NC
47	MIPI_TRACE14	48	NC
49	MIPI_TRACE15	50	NC
51	NC	52	NC
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	NC	60	NC

5.4 Debug Connector 60-Pin (J7)

This connector enables interfacing of LVDS signals to the DCA1000 EVM for data capturing purposes as well as SPI, I2C, JTAG, GPADC, and other control signals from the TMDS273GPEVM for debug purposes.

The SPI interface must be muxed to the Debug Connector. For more details, refer to Section 3.3.

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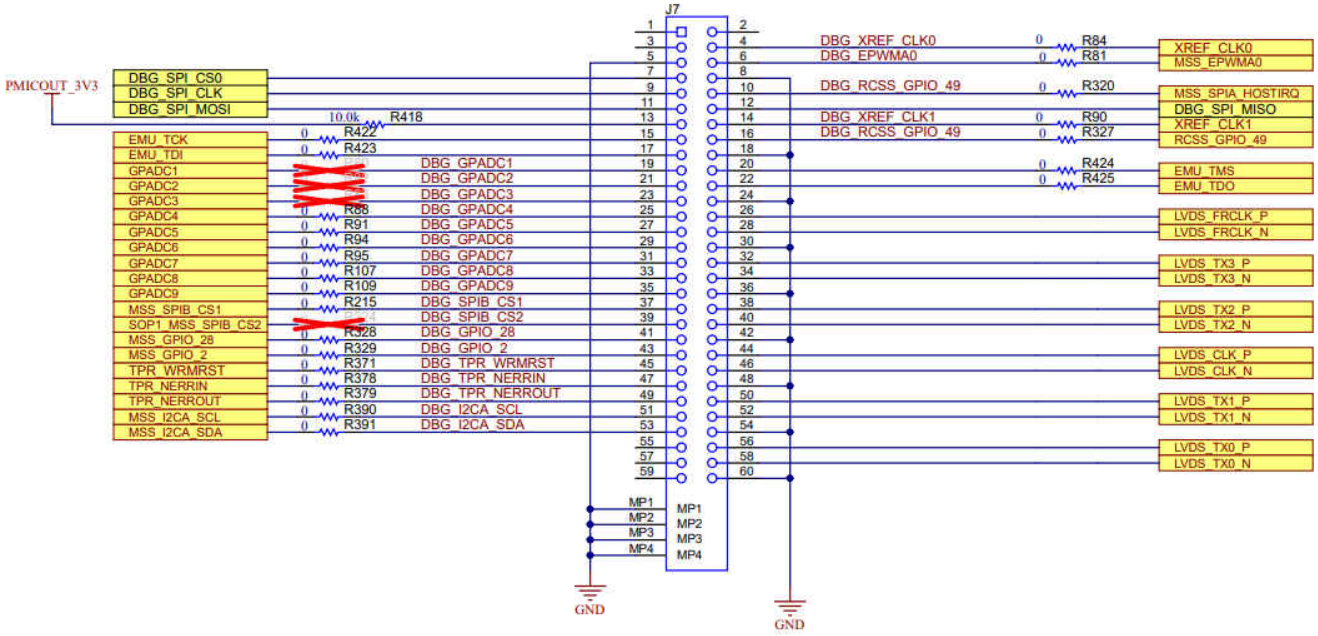

Figure 5-4. Debug Connector Schematic

Table 5-4. J7 Connector Pin

Pin Number	Description	Pin Number	Description
1	NC	2	NC
3	NC	4	XREF_CLK0
5	GND	6	MSS_EPWMA0
7	MSS_SPIB_CS0	8	GND
9	MSS_SPIB_CLK	10	MSS_SPIA_HOSTIRQ
11	MSS_SPIB_MOSI	12	MSS_SPIB_MISO
13	3.3V PULL_UP	14	XREF_CLK1
15	EMU_TCK	16	RCSS_GPIO_49
17	EMU_TDI	18	GND
19	GPADC1	20	EMU_TMS
21	GPADC2	22	EMU_TDS
23	GPADC3	24	GND
25	GPADC4	26	LVDS_FRCLK_P
27	GPADC5	28	LVDS_FRCLK_N
29	GPADC6	30	GND
31	GPADC7	32	LVDS_TX3_P
33	GPADC8	34	LVDS_TX3_N
35	GPADC9	36	GND
37	MSS_SPIB_CS1	38	LVDS_TX2_P
39	SOP1_MSS_SPIB_CS2	40	LVDS_TX2_N
41	MSS_GPI0_28	42	GND
43	MSS_GPI0_2	44	LVDS_CLK_P
45	TPR_WRMRST	46	LVDS_CLK_N
47	TPR_NERRIN	48	GND
49	TPR_NERROUT	50	LVDS_TX1_P
51	MSS_I2CA_SCL	52	LVDS_TX1_N

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Table 5-4. J7 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
53	MSS_I2CA_SDA	54	
55	NC	56	LVDS_TX0_P
57	NC	58	LVDS_TX0_N
59	NC	60	GND

5.5 External Clock Option (J13, J1)

The AM273x SoC can operate with external clock source provided from J13 connector or clock provided from Radar FE via OSCK_FE1 on connector J1 (the HD Front End Connector).

It supports externally driven clock (Square/Sine) at 40/50 MHz.

Note

To enable an external clock source from the J13 connector, the R269 resistor must be populated on board.

To enable an external clock from the J1 connector, the R281 resistor must be populated on board.

Refer to the AM273x data sheet for external clock specifications.

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6 Mechanical Mounting of the PCB

The spacers and screws provided with the TMDS273GPEVM kit help to arrest the TMDS273GPEVM in the horizontal plane. Figure 6-1 shows the assembly of mechanical spacers to the board.

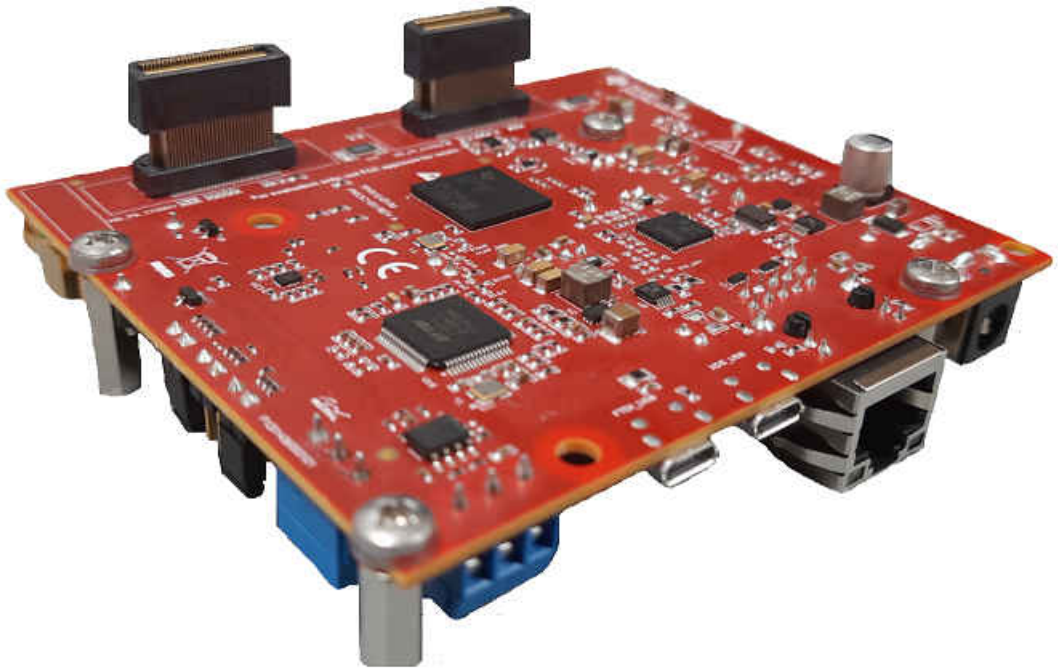

Figure 6-1. TMDS273GPEVM Mechanical Assembly

The L-brackets provided with the AWR2443 EVM kit, along with the screws and nuts, help in the vertical mounting of the EVM. Figure 6-2 shows how the L-brackets can be assembled.

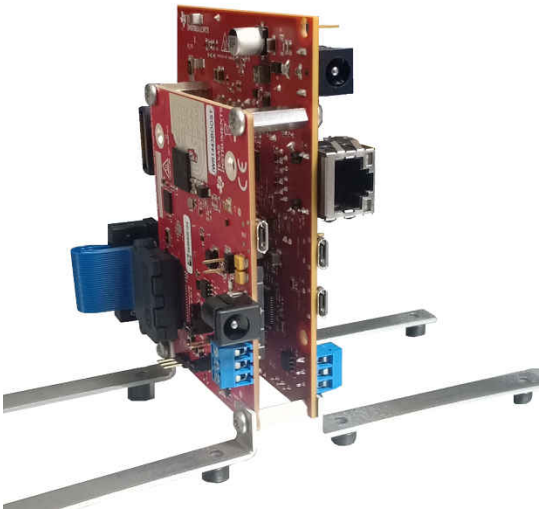

Figure 6-2. TMDS273GPEVM Interfaced to the AWR2944BOOST EVM

The TMDS273GPEVM is designed to interface with the DCA1000 EVM on Debug Connector (J7). Figure 6-3 shows how the TMDS273GPEVM can be connected to the DCA1000 EVM.

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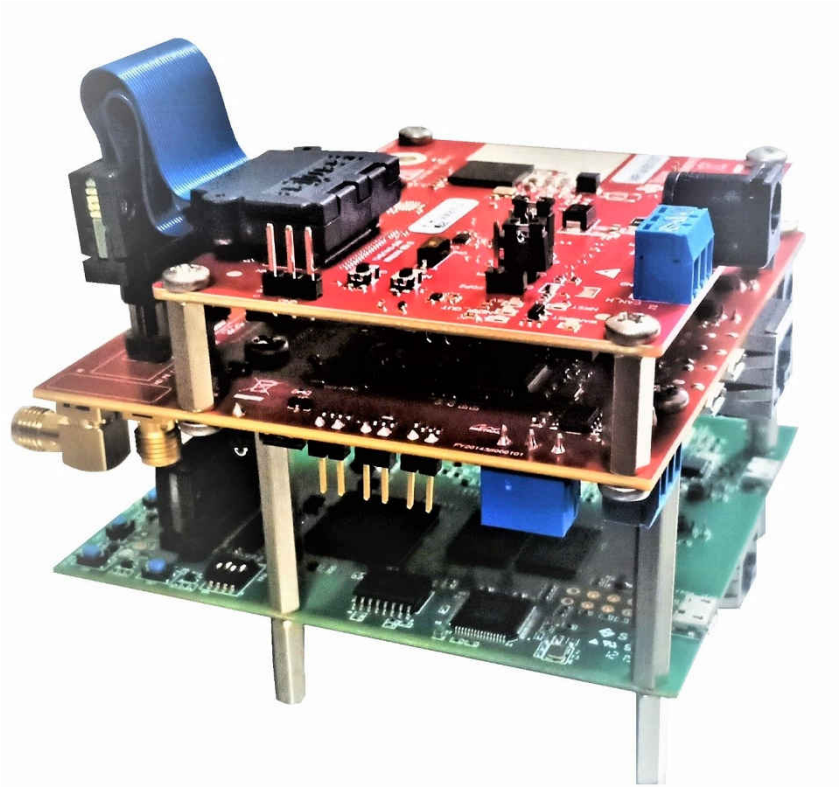

Figure 6-3. TMDS273GPEVM Interfaced to the DCA1000 EVM

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3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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