Application Report
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Transitioning Designs From Stellaris® LM3S Microcontrollers to Tiva™ C Series Microcontrollers

Sue Cozart

ABSTRACT

This application report addresses design considerations when migrating working designs from Stellaris LM3S microcontrollers to Tiva C Series microcontrollers. Topics covered include software and hardware considerations as well as feature changes and enhancements. Software migration is very straightforward when using the Driver Library APIs in the StellarisWare® and TivaWare™ for C Series software.

Contents

1 Introduction

The purpose of this document is to highlight items that should be considered when migrating designs from Stellaris LM3S microcontrollers to Tiva C Series microcontrollers. Both families are based on the ARM® Cortex™-M core, and the peripherals are generally very similar, and in some cases identical. In addition, the Tiva C Series MCUs offer lower power consumption, robust Flash memory technology, enhanced analog capabilities, hardware floating point to accelerate math-intensive operations, and a variety of price and performance points. When using DriverLib APIs, code can easily be migrated between MCU families as well as from StellarisWare to TivaWare for C Series.

The primary focus of this document is those items that require changes to a Tiva C Series system design if they are originally implemented with a Stellaris LM3S device. In addition, enhanced features that can save system cost are also highlighted.

2 Determining the Product Class

In this document, information is presented in terms of product class. To determine what class a particular microcontroller is in, see the CLASS field in the Device Identification 0 (DID0) register at offset 0x400F.E000. The CLASS designations in this register are as follows:

- Sandstorm - 0x0
- Fury - 0x1
- DustDevil - 0x3
- Tempest - 0x4
- Firestorm - 0x6
- TM4C123x - 0x5
- TM4C129x - 0xA

To determine which microcontrollers are in a particular class, check the following TI web pages:

- Sandstorm-class
- Fury-class
- DustDevil-class
- Tempest-class
- Firestorm-class

3 Using this Document

This application report focuses on items to consider when migrating designs. Additional documentation is available:

- For more information on any particular microcontroller feature, see: the device-specific data sheet and errata documents.
- To read about the differences between device classes, see: *Differences Among Stellaris® LM3S and Tiva™ C Series TM4C123x MCUs* (SPMA035) and *Differences Between Stellaris® Tempest- and Firestorm-Class MCUs and Tiva™ C Series TM4C129x MCUs* (SPMA063).
- For more details on software differences, see: *Migrating Software Projects from StellarisWare® to TivaWare™* (SPMA050).
- For recommendations on designing a successful TM4C system design, see:
  - *System Design Guidelines for the TM4C129x Family of Tiva™ C Series Microcontrollers* (SPMA056)
  - *System Design Guidelines for the TM4C123x Family of Tiva™ C Series Microcontrollers* (SPMA059)

4 Pinout Considerations

One of the goals for the Tiva C Series MCUs was to increase the number of available GPIOs. As a result, the pinout has been changed between the LM3S and the TM4C MCUs. In addition, greater flexibility for system design was introduced with pin muxing on some later LM3S devices, and this concept has been carried over to the TM4C MCUs. While not directly pin compatible, Table 1 shows that most fixed pins are in the same general location on the package.

Table 1. Pinout Comparison

Feature	Sandstorm	Fury	DustDevil	Tempest/ Firestorm	TM4C123x	TM4C129x
ADC	Top left corner					
Hibernate	N/A	Bottom right corner				
JTAG	Right side of top					
LDO/VDD25/ VDDC (1)	LDO pin only, center left side	LQFP package - Center each side, LDO pin on top of left side BGA package - Left side of center opening	Center each side, LDO pin on top of left side	LQFP package - Center top and bottom sides, LDO pin on top of left side BGA package - Left side of center opening	LQFP package - Center top side, center bottom side BGA package - Center at the top and bottom of center opening and third pin in center on left side	LQFP package - Center top side, center bottom side BGA package - Center at top and right of center cluster
UART0	Center of bottom side	Left side of bottom				
SSI0	Center of bottom side	Left side of bottom				
I2C0	Top of right side					
USB0	N/A		Top of right side			
Ethernet	N/A	LQFP package - Center and right side of bottom, center of right side; XTAL pins center left side BGA package - Bottom right corner; XTAL pins center left side	N/A	LQFP package - Center and right side of bottom, center of right side; XTAL pins center left side BGA package - Bottom right corner; XTAL pins center left side	N/A	Right side of bottom; separate XTAL no longer needed
Reset	Center of left side	Center of right side				Bottom of right side
Oscillator pins	Bottom of left side	Right side of bottom			Center of right side	

(1) Some LM3S devices have VDD25 and LDO pins and others have VDDC and LDO pins. TM4C devices only have VDDC pins.

Pin muxing provides system designers with a great deal of control over the placement and selection of peripheral module signals that are alternate functions for GPIO signals. These pins can be customized to provide the best possible signal combination for each individual system design. Texas Instruments provides a Pin Mux Utility to allow a developer to graphically configure the device peripherals in an intuitive and rapid manner. The tool provides an easy-to-use interface that makes setting up alternate functions for GPIOs easy and error-free.

Two pinout changes that should be specifically noted are:

- The `NMI` pin is located on `PB7` for DustDevil-, Tempest-, and Firestorm-class devices (Sandstorm- and Fury-class do not have `NMI` pins), but on TM4C123x devices, the `NMI` pin is on either `PD7` or `PF0`, and on TM4C129x devices, the `NMI` pin is on either `PD7` or `PE7`. Note that all pins with NMI as an alternate function are under GPIO commit control and must be unlocked before their function can be changed.

- SSI0Tx is on pin PA5 and SSI0Rx is on pin PA4 for all LM3S devices as well as TM4C123x devices. On TM4C129x devices, the function of SSI0Tx is on pin SSI0XDAT0, which is on pin PA4, and the function of SSI0Rx is on pin SSI0XDAT1, which is on pin PA5.

5 Packaging

Table 2 shows the available packages for each class of devices.

Table 2. Available Packages

Feature	Sandstorm	Fury	DustDevil	Tempest/ Firestorm	TM4C123x	TM4C129x
48-pin LQFP, 7 x 7 mm body size, 0.50 mm pitch	Yes	-	-	-	-	-
64-pin LQFP, 10 x 10 mm body size, 0.50 mm pitch	-	-	Yes	Yes	Yes	-
100-pin LQFP, 14 x 14 mm body size, 0.50 mm pitch	-	Yes	Yes	Yes	Yes	-
108-ball BGA, 10 x 10 mm body size, 0.8 mm pitch, 12 x 12 array	-	Yes	Yes	Yes	-	-
128-pin TQFP, 14 x 14 mm body size, 0.40 mm pitch	-	-	-	-	-	Yes
144-pin LQFP, 20 x 20 mm body size, 0.50 mm pitch	-	-	-	-	Yes	-
157-ball BGA, 9 x 9 mm body size, 0.65 mm pitch, 13 x 13 array	-	-	-	-	Yes	-
212-ball BGA, 10 x 10 mm body size, 0.5 mm pitch, 19 x 19 array	-	-	-	-	-	Yes

6 Power Considerations

NOTE: All LM3S and Tiva C Series devices require only a 3.3 V supply. On TM4C123x devices, the minimum V_{DD} is 3.15 V, which differs from the minimum V_{DD} of 3.0 V on LM3S devices. The minimum V_{DD} on TM4C129x devices is 2.97 V.

Additional supply voltages are generated internally by on-chip LDO regulators. On TM4C devices, the LDO input is no longer brought out of the package. However, the core voltage, V_{DDC}, continues to be visible externally, as it requires filter and decoupling capacitors. When migrating designs to Tiva C Series MCUs, attention must be paid to the values of these capacitors, as they may be different. For more information, see the *On-Chip Low Drop-Out (LDO) Regulator* section of the *Electrical Characteristics* chapter in the device-specific data sheet. External regulators are not supported.

In addition, the regulated value of the LDO could be changed in Run mode on Sandstorm-, Fury-, and DustDevil-class devices. The TM4C devices support this capability only in Deep-sleep mode.

NOTE: All LM3S and TM4C123x devices provide 5-V tolerant general-purpose inputs. However, TM4C129x devices only support 3.3-V tolerant general-purpose inputs. When migrating designs to TM4C129x MCUs, ensure that all GPIOs do not have input voltages greater than the maximum VIH specified in the *Electrical Characteristics* section in the device-specific data sheet. The only exception to this specification is the USB VBUS input, which is 5-V tolerant.

Due to process and architectural improvements, Run mode power consumption is greatly reduced between LM3S and TM4C123x devices as shown in Table 3.

Table 3. Nominal Power Consumption Comparison (1)

Feature	Sandstorm	Fury	DustDevil	Tempest/ Firestorm	TM4C123x	TM4C129x
Run mode 1 (Flash loop, all peripherals on)	95 mA at 50 MHz	156 mA at 50 MHz	135 mA at 50 MHz	70 mA at 50 MHz or 101 mA at 80 MHz, Ethernet PHY powered off 130 mA at 50 MHz or 159 at 80 MHz, Ethernet operating	45 mA at 80 MHz	79 mA at 120 MHz, Ethernet PHY powered off 99 mA at 120 MHz with Ethernet PHY operating
Run mode 2 (Flash loop, all peripherals off)	60 mA at 50 MHz	57 mA at 50 MHz	59 mA at 50 MHz	Not provided	25 mA at 80 MHz	42 mA at 120 MHz
Run mode 1 (SRAM loop, all peripherals on)	85 mA at 50 MHz	148 mA at 50 MHz	133 mA at 50 MHz	Not provided	35 mA at 80 MHz	82 mA at 120 MHz
Run mode 2 (SRAM loop, all peripherals off)	50 mA at 50 MHz	50 mA at 50 MHz	52 mA at 50 MHz	Not provided	15 mA at 80 MHz	43 mA at 120 MHz
Sleep mode (all peripherals off)	19 mA at 50 MHz	21 mA at 50 MHz	25 mA at 50 MHz	14 mA at 50 MHz, 20 mA at 80 MHz	9 mA at 80 MHz, 3.5 mA with PIOSC (16 MHz), 2.7 mA with PIOSC/ 16 (1 MHz)	23 mA at 120 MHz with Flash in low power mode, 9 mA with PIOSC (16 MHz) with Flash in low power mode, 6 mA with PIOSC/16 (1 MHz) with Flash in low power mode
Deep-sleep mode (all peripherals off)	950 µA at MOSC/16	4.8 mA at IOSC/64	290 µA at IOSC/64	Not usable due to erratum	1.07 mA with LFIOSC (with Flash in low power mode)	0.42 mA with LFIOSC, system clock = PIOSC
Hibernate	N/A	Not usable due to erratum	16 µA at 32.768 kHz	30 µA with RTC disabled, 44 µA with RTC enabled	1.4 µA with RTC disabled, 1.4 µA with RTC enabled, 4.5 µA VDD3ON mode	1.2 µA with RTC disabled, 1.3 µA with RTC enabled, 6.7 µA VDD3ON mode with tamper disabled, 7.5 µA VDD3ON mode with tamper enabled

(1) For more details on the conditions for the measurements provided, see the device-specific data sheet.

The Tiva C Series provide additional modes that are not available on the LM3S devices that lower power consumption in Sleep and Deep-sleep modes. These dynamic power management options include lowering the LDO voltage in Deep-sleep mode, standby and low-power modes for Flash memory and SRAM while in Sleep and Deep-sleep modes, and the ability to power down the PIOSC in deep-sleep mode.

7 Clocking

The Tiva C Series provides an internal precision oscillator (PIOSC) that is not present on some LM3S devices. The PIOSC is accurate enough for some applications not requiring USB or Ethernet such that an external crystal connected to the main oscillator may be omitted. For example, a UART-based application works well using the PIOSC. If an external crystal is used, careful attention should be paid to the selection of the crystal and its supporting components. For more information, see the *Main Oscillator Specifications* section in the *Electrical Characteristics* chapter of the device-specific data sheet.

On TM4C129x devices, the clock control has been completely reimplemented. The Run-Mode Clock Configuration (RCC) and Run-Mode Clock Configuration 2 (RCC2) registers have been removed. Instead, the PLL is configurable and is controlled by the PLL Frequency 0 (PLLFREQ0) and PLL Frequency 1 (PLLFREQ1) registers. MCUs that have a USB module in LM3S and TM4C123x devices have a separate and dedicated PLL for the USB module. On TM4C129x devices, this dedicated PLL is removed, and the USB clock is provided from the main PLL. Care must be taken when choosing PLL and system clock frequencies such that clocking requirements for the USB and ADC modules are met. In addition, when using Ethernet on TM4C129x devices, a 25 MHz clock source must be connected to MOSC. For more information, see the *Clock Configuration* section of the *System Control* section in the device-specific data sheet. An additional result of these clocking changes is that the configuration of the Deep Sleep Clock Configuration Register (DSCLKCFG) register has been changed.

To address these changes in the TM4C129x series, new APIs were added to the Driver Library. When porting code from LM3S or LM4F devices, use the *SysCtlClockFreqSet()* function instead of the *SysCtlClockSet()* function. The *SysCtlClockFreqSet()* function also returns the current clock frequency. All calls to *SysCtlClockSet()* and *SysCtlClockGet()* should be removed and replaced with *SysCtlClockFreqSet()*. In addition, use the *SysCtlDeepSleepClockConfigSet()* function instead of the *SysCtlDeepSleepClockSet()* function.

8 Hibernation Module

The Hibernation module on LM3S devices has some errata that greatly affect its proper operation. The Hibernation module was completely redesigned for Tiva C Series devices and offers robust operation and additional features such as:

- VDD3ON mode, which keeps the I/O ring powered in its state prior to entering hibernation. It requires fewer external components and it is not sensitive to voltage on the I/Os.
- The current consumption in hibernation is lower as shown in Table 3.
- TM4C129x devices have an internal low-frequency oscillator (HIBLFIOSC) dedicated to the Hibernate module. If accurate timing for the RTC is not required, an external crystal is not needed, and the Hibernation module can be clocked from the HIBLFIOSC.
- LM3S devices require an external pull-up on the $\overline{\text{HIB}}$ signal. This pull-up is no longer necessary on TM4C devices.
- LM3S devices support a 4.194304-MHz crystal. This crystal is not supported for TM4C devices, however a 32.768-kHz crystal is supported. In addition, an external load resistor is not required.
- Additional features are added for better battery management, hibernate after arbitrary power removal, sub-seconds counting, hardware calendar and alarm functions, tamper function and more. For more information, see the device-specific data sheet.

Two other changes to note include:

- TM4C devices have only one match register and interrupt compared to the two available on LM3S devices.
- TM4C devices have 16 words of battery-backed memory instead of the 64 words on LM3S devices.

As a result of the changes in TM4C devices, the following Driver Library APIs should not be used with the TM4C designs:

- The HIBERNATE_CLOCK_SEL_DIV128 parameter with the *HibernateClockSelect()* function
- The HIBERNATE_INT_RTC_MATCH_1 parameter with the *HibernateIntClear()*, *HibernateIntDisable()*, *HibernateIntEnable()*, *HibernateIntRegister()*, *HibernateIntStatus()*, and *HibernateIntUnregister()* functions
- The *HibernateRTCMatch1Get()* and *HibernateRTCMatch1Set()* functions

9 Internal Memory

The Flash memory that is used on TM4C devices is based on automotive-grade technology and provides 100,000 program/erase cycles. In addition, the Tiva C Series devices offer EEPROM with built-in wear leveling.

For TM4C123x devices, the Flash memory is single-cycle at 40 MHz and 1 wait state is automatically added, up to the maximum speed of 80 MHz. For TM4C129x devices, the timing for the Flash memory must be properly configured for the system clock frequency. The *SysCtlClockFreqSet()* function takes care of this programming automatically, but if this API is not used, the Memory Timing Parameter Register 0 for Main Flash and EEPROM (MEMTIM0) must be properly configured. Sandstorm- and Fury-class devices have a requirement that the system clock rate must be programmed in the USec Reload (USECRL) register using the *FlashUsecGet()* and *FlashUsecSet()* functions. These functions should not be used on TM4C devices.

The Flash memory on Tempest- and Firestorm-class devices requires that the device not be frequently powered on and off for less than 5 minutes at a time, and the Flash Control (FCTL) register is provided to ensure that the microcontroller is powered down in a controlled fashion in systems that may be affected by this situation. In addition, these devices require that two writes to the same word must be separated by an erase. None of these restrictions are carried forward with TM4C devices, and any software added to address them can be removed when porting code.

The Flash memory-resident registers also have changes in how they operate through the classes. Changing and committing the DBG field can permanently disable debug access to the device. Some devices allow this state to be reversed by the Debug Port Unlock sequence, but others do not. Some registers have an NW bit to indicate whether the register has been committed. These differences are summarized in Table 4.

Table 4. Flash Memory Resident Registers

Feature	Sandstorm	Fury	DustDevil	Tempest/ Firestorm	TM4C
DBG field location	FMPRE	USER_DBG	USER_DBG	BOOTCFG	BOOTCFG
Able to be restored once changed and committed	No	No	Yes	Yes	Yes
NW bit in USER_REGn registers	Yes	Yes	Yes	Yes	No
Able to change USER_DBG / BOOTCFG register after committing	No	No	No	No	Yes

Sandstorm- and Fury-class devices do not have on-chip ROM, but all other LM3S and TM4C devices do have ROM. Most DriverLib APIs are stored in ROM along with a basic bootloader, so more of the on-chip Flash memory is available for the application. Some LM3S devices have SafeRTOS in ROM, however there are not presently any TM4C devices with SafeRTOS in ROM.

10 Micro Direct Memory Access (µDMA)

The channel mapping for the µDMA controller changes among the classes. Sandstorm- and Fury-class MCUs do not have the µDMA controller. On DustDevil-class devices, there is only one possible channel assignment for each peripheral. On Tempest- and Firestorm-class devices, there is a primary and secondary assignment for each channel, configured by the DMA Channel Assignment (DMACHASGN) register. On TM4C123x devices, there are up to five assignments for each channel, configured by the DMA Channel Map Select n (DMACHMAPn) registers. TM4C129x devices expand the options to up to nine assignments per channel. From a software perspective, the *uDMAChannelSelectDefault()* and *uDMAChannelSelectSecondary()* APIs are used for Tempest- and Firestorm-class devices. These APIs still work on TM4C devices if the mappings are the same for the default and option 1 mapping. However, for mappings that are different or don't exist in earlier devices, the *uDMAChannelAssign()* API should be used.

11 General-Purpose Input/Outputs (GPIOs)

With the exception of the limit of 3.3-V tolerance on TM4C129x device inputs, there are generally no concerns with GPIOs when moving from LM3S to TM4C designs. The GPIOs on TM4C devices are more flexible, with added features such as per-pin interrupts, the ability to trigger µDMA, wake from hibernation, and increased drive strength options. For more information, see the device-specific data sheet.

12 External Peripheral Interface (EPI)

The EPI module on Tiva C Series devices is compatible with the EPI module on LM3S devices, and offers additional features such as higher speed, support for PSRAM, bursting, additional chip selects and more.

The EPI module has no significant concerns when moving from LM3S to TM4C designs. For more design recommendations, see the *EPI* section of the *System Design Guidelines for the TM4C129x Family of Tiva™ C Series Microcontrollers* (SPMA056). There are four changes that were made that could affect older designs:

- The WORD bit in the the EPI Host-Bus 8 Configuration 2 (EPIHB8CFG2), EPI Host-Bus 16 Configuration 2 (EPIHB16CFG2), and EPI General-Purpose Configuration 2 (EPIGPCFG2) registers has been removed
- The RD2CYC bit in the EPI General-Purpose Configuration (EPIGPCFG) register has been removed
- iRDY operation is no longer supported in General Purpose mode
- Dual chip select operation is no longer supported in Host Bus continuous read mode

The WORD bit is used to automatically route bytes of data onto the correct byte lanes enabling memories wider than 8 bits to be fully utilized. On TM4C129x devices, the data is automatically routed, meaning the bit is no longer necessary. The RD2CYC bit is required to be set on LM3S devices, so it was removed and all reads in General-Purpose mode are 2 cycles. As a result of these changes, the following API/parameter combinations should not be used:

- EPI_HB8_WORD_ACCESS with *EPIConfigHB8Set()*
- EPI_HB16_WORD_ACCESS with *EPIConfigHB16Set()*
- EPI_GPMODE_WORD_ACCESS with *EPIConfigGPModeSet()*
- EPI_GPMODE_READ2CYCLE with *EPIConfigGPModeSet()*
- EPI_GPMODE_RDYEN with *EPIConfigGPModeSet()*
- EPI_HB8_MODE_SRAM and EPI_HB8_CSCFG_ALE_DUAL_CS or EPI_HB8_CSCFG_DUAL_CS with *EPIConfigHB8Set()*
- EPI_HB16_MODE_SRAM and EPI_HB16_CSCFG_ALE_DUAL_CS or EPI_HB16_CSCFG_DUAL_CS with *EPIConfigHB16Set()*

13 General-Purpose Timers

The General-Purpose Timer modules on TM4C devices are compatible with the timer modules on LM3S devices, and offer additional features such as synchronization, wider counts in some modes, up and down counting in some modes, delayed load of new timer values, and more.

14 Watchdog Timers

The Watchdog Timer modules on TM4C devices are compatible with the Watchdog Timer modules on LM3S devices, and offer additional features such as a second module clocked by PIOSC and the option to generate an NMI on timeout.

15 Analog-to-Digital Converters (ADC)

The ADC module was redesigned for TM4C devices to provide higher accuracy. The key changes to consider when migrating designs from LM3S to TM4C devices are the changes to the internal and external references, the clocking changes, and the source resistance. On LM3S devices, the internal reference is a 3.0-V reference derived from the bandgap. TM4C devices do not have an internal reference, but can use VDDA and GNDA as the voltage reference. As a result, care should be taken to provide a clean VDDA and good ground isolation between analog and digital grounds. Firestorm-class devices also have the ability to select 10- or 12-bit resolution and an option for a 1.0-V reference, which are not supported on TM4C devices. Because of this change, the Firestorm APIs of *ADCResolutionGet()* and *ADCResolutionSet()* as well as the parameter of ADC_REF_EXT_1V in conjunction with *ADCReferenceGet()* or *ADCReferenceSet()* should not be used.

LM3S devices use the Run-Mode Clock Gating Control (RCGC0) register in the System Control module to configure the sampling speed. On the Tiva devices, this function is moved to the ADC Peripheral Configuration (ADCPC) register. As a result, the *SysCtlADCSpeedSet()* and *SysCtlADCSpeedGet()* functions should not be used on Tiva devices.

On LM3S devices that support an external reference, the reference voltage is provided on the VREF pin and can be between 2.97 V and 3.03 V. TM4C123x devices that provide an external reference have two reference pins, VREFA+ and VREFA-. VREFA+ must be between 2.4 V and VDDA, while VREFA- must be between GNDA and 0.3 V. An external decoupling capacitor is required between these two signals as shown in the device-specific data sheet. Some TM4C129x devices have the two reference voltage inputs, while others have only a single reference input, VREFA+.

As on LM3S devices, the PLL on TM4C123x devices is automatically divided down to provide a 16-MHz clock to the ADC. On TM4C123x devices, the PIOSC can also be used to clock the ADC at 16 MHz. TM4C129x devices have a configurable VCO frequency, so when using the ADC, care must be taken to use a VCO frequency that provides a clock in the proper frequency range to the ADC. For more information, see the *Module Clocking* section in the *ADC* section of the device-specific data sheet.

On TM4C123x devices, the effective input impedance is 500 Ωs. Care must be taken to ensure the input being sampled can supply this impedance requirement during the sample-and-hold window. TM4C129x devices have a configurable sample-and-hold window to support larger effective input impedances that is relative to the size of the sample-and-hold window. Note, however, that a longer sample-and-hold window results in a reduced conversion frequency. For more details, see the *ADC* section in the device-specific data sheet.

16 Universal Asynchronous Receivers/Transmitters (UARTs)

The UART modules on TM4C devices are compatible with those on LM3S devices, and offer additional features such as the option to clock the baud clock with the PIOSC and 9-bit support.

17 Synchronous Serial Interface (SSI)

The SSI modules on TM4C devices are compatible with those on LM3S devices, and offer additional features such as the option to clock the baud clock with the PIOSC and higher slave clock speeds. TM4C129x devices support bi-SSI, quad-SSI and advanced mode. In addition, the limit of the master clock of 25 MHz is removed, so the master clock can go up to 60 MHz, which is 1/2 the maximum clock speed of these devices. Two items to be aware of are that Microwire format is no longer supported on TM4C129x devices, and the legacy location of the SSI Rx and Tx signals has been swapped. SSI0Tx is on pin PA5 and SSI0Rx is on pin PA4 for all LM3S devices as well as TM4C123x series devices. On TM4C129x devices, the function of SSI0Tx is on SSI0XDAT0 which is on pin PA4 and the function of SSI0Rx is on SSI0XDAT1 which is on pin PA5.

18 Inter-Integrated Circuit (I2C) Interface

The main item to be aware of with the I2C Interface is that the SCL signal is not an open-drain signal on TM4C devices. As a result, the *GPIOPinTypeI2C()* API should not be used with the SCL signal; instead, use *GPIOPinTypeI2CSCL()*. In addition, the I2C Interface on TM4C devices has additional features such as a high-speed option, dual-slave address, clock low timeout, glitch suppression, µDMA support, transmit and receive FIFOs, and more. For more information, see the device-specific data sheet.

19 Controller Area Network (CAN) Module

The CAN module is the same in all LM3S and TM4C devices. The one change to be aware of is that on Fury-class devices, the CAN module runs on an 8-MHz clock generated from the PLL, so the PLL must be operating when using the CAN module. On all other LM3S and TM4C devices, the CAN module runs on the system clock.

20 Ethernet Controller

The Ethernet Controller on Tiva C Series devices is completely redesigned to provide much higher performance and capability. The new controller has integrated DMA to efficiently move large amounts of Ethernet data in the background. Several other features are included as well, such as VLAN tag detection, source and destination address filters, multicast address filtering, and more. For more information, see the device-specific data sheet. Note that when using the on-chip Ethernet PHY, a 25-MHz clock source must be connected to MOSC. Because of the integrated DMA controller, the µDMA is not used with the Ethernet Controller on these devices.

For system designers who use lwIP for their Ethernet stack, moving their code is very straightforward as they just have to include lwIP version 4.1 in their project. For system designers who do not use lwIP, code must be rewritten using the EMACXxxx APIs instead of the EthXxxx APIs in Driver Library. One hardware item to note is that the value of the resistor connected to the RBIAS signal on the TM4C devices is 4.87 KΩ ± 1%.

21 Universal Serial Bus (USB) Controller

The basic USB Controller is largely unchanged between LM3S and TM4C123x devices. The number of endpoints is 8 on DustDevil-class devices, 32 on Tempest- and Firestorm-class devices, and 16 on TM4C devices. In addition, the `USB0RBIAS` pin is no longer required on Tiva devices. The Valid ID feature is not supported on TM4C devices, but there are no Driver Library APIs for this function. The USB Controller on TM4C129x devices provides additional features such as integrated DMA dedicated to USB data transfer, a ULPI interface with optional high-speed operation, and LPM mode. An API was added, *USBControllerVersion()* that can be used to determine if these added features are available. Because of the integrated DMA controller, the µDMA is not used with the USB Controller on these devices.

22 Analog Comparators

The resistor ladder step sizes changed between the LM3S and TM4C devices. For a detailed explanation, see the device-specific data sheet. Otherwise, the modules are identical and all Driver Library APIs function on all devices.

23 Pulse Width Modulator (PWM)

The PWM modules are unchanged between LM3S and TM4C123x devices. TM4C129x devices add only an enhanced µDMA interface and alternate clocking capabilities. All Driver Library APIs that run on LM3S run on TM4C devices.

One item to note however, is that on LM3S and TM4C123x devices, the Run-Mode Clock Configuraton (RCC) register in the System Control module is used to configure the PWM clock divisor. On the TM4C129x devices, this function is moved to the PWM Clock Configuration (PWMCC) register. As a result, the *SysCtlPWMClockSet()* and *SysCtlPWMClockGet()* functions should not be used on TM4C129x devices. Instead the *PWMClockSet()* and *PWMClockGet()* functions should be used.

24 Quadrature Encoder Interface (QEI)

The QEI modules are unchanged between LM3S and TM4C devices, with the exception that the programmable noise filter that was added on Tempest-class devices carries through to the Firestorm-class and all TM4C devices. All Driver Library APIs that run on LM3S run on the TM4C devices.

25 Conclusion

Migrating designs from LM3S MCUs to Tiva C Series MCUs is very straightforward, with only a few items to keep in mind when updating the hardware and software. This guide, along with the documents referenced in Section 26 provide the necessary information to upgrade Stellaris LM3S designs.

26 References

The following related documents and software are available on the TI web site. Documents can also be found through the Tiva Technical Documents search tab.

- *Tiva™ C Series Data Sheet* (individual device-specific documents available through the product folders)
- *Tiva™ C Series TM4C129x Microcontrollers Silicon Revisions 1 and 2 Silicon Errata* (SPMZ850)
- *Tiva™ C Series TMS4C129x ROM User's Guide* (SPMU363)
- TivaWare™ Peripheral Driver Library for C Series
- *TivaWare™ Peripheral Driver Library User's Guide* (SPMU298)
- *Differences Among Stellaris® LM3S and Tiva™ C Series TM4C123x MCUs* (SPMA035)
- *Differences Between Tiva™ C Series Microcontrollers* (SPMA065)
- *Differences Between Stellaris® Tempest- and Firestorm-Class MCUs and Tiva™ C Series TM4C129x MCUs* (SPMA063)
- *Migrating Software Projects from StellarisWare® to TivaWare™* (SPMA050)
- *System Design Guidelines for the TM4C129x Family of Tiva™ C Series Microcontrollers* (SPMA056)
- *System Design Guidelines for the TM4C123x Family of Tiva™ C Series Microcontrollers* (SPMA059)

Appendix A Revision History

This document has been revised from SPMA049 to SPMA049A because of the following technical change(s).

Table 5. SPMA049A Revisions

Location	Additions, Deletes, and Edits
	Removed TM4C129x from the title
Table 1	Changed 'TM4C123x devices' to 'TM4C devices' the note
Section 4	Added 'and must be unlocked before their function can be changed' in the first bullet
Section 6	Changed end of the second sentence to 'support this capability only in Deep-sleep mode'.
Table 3	Updated information in TM4C123x and TM4C129x columns
Section 7	Changed information
Section 10	Changed information in first paragraph: from 'eight' to 'nine' assignments per channel
Section 12	Added information
Section 15	Added information
Section 20	Deleted information
Section 23	Added information

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