Application Report
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Differences Between Tiva™ C Series TM4C Microcontrollers

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ABSTRACT

This document addresses design considerations when migrating working designs between Tiva C Series TM4C123x and TM4C129x microcontrollers. While most modules shared among the devices are largely the same, some feature enhancements are worth noting. This document describes software and hardware differences for both feature changes and enhancements. All software differences are comprehended in the TivaWare™ for C Series APIs. As a result, system designers are strongly encouraged to use TivaWare to write software, making it easy to port software among various Tiva MCUs.

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1 Introduction

While most of the modules shared between the families are largely the same, some feature enhancements are worth noting. In this document, information on these minor implementation differences is presented by module, with both hardware and software considerations discussed. In general, features that are the same on all devices are not mentioned. Not all modules are included on every part. Modules on only one class of part are also not mentioned. In-depth descriptions of functions and features are not included; for further information on overall functionality or details on any item, see the microcontroller data sheet. Also, in general, differences due to errata are not comprehended in this document; see the errata document for a specific device to ensure proper system design.

This document addresses differences between the TM4C classes. For information on differences between Fury- through Firestorm-class and TMC123x devices, see *Differences Between Stellaris® LM3S and Tiva™ C Series TM4C123x MCUs* (SPMA035). For information on differences between Tempest- and Firestorm-class and TM4C129x MCUs, see *AN01288 - Differences Stellaris® Tempest- and Firestorm-Class MCUs and Tiva™ C Series TM4C129x MCUs* (SPMA063).

NOTE: By using TivaWare for C Series APIs, software can be easily ported among the various MCUs as these APIs comprehend functional differences.

2 ARM® Cortex™ CPU

Table 1. ARM Cortex-M Features

Feature	TM4C123x	TM4C129x
Cortex-M version	M4F, r0p1	M4F, r0p1

3 System Control

3.1 Peripheral Control and Capabilities

Table 2. Peripheral Control and Capabilities Registers

Feature	TM4C123x	TM4C129x
Legacy SRCRn, RCGCn, SCGCn, DCGCn, and DCn registers present	Yes	No

3.2 Operating Voltages

Table 3. Operating Voltages

Feature	TM4C123x	TM4C129x
VDD operating voltages	3.15 to 3.63 V	2.97 to 3.63 V
VDDA operating voltages	2.97 to 3.63 V	2.97 to 3.63 V

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3.3 Reset Operation

Table 4. Reset Operation

Feature	TM4C123x	TM4C129x
Hardware System Service reset	No	Yes
Enhanced BOR function	No	Yes
Choice of reset behavior	No	Yes
Reset JTAG using TMS pin	No	Yes
Hibernation reset reported in the Reset Cause register	No	Yes

3.4 Brown-Out Operation

Table 5. Brown-Out Operation

Feature	TM4C123x	TM4C129x
Default brown-out operation	Interrupt	POR
Available BOR voltage levels	2	1
Brown-out control register	PBORCTL	PTBOCTL
Power-temperature cause register	No	PWRTC

3.5 Clocking

NOTE: TivaWare for C Series APIs have been added to adjust for these functional differences, see Section 3.10.

Table 6. System Clock Options

Feature	TM4C123x	TM4C129x
Clock configuration registers	RCC, RCC2, and DSLPCLKCFG	RSCLKCFG, DSCLKCFG, PLLFREQ0 and PLLFREQ1
Alternate Clock Configuration Register (ALTCLKCFG)	No	Yes
SESRC bit in MOSCCTL register (Single-Ended Source)	No	Yes
OSCRNG bit in MOSCCTL register (Oscillator Range)	No	Yes
PWRDN bit in MOSCCTL register (Power Down)	No	Yes
MOSCDPD bit in DSCLKCFG register (MOSC Disable Power Down)	No	Yes
DIVSCLK output signal	No	Yes

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Table 7. Module Clocking

Feature	TM4C123x	TM4C129x
PIOSC divide by 4 available for use as system clock	Yes	No
Hibernate RTCOSC	32.768-kHz oscillator; 32.768-MHz crystal	32.768-kHz oscillator; 32.768-kHz crystal, internal Hibernate LFIOSC
ADC	PLL/25, 16-MHz MOSC, or PIOSC	Derived from main PLL, MOSC, or PIOSC
USB	Dedicated PLL	Derived from main PLL (1)
Ethernet PHY	N/A	25-MHz MOSC
GPTM	System clock	System clock or alternate clock (choose from PIOSC, LFIOSC, and Hibernation module RTCOSC)
SSI baud clock	System clock or PIOSC	System clock or alternate clock
UART baud clock	System clock or PIOSC	System clock or alternate clock

(1) The ULPI interface uses either the main PLL or the USB0CLK input.

3.6 NMI

Table 8. NMI Characteristics

Feature	TM4C123x	TM4C129x
NMI signal location	PD7 and PF0	PD7 and PE7
Tamper event can cause NMI	N/A	Yes
Voltage under BOR setting	No	Yes
NMI Cause register	No	NMIC

3.7 GPIO High-Performance Bus Control

Table 9. GPIO Ports Available on AHB

Feature	TM4C123x	TM4C129x
GPIO ports available on AHB	Port A - Port J (1)	All ports available only on the AHB

(1) Ports K and higher are only available on the AHB. The corresponding bits in the GPIO High-Performance Bus Control (GPIOHBCTL) register must always be set.

3.8 Flash and EEPROM Memory Timing

Table 10. Flash and EEPROM Memory Timing Control

Feature	TM4C123x	TM4C129x
MEMTIM0 and DSMEMTIM0 registers	No	Yes

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3.9 Peripheral Power Control Features

Table 11. Peripheral Power Control Registers

Feature	TM4C123x	TM4C129x
USB Power Domain Status and Memory Power Control registers, USB Power Control register	No	USBPDS, USBMPC, PCUSB
Ethernet MAC Power Domain Status and Memory Power Control registers, Ethernet MAC Power Control and Ethernet PHY Power Control registers	N/A	EMACPDS, EMACMPC, PCEMAC, PCEPHY
LCD Power Domain Status and Memory Power Control registers, LCD Controller Power Control register	N/A	LCDPDS, LCDMPC, PCLCD
CAN Power Domain Status and Memory Power Control registers, CAN Power Control register	No	CANnPDS, CANnMPC, PCCAN
CRC and Cryptographic Modules Power Control register	N/A	PCCCM

3.10 TivaWare for C Series APIs

In this section and sections like it throughout this document, the APIs shown in the table are applicable APIs. The ROM version of the various APIs may or may not be included in the on-chip ROM. To determine which APIs are available in ROM, see the *Tiva™ C Series TMS4C129x ROM User's Guide* (SPMU363).

Table 12. System TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
SysCtlAltClockConfig	No	Yes
SysCtlClockFreqSet	No	Yes
SysCtlClockSet, SysCtlClockGet	Yes	No
SysCtlCodeSRAMSizeGet	Yes (1)	Yes (1)
SysCtlClockOutConfig	No	Yes
SysCtlDeepSleepClockSet	Yes	No
SysCtlDeepSleepClockConfigSet	No	Yes
SysCtlFlashTming, SysCtlFlashDeepSleepTiming, SysCtlEEPROMTiming	No	Yes
SysCtlLPCLowPowerConfigSet, SysCtlLPCLowPowerStatusGet	No	Yes
SysCtlMOSCConfigSet, SYSCTL_MOSC_PWR_DIS, SysCtlMOSCConfigSet, SYSCTL_MOSC_PWR_DIS, SYSCTL_MOSC_SESRC	No	Yes
SysCtlNMIStatus, SysCtlNMIClear	No	Yes
SysCtlResetBehaviorSet, SysCtlResetBehaviorGet	No	Yes
SysCtlResetCauseClear, SysCtlResetCauseGet, SYSCTL_CAUSE_HSRVREQ, SYSCTL_CAUSE_HIB	No	Yes
SysCtlVoltageEventConfig, SysCtlVoltageEventStatus, SysCtlVoltageEventClear	No	Yes

(1) Returns a 0 to indicate no code SRAM on these devices.

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4 Hibernation Module

4.1 Features

Table 13. Hibernation Features

Feature	TM4C123x	TM4C129x
Hardware calendar and alarm functions	No	Yes
V_{DD} supplies power even when $V_{BAT} > V_{DD}$	No	Yes
Wake from GPIO or $\overline{RST}$	No	Yes
Tamper function	No	Yes
Low-frequency internal oscillator (LFIOSC)	No	Yes
Pins that do not retain state in VDD3ON mode	None	Port C[0:3]
Minimum Sysclk required when reading HIBRTCC	No	Yes
RETCLR bit to retain GPIO state until cleared by software	No	Yes
External wake interrupt can be used in run, sleep and deep-sleep modes	No	Yes
External wake interrupt must be manually cleared	No	Yes

4.2 Clocking Options

Table 14. Hibernation Clocking Options

Feature	TM4C123x	TM4C129x
HIB Low-Frequency Oscillator (HIBLFIOSC)	No	Yes
Hibernate cock (RTCOSC) can be used as the system clock source	No	Yes
Hibernate clock output	No	Yes

4.3 Hibernate Interrupt Sources

Table 15. Hibernate Interrupt Sources

Feature	TM4C123x	TM4C129x
PADIOWK	No	Yes
RSTWK	No	Yes
VDDFAIL	No	Yes

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4.4 TivaWare for C Series APIs

Table 16. Hibernate TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
HibernateCalendarSet, HibernateCalendarGet, HibernateCalendarMatchSet, HibernateCalendarMatchGet	No	Yes
HibernateClockConfig, HIBERNATE_OSC_LFIOSC, HIBERNATE_OUT_SYSCLK, HIBERNATE_OUT_ALT1CLK	No	Yes
HibernateCounterMode	No	Yes
HibernateClockSelect, HIBERNATE_CLOCK_SEL_LFIOSC	No	Yes
HibernateIntClear, HibernateIntDisable, HibernateIntEnable, HibernateIntRegister, HibernateIntStatus, HibernateIntUnregister, HIBERNATE_INT_RESET_WAKE, HIBERNATE_INT_GPIO_WAKE	No	Yes
HibernateIntClear, HibernateIntDisable, HibernateIntEnable, HibernateIntRegister, HibernateIntStatus, HibernateIntUnregister, HIBERNATE_INT_VDDFAIL	No	Yes
HibernateTamperEnable, HibernateTamperEventsConfig, HibernateTamperEventsGet, HibernateTamperEventsClear, HibernateTamperDisable, HibernateTamperIOEnable, HibernateTamperIODisable, HibernateTamperStatusGet, HibernateTamperExtOscRecover, HibernateTamperExtOscValid	No	Yes
HibernateWakeSet,HibernateWakeGet,HIBERNATE_WAKE_GPIO, HIBERNATE_WAKE_RESET	No	Yes
HibernateWakeSet, HibernateWakeGet, HIBERNATE_WAKE_TAMPER	No	Yes

5 Internal Memory

5.1 Features

Table 17. Internal Memory Features

Feature	TM4C123x	TM4C129x
ROM	Yes	Yes
Flash Memory	384 KB - 512 KB	512 KB - 1024 KB
Code SRAM	N/A	N/A
SRAM	12 KB - 32 KB	128 KB - 256 KB
EEPROM	2 KB	6 KB

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5.2 Flash Memory Features

Table 18. Flash Memory Features

Feature	TM4C123x	TM4C129x
Organization	1-KB blocks	2 (512-KB) or 4 (1024-KB) banks of 8 K x 128 bits, two-way interleaved
Erase size	1 KB	16 KB
Speed	40 MHz	16 MHz
Prefetch buffer	2 32-bit words	2 x 256-bit buffer or 4 x 256-bit buffer
Programmable wait states	No	Yes
Flash mirroring	No	Yes
Program protection	2-KB blocks	16-KB blocks
Read protection	2-KB blocks	2-KB blocks
µDMA read access	No	Yes
Flash Configuration register	No	FLASHCONF

5.3 Memory Registers

Table 19. Memory Registers

Feature	TM4C123x	TM4C129x
Reset Vector Pointer register	No	RVP
ROM Control register	Yes	No
User Power-up Control register	No	USRPWRUP

5.4 TivaWare for C Series APIs

There are no differences in the TivaWare for C Series APIs for Internal Memory among the TivaWare for C Series devices.

6 Micro Direct Memory Access (µDMA)

6.1 Features

NOTE: TivaWare for C Series APIs automatically adjust for these functional differences.

Table 20. µDMA Features

Feature	TM4C123x	TM4C129x
Transfer from Flash Memory	No	Yes
Possible channel mapping encoding	5	9
Option in basic mode to continue transferring as long as peripheral request is asserted	No	Yes
DMA Done interrupts in the Interrupt registers in each peripheral	No	Yes
Privilege access protection	No	Yes
DMA Channel Interrupt Status Register (DMACHIS)	Yes	No
DMA Channel Map Select n Registers (DMACHMAPn)	No	Yes

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6.2 Peripherals

Table 21. Peripheral µDMA Request Types

Feature	TM4C123x	TM4C129x
ADC	Single - N/A Burst - FIFO half full	Single - FIFO not empty Burst - FIFO half full
USB TX	Burst - FIFO TXRDY	USB has integrated DMA and does not use µDMA
USB RX	Burst - FIFO RXRDY	USB has integrated DMA and does not use µDMA
GPIO	Single - triggered by raw interrupt pulse Burst - N/A	Single - N/A Burst - trigger event
I2C TX	N/A	Single - TX buffer not full Burst - TX FIFO level (configurable)
I2C RX	N/A	Single - RX buffer not full Burst - RX FIFO level (configurable)

6.3 TivaWare for C Series APIs

There are no differences in the TivaWare for C Series APIs for µDMA between the TivaWare for C Series devices, except for the peripherals that can be DMA bus masters, which have the DMA APIs included in the APIs for those modules.

7 General-Purpose Input/Outputs (GPIOs)

7.1 Features

Table 22. GPIO Features

Feature	TM4C123x	TM4C129x
Input voltage tolerance	5 V	3.3 V (1)
I/O pins clamped by diode when device Is unpowered	Yes	No
Available ports	A - G, 64-pin parts A - K, 100-pin parts A - P, 144-pin parts A - Q, 157-pin parts	A - Q, 128-pin parts A - T, 212-pin parts
Bus location	A-J APB or AHB, K-Q AHB only	A-T AHB only
6-, 10- and 12-mA drive options	No	Yes
Pins that can wake from Hibernation	N/A	Port K [7:4]
Pins with default functions	PA[1:0] - UART0 PA[5:2] - SSI0 PB[3:2] - I2C0 PC[3:0] - JTAG/SWD	PC[3:0] - JTAG/SWD
µDMA Done interrupt	No	Yes

(1) PB1 (USB0VBUS) is 5-V tolerant.

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7.2 TivaWare for C Series APIs

Table 23. GPIO TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
GPIOIntEnable, GPIOIntDisable, GPIOIntStatus, GPIOIntClear	No	Yes
GPIOPadConfigSet,GPIOPadConfigGet, GPIO_STRENGTH_6MA, GPIO_STRENGTH_10MA, PIO_STRENGTH_12MA	No	Yes
GPIOPadConfigSet, GPIOPadConfigGet, GPIO_PIN_TYPE_WAKE_HIGH, GPIO_PIN_TYPE_WAKE_LOW	No	Yes
GPIOPinTypeWakeHigh, GPIOPinTypeWakeLow, GPIOPinWakeStatus	N/A	Yes
GPIOPinTypeLCD, GPIOPinTypeEthernetMII, GPIOPinTypeEthernetLED	N/A	Yes

8 External Peripheral Interface (EPI)

TM4C123x devices do not have EPI. For information on differences for this module between Tempest- and Firestorm-class and TM4C129x MCUs, see *AN01288 - Differences Between Stellaris® Tempest and Firestorm MCUs and Tiva™ C Series TM4C129x MCUs* (SPMA063).

9 General-Purpose Timers

9.1 Features

Table 24. General-Purpose Timer Features

Feature	TM4C123x	TM4C129x
16/32-bit timers	Yes	Yes
32/64-bit timers	Yes	No
Clocking options	System clock only	System clock or alternate clock
Configurable ADC and µDMA trigger events	No	Yes
Timer Compare Action mode	No	Yes
µDMA Done interrupt	No	Yes

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9.2 TivaWare for C Series APIs

Table 25. General-Purpose Timer TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
TimerADCEventSet, TimerADCEventGet	No	Yes
TimerConfigure, TIMER_CFG_A_ACT_TOINTD, TIMER_CFG_A_ACT_NONE, TIMER_CFG_A_ACT_TOGGLE, TIMER_CFG_A_ACT_CLRTO, TIMER_CFG_A_ACT_SETTO, TIMER_CFG_A_ACT_SETTOGTO, TIMER_CFG_A_ACT_CLRTOGTO, TIMER_CFG_A_ACT_CLRSETTO, TIMER_CFG_B_ACT_TOINTD, TIMER_CFG_B_ACT_NONE, TIMER_CFG_B_ACT_TOGGLE, TIMER_CFG_B_ACT_CLRTO, TIMER_CFG_B_ACT_SETTO, TIMER_CFG_B_ACT_SETTOGTO, TIMER_CFG_B_ACT_CLRTOGTO, TIMER_CFG_B_ACT_CLRSETTO,	No	Yes
TimerClockSourceSet, TimerClockSourceGet	No	Yes
TimerDMAEventSet, TimerDMAEventGet	No	Yes
TimerIntEnable, TimerIntDisable, TimerIntClear, TimerIntStatus, TIMER_TIMA_DMA, TIMER_TIMB_DMA	No	Yes

10 Watchdog Timers

There are no differences among the Watchdog Timers on the various classes of product.

11 Analog-to-Digital Converters (ADC)

11.1 Features

Table 26. ADC Features

Feature	TM4C123x	TM4C129x
2 Msps operation	No	Yes
Enhanced µDMA interface	No	Yes
Clocking options	Automatic PLL / 25, MOSC, PIOSC	Derived from main PLL, MOSC, or alternate clock
Never trigger option available	No	Yes
Configurable sample and hold time	No	Yes
DITHER bit enabled at reset	No	Yes

11.2 TivaWare for C Series APIs

Table 27. ADC TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
ADCIntDisableEx, ADCIntEnableEx, ADCIntStatusEX, No ADCIntClearEx	No	Yes
ADCSequenceConfigure, ADC_TRIGGER_NEVER	No	Yes
ADCSequenceDMAEnable, No ADCSequenceDMADisable	No	Yes

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12 Universal Asynchronous Receivers/Transmitters (UARTs)

12.1 Features

Table 28. UART Features

Feature	TM4C123x	TM4C129x
Modem support	Modem flow control and status on UART1 on some devices; Modem flow control on UART1 on the rest	Modem flow control and status on UART0 and UART1 Modem flow control on UART2, UART3, and UART4
Clocking options	System clock, PIOSC	System clock, alternate clock
Enhanced µDMA interface	No	Yes

12.2 TivaWare for C Series APIs

Table 29. UART TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
UARTIntEnable, UARTIntDisable, UARTIntClear, UARTIntStatus, UART_INT_DMARX, UART_INT_DMATX	Yes	No

13 Synchronous Serial Interface (SSI)

13.1 Features

Table 30. SSI Features

Feature	TM4C123x	TM4C129x
Module types	Four legacy modules	Four modules support legacy, advanced, bi-SSI and quad-SSI
Maximum master clock speed	1/2 system clock speed up to 25 MHz	1/2 system clock speed
SSI0 transmit and receive pin mapping	SSI0Rx - PA4 SSI0Tx - PA5	SSI0XDAT1 (SSI0Rx) - PA5 SSI0XDAT0 (SSI0Tx) - PA4
Enhanced µDMA interface	No	Yes
Clocking options	System clock, PIOSC	System clock, alternate clock
High-speed clock option	No	Yes
Supported frame formats	TI, Freescale, Microwire	TI, Freescale (1)
Separate EOT interrupt	No	Yes
FSS hold frame option	No	Yes

(1) Note that in advanced, bi and quad modes, the only configuration that can be used is the Freescale mode with SPO = 0 and SPH = 0.

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13.2 TivaWare for C Series APIs

Table 31. SSI TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
SSIAdvDataPutFrameEnd, SSIAdvDataPutFrameEndNonBlocking	No	Yes
SSIAdvFrameHoldEnable, SSIAdvFrameHoldDisable	No	Yes
SSIAdvModeSet	No	Yes
SSIIntEnable, SSIIntDisable, SSIIntClear, SSIIntStatus, SSI_DMARX, SSI_DMATX, SSI_TXEOT	No	Yes
SSISlaveDiv6Enable, SSISlaveDiv6Disable	No	Yes

14 Inter-Integrated Circuit (I2C) Interface

14.1 Features

Table 32. I2C Features

Feature	TM4C123x	TM4C129x
Receive and transmit FIFOs	No	Yes
µDMA support	No	Yes
Multi-master disable option	No	Yes
Location of glitch suppression control	Enable in I2C Mater Configuration (I2CMCR) register, width control in I2C Master Configuration 2 (I2CMCR2) register	I2C Master Timer Period (I2CMTPR) register
Burst operation option	No	Yes

14.2 I2C Interrupt Sources

Table 33. I2C Interrupt Sources

Feature	TM4C123x	TM4C129x
DMARXRIS, DMATXRIS (µDMA interrupts)	No	Yes
NACKRIS (NACK interrupt)	No	Yes
STARTRIS, STOPRIS (start and stop detection)	No	Yes
ARBLOSTRIS (arbitration lost)	No	Yes
RXRIS, TXRIS (FIFO interrupts)	No	Yes
TXFERIS, RXFFRIS (FIFO interrupts)	No	Yes
DATARIS (slave data interrupt)	No	Yes

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14.3 TivaWare for C Series APIs

Table 34. I2C TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
I2CFIFOStatus, I2CFIFODataPut, I2CFIFODataPutNonBlocking, I2CFIFODataGet, I2CFIFODataGetNonBlocking	No	Yes
I2CMasterBurstLengthSet, I2CMasterBurstCountGet	No	Yes
I2CMasterControl, No I2C_MASTER_CMD_FIFO_SINGLE_SEND, I2C_MASTER_CMD_FIFO_SINGLE_RECEIVE, I2C_MASTER_CMD_FIFO_BURST_SEND_START, I2C_MASTER_CMD_FIFO_BURST_SEND_CONT, I2C_MASTER_CMD_FIFO_BURST_SEND_FINISH, I2C_MASTER_CMD_FIFO_BURST_SEND_ERROR_STOP, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_START, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_CONT, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_FINISH, I2C_MASTER_CMD_FIFO_BURST_RECEIVE_ERROR_STOP	No	Yes
I2CMasterGlitchFilterConfigSet	No	Yes
I2CMasterIntEnableEx, I2CMasterIntDisableEx, I2CMasterIntStatusEx, I2CMasterIntClearEx, I2C_MASTER_INT_RX_FIFO_FULL, I2C_MASTER_INT_TX_FIFO_EMPTY, I2C_MASTER_INT_RX_FIFO_REQ, I2C_MASTER_INT_TX_FIFO_REQ, I2C_MASTER_INT_ARB_LOST, I2C_MASTER_INT_STOP, I2C_MASTER_INT_START, I2C_MASTER_INT_NACK, I2C_MASTER_INT_TX_DMA_DONE, I2C_MASTER_INT_RX_DMA_DONE	No	Yes
I2CMasterMultiMasterEnable, I2CMasterMultiMasterDisable	No	Yes
I2CRxFIFOConfigSet, I2CRxFIFOFlush	No	Yes
I2CSlaveFIFOEnable, I2CSlaveFIFODisable	No	Yes
I2CSlaveIntEnable, I2CSlaveIntDisableEx, I2CSlaveIntStatusEx, I2CSlaveIntClearEx, I2C_SLAVE_INT_RX_FIFO_FULL, I2C_SLAVE_INT_TX_FIFO_EMPTY, I2C_SLAVE_INT_RX_FIFO_REQ, I2C_SLAVE_INT_TX_FIFO_REQ, I2C_MASTER_INT_ARB_LOST, I2C_SLAVE_INT_TX_DMA_DONE, I2C_SLAVE_INT_RX_DMA_DONE	No	Yes
I2CTxFIFOConfigSet, I2CTxFIFOFlush	No	Yes

15 Controller Area Network (CAN) Module

There are no differences among the CAN modules between Tempest- and Firestorm-class and TM4C129x devices.

16 Ethernet Controller

TM4C123x devices do not have the Ethernet controller module. For information on differences for this module among Tempest, Firestorm and TM4C129x classes, see *AN01288 - Differences Between Stellaris® Tempest and Firestorm MCUs and Tiva™ C Series TM4C129x MCUs* (SPMA063).

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17 Universal Serial Bus (USB) Controller

17.1 Features

Table 35. USB Controller Features

Feature	TM4C123x	TM4C129x
Integrated USB DMA with bus master capability	No	Yes
ULPI interface with optional high-speed operation	No	Yes
Link Power Management (LPM) mode	No	Yes
Enhanced control of USB0VBUS and USB0ID signals	No	Yes
Valid ID detect	Yes	No
Test packet support	No	Yes
USB information registers (USBEPINFO and USBRAMINFO)	No	Yes
Ping disable	No	Yes
Incomplete RX transmission status	No	Yes

17.2 TivaWare for C Series APIs

Table 36. USB TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
USBClockEnable, USBClockDisable	No	Yes
USBControllerVersion	No	Yes
USBDevEndpointConfigSet, USB_EP_DIS_NYET, USB_EP_SPEED_HIGH, USB_EP_DMA_INT_EN, USB_EP_DMA_DISABLE	No	Yes
USBDevLPMConfig, USBDevLPMRemoteWake, USBDevLPMEnable, USBDevLPMDisable	No	Yes
USBDMAChannelAddressSet, USBDMAChannelAddressGet, USBDMAChannelCountSet, USBDMAChannelCountGet, USBDMANumChannels, USBDMAChannelAssign	No	Yes
USBDMAChannelEnable, USBDMAChannelDisable, USBDMAChannelConfigSet, USBDMAChannelStatus, USBDMAChannelStatusClear	No	Yes
USBDMAChannelIntEnable, USBDMAChannelIntDisable, USBDMAChannelIntStatus	No	Yes
USBDMAError, USBDMAErrorClear	No	Yes
USBDMAModeSet, USBDMAModeGet	No	Yes
USBHighSpeed, USBDevSpeedGet	No	Yes
USBHostEndpointSpeed, USBHostEndpointPing	No	Yes
USBHostLPMConfig, USBHostLPMSend, USBHostLPMResume	No	Yes
USBHostSpeedGet, USB_HIGH_SPEED	No	Yes
USBLPMLinkStateGet, USBLPMIntEnable, USBLPMIntDisable, USBLPMIntStatus	No	Yes
USBRequestPacketCountSet	No	Yes
USBULPIConfig, USBULPIEnable, USBULPIDisable, USBULPIRegRead, USBULPIRegWrite	No	No

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18 Analog Comparators

There are no differences among the Analog Comparators between Tempest- and Firestorm-class and TM4C devices.

19 Pulse Width Modulator (PWM)

19.1 Features

Table 37. PWM Controller Features

Feature	TM4C123x	TM4C129x
PWM Clock Configuration register	Run-mode Clock Configuration (RCC) register in System Control	PWM Clock Configuration (PWMCC)

19.2 TivaWare for C Series APIs

Table 38. PWM TivaWare for C Series Available Functions and Parameters

Driver Library Function/Parameter	TM4C123x	TM4C129x
PWMClockSet, PWMClockGet	No	Yes

20 Quadrature Encoder Interface (QEI)

There are no differences among the QEI modules between Tempest- and Firestorm-class and TM4C devices.

21 Packaging and Pinout

21.1 Packages

Table 39. Device Packages

Feature	TM4C123x	TM4C129x
64-pin LQFP, 10 x 10 mm body size, 0.50 mm pitch	Yes	No
100-pin LQFP, 14 x 14 mm body size, 0.50 mm pitch	Yes	No
128-pin TQFP, 14 x 14 mm body size, 0.40 mm pitch	No	Yes
144 LQFP, 20 x 20 mm body size, 0.50 mm pitch	Yes	No
157 BGA, 9 x 9 mm body size, 0.65 mm pitch, 13 x 13 array	Yes	No
212-ball BGA, 10 x 10 mm body size, 0.5 mm pitch, No 19 x 19 array	No	Yes

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21.2 Pinout Comparison

Table 40. Device Pinout

Feature	TM4C123x	TM4C129x
ADC	Top left corner	Top left corner
Hibernate	Bottom right corner	Bottom right corner
JTAG	Right side of top	Right side of top
VDDC	Center top side, center bottom side; BGA has a third pin in the center on the left	Center of top, center of right sider
UART0	Left of bottom side	Left of bottom side
SSI0	Left of bottom side	Left of bottom side
I2C0	Top of right side	Top of right side
USB0	Top of right side	Top of right side
Reset	Center of right side	Lower right side
Oscillator pins	Center of right side	Upper right side

22 Conclusion

Among the various classes of Tiva C Series microcontrollers, there are minor hardware and software differences. This application report has provided an overview of these differences for the TM4C123x and TM4C129x classes. By using TivaWare for C Series APIs, software can be easily ported among the various classes.

23 References

The following related documents and software are available on the TI web site. Documents can also be found through the Tiva Technical Documents search tab.

- Tiva C Series Data Sheet (individual device documents available through the product folders)
- *Tiva™ C Series TM4C129x Microcontrollers Silicon Revisions 1 and 2 Silicon Errata* (SPMZ850)
- TivaWare Peripheral Driver Library for C Series
- *TivaWare™ Peripheral Driver Library User's Guide* (SPMU298)
- *Tiva™ C Series TMS4C129x ROM User's Guide* (SPMU363)
- *Differences Among Stellaris® LM3S and Tiva™ C Series TM4C123x MCUs* (SPMA035)
- *Transitioning Designs from Stellaris® LM3S Microcontrollers to Tiva™ C Series Microcontrollers* (SPMA049)
- *Differences Between Stellaris Tempest- and Firestorm-Class MCUs and Tiva C Series 4C129x MCUs* (SPMA063)
- *Migrating Software Projects from StellarisWare® to TivaWare™* (SPMA050)
- *System Design Guidelines for the TM4C129x Family of Tiva™ C Series Microcontrollers* (SPMA056)
- *System Design Guidelines for the TM4C123x Family of Tiva™ C Series Microcontrollers* (SPMA059)

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